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RESEARCH ARTICLE

Implications of Various Charge Sources in AlGaN/GaN Epi-Stack on the Drain & Gate Connected Field Plate Design in HEMTs

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ABSTRACT We have established that a design strategy for drain and gate connected field plates should be adopted while keeping in mind the interplay of various charge sources across AlGaN/GaN epi-stack, which governs the electric field distribution across HEMT. The investigations in this work are carried out for Schottky, MIS and p-GaN gate stacks while accounting for possible GaN buffer types (Fe-doped and C-doped). The role of gate and drain field plates was found to be different in the Fe-doped buffer compared to the C-doped buffer. More than suppression of avalanche generation, mitigation of gate injection by shifting the peak electric field position away from the gate edge was found to be the dominant cause of breakdown voltage improvement when field plates were adopted. In a few cases, however, the widening of the depletion region near the gate or dominance of the buffer field was the reason for breakdown voltage improvement with a gate field plate. On the other hand, the drain field plate was found to be effective only for lower polarization % and lower surface trap concentration. The role of buffer trap parameters, surface/passivation trap concentration, interface trap concentration at the gate, and passivation thickness in defining the optimum field plate strategy are discussed.

INDEX TERMS AlGaN/GaN HEMT, field plate, field plate design, HEMT simulation, GaN HEMT, TCAD.

I. INTRODUCTION

The localized high electric field regions lead to premature breakdown and other reliability issues in AlGaN/GaN HEMTs. To address this, electric field engineering to redistribute it uniformly across the active region of the device is often adopted. Employing a field plate is one such technique that has been widely adopted for improving the breakdown voltage in HEMTs and the majority of other high power devices. It is imperative for a device designer to know which field plate topology should be selected to maximize the breakdown voltage and mitigate reliability issues. Simultaneously, an optimum field plate design is necessary to ensure the device's ON state performance and parasitic capacitance is not compromised. In principle, the selection of field plate strategy and its design should be strongly correlated to the location of electric field peaks in the device and relative strengths, respectively. Earlier works have shown device failure or peak electric field location at the gate edge. Hence, gate connected field plate [1]–[9] or source connected field plate [10]–[13] was employed to improve the breakdown voltage. On the other hand, several other works report electric field peak at the drain edge [13]–[18] and therefore drain connected field plates were used in these cases. Whereas, few other works reported improvement in breakdown voltage when both gate and drain connected (dual) field plates were used [11], [15]. However, it is not clear under which physical scenario a given field plate approach should be used. The ambiguities present in previous works present a huge challenge in deriving universal field plate design guidelines for AlGaN/GaN HEMTs. Besides, most of the earlier works are limited to UID buffers and

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Schottky gates, limiting its application in more advanced gate stacks and buffer types. The gap has been elaborated below.

Karmalkar *et al.*. [4] presented a gate field plate for AlGaN/GaN HEMTs, which was limited to the optimization of passivation material and thickness. Saito *et al.* [12] reported the field plate scaling as a function of the gate to drain distance, field plate length and buffer thickness. However, these optimization studies were limited to UID buffer and Schottky gates without accounting for crucial parameters such as polarization charge, surface, and buffer traps. Dual field plate architectures have been reported in [9], [15]. However, the implementation of the dual field plate is rather ambiguous. Karmalkar *et al.* [9] proposed dual field plate architecture in a RESURF HEMT structure, where the drain field peak is observed due to the RESURF effect. Whereas Saito *et al.* [15], suggest that the dual field plate suppresses a high drain field caused by space charge modification in the undoped barrier layer. The influence of surface defect charge, breakdown voltage, and field plate scaling is discussed in [19]. However, The surface defects are accounted for by assuming a 20nm thick doped AlGaN layer, which may not reflect the realistic device behavior in case of an undoped barrier HEMT. Our earlier work proposed novel drain field plate HEMT designs with improved breakdown and RF performance [20]. While most of the reports demonstrate improved breakdown voltage by implementing a field plate, however, the physics behind the electric field distribution and field plate design is largely missing in previous works. Moreover, besides the location of field plate, other design aspects of field plate for achieving optimum performance are also required to be understood, which depends on the strength of the electric field and its dependence on various charge sources (across the Epi-stack), charge concentrations, polarization percentage, and gate stack type. The latter aspects are by and large missing in previously published works.

The past works on the design of field plates lack in following aspects – (i) As presented in our earlier work, the electric field is primarily derived from the charge dynamics in the device [21]. In HEMT, buffer and surface play a crucial role in modifying the field profile and hence the device's breakdown voltage. Buffer traps are ionized charges that modulate the electric field in the channel. With the advent of Fe-doped and C-doped buffers, it is critical to account for its impact on field plate design. However, the impact of buffer doping on-field plate design strategy has been missing in prior works. (ii) Earlier works, which are based on TCAD computations, did not account for the effect of surface traps and polarization charges in the adopted simulation framework. The breakdown voltage optimization studies were performed in the previous reports by assuming a fixed sheet charge in the barrier to emulate 2DEG. However, this approach fails to accurately capture physical behavior as the electric field distribution is sensitive to these parameters and hence cannot be ignored. (iii) While there are a few optimization studies on the impact of passivation thickness, buffer thickness, and the gate to drain spacing on the field plate design; an elaborated design methodology for field plates is missing. Besides, the previous field plate design and modeling works have been derived for the Schottky gate stack. Its validity for MIS and p-GaN gate stack is not investigated. Lack of physics-based design guidelines cost a lot of resource and optimization time. Keeping this gap in mind, the objective of this work is to develop field plate design guidelines for AlGaN/GaN HEMTs while using the physical insights develop in the earlier work [21]. The guidelines developed in this work accounts for various buffer types/buffer charges (acceptors and donors), different gate stack (Schottky, MIS and p-GaN), surface charge/traps, interface traps for a range of polarization charge/polarization percentage.

II. ELECTRIC FIELD DISTRIBUTION GOVERNED BY INTERPLAY OF VARIOUS CHARGES

In the earlier work [21], we revealed that the electric field position and strength in AlGaN/GaN HEMTs are a strong function of surface traps, polarization charge, nature of buffer traps and relative concentration of various types of charges present. The field plate design approach discussed in this work is based upon these findings while keeping in mind (i) the spatial field profile at the breakdown, as depicted in Fig. 1, to identify field plate topology and (ii) the relative charge concentrations as well as gate stack type for finding the optimum design window for a given field plate topology. Fig. 1 shows that in the case of Fe doped buffer, the electric field peaks at the gate edge under breakdown condition for 2DEG density (n_s) greater than a specific critical 2DEG concentration (n_c). Whereas, for $n_s < n_c$, breakdown occurs at the drain contact. On the other hand, in self-compensating C-doped buffer, the electric field is distributed across gate, drain, and buffer/bulk (not shown here) regions. Below critical 2DEG density ($n_s < n_c$), the majority of space charge distributes across drain and buffer regions, leading to a suppressed peak electric field at the gate and increased breakdown voltage. However, for $n_s > n_c$, the breakdown at the gate dominates. Besides, it is also worth remembering that while the nature of inequality between n_s and n_c helps to choose a given field plate topology, n_c is a strong function of relative charge concentrations, which should affect the optimum design window and maximum achievable breakdown voltage. These are explored and discussed in detail in subsequent sections.

III. FIELD PLATE DESIGN AND BREAKDOWN VOLTAGE SCALING

The computational framework used is similar to the one used in [21] and elaborated in our earlier reports [22]–[26]. The calibration of device characteristics with experiments is presented in [22]. In order to emulate the experimental observations, the surface traps are considered at the AlGaN/SiN interface. Fig. 2 depicts the cross-section of the devices used

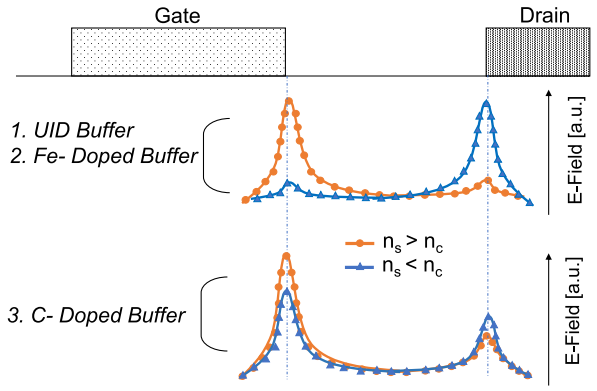

FIGURE 1. Illustration of spatial electric field distribution at breakdown in Fe-doped and C-doped buffer as a function of sheet density, as elaborated in [21]. The value of critical 2DEG density (n_c) is different for different buffer types.

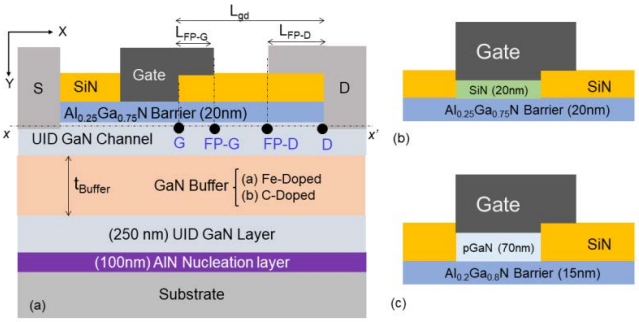

FIGURE 2. (a) Cross-sectional schematic of the Schottky HEMT device, (b) illustration of gate stack for MIS HEMT, and (c) p-GaN HEMT used for the simulation studies. Electric field/avalanche coefficients are extracted in regions - gate edge (G), gate field plate edge (FP-G), drain edge (D) and drain field plate edge (FP-D). The substrate was undoped and kept floating to match the experimental conditions and to isolate substrate-induced breakdown effects. High acceptor trap concentration of $3 \times 10^{18} cm^{-3}$ is assumed in the AlN nucleation layer and at the Substrate-AlN interface. The p-GaN layer in (c) is Mg doped with concentration of $3 \times 10^{18} cm^{-3}$. The physical device parameters used, unless specified otherwise, are: source-to-gate length ($L_{sg} = 1\mu m$), gate length ($L_g = 0.7\mu m$), gate-to-drain distance ($L_{gd} = 5\mu m$), channel thickness ($t_{Channel} = 150nm$), and buffer thickness ($t_{Buffer} = 1.5\mu m$).

for the studies. The relevant doping, trap and gate stack parameters are the same as used in earlier work [21].

For a fixed polarization charge, the surface trap density determines the 2DEG density in the channel. For a polarization charge P_1, the maximum (n_{H1}) and minimum (n_{L1}) possible values of 2DEG concentration is defined by the number of donor traps available at the AlGaN surface for a given buffer type. For instance, in the case of polarization charge P_1, the lower limit of sheet density 'n_{L1}' is obtained at a surface trap concentration of ST_{min}. Decreasing the surface charge below ST_{min} results in hole gas at the AlGaN surface as the negative polarization charge at the AlGaN surface has to be compensated. On the other hand, the upper limit of sheet density 'n_{H1}' is obtained by surface trap concentration of ST_{max}. Increasing the trap concentration beyond ST_{max}, does not result in an increase in 2DEG concentration due to Fermi level pinning at the surface. Similarly, the corresponding

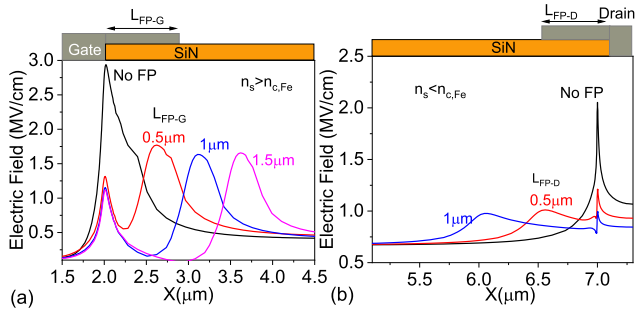

FIGURE 3. (a) For $n_s > n_{c,Fe}$, electric field distribution in channel as function of gate field plate, (b) for $n_s < n_{c,Fe}$, electric field distribution as function of drain field plate. The plots are extracted along the line xx', shown in Fig. 2(a). The plots are extracted at 50V drain bias.

2DEG concentration limits are extracted for polarization vector P_2 as given by n_{L2} and n_{H2}. The values of polarization vector P_1 (100% polarization) and P_2 (60%) polarization are chosen to study the cases of complete and partial polarization that result in 2DEG concentration in HEMT ranging from of $10^{12} cm^{-2} - 10^{13} cm^{-2}$ as observed experimentally. In these subsequent sections, we will individually study the field plate implementation corresponding to varying polarization and surface charge in HEMT for different buffer types.

A. FE-DOPED BUFFER

1) FP DESIGN

In Fe-doped buffer, for $n_s > n_{c,Fe}$, the breakdown was dominated by gate injection due to electric field peak at the gate edge, as illustrated in Fig.1. Adopting a gate field plate in this case, shifts the peak electric field away from the gate edge and at the field plate edge, as shown in Fig. 3(a). This, in turn, mitigates gate injection and improves the breakdown voltage as depicted by breakdown voltage and gate/source leakage trends shown in Fig. 4(a)-(c). On the other hand, for $n_s < n_{c,Fe}$, the depletion region extends till the drain edge, and the electric field shifts to the drain contact edge. In this case, the peak field at the drain can be relaxed by using a drain field plate, as depicted in Fig. 3(b), which in turn improves the breakdown voltage as shown in Fig. 4(d). It is to be noted that due to the difference in the distribution of depletion charges in the aforementioned cases, for the same applied drain bias, the depletion area is larger in case of Fe doped device. Therefore, the peak electric field strength and the shift due to field plate is weaker in case of Fe doped buffer with $n_s < n_{c,Fe}$ compared to $n_s > n_{c,Fe}$ as illustrated in Fig. 3.

No effect of the drain field plate was seen in the earlier case ($n_s > n_{c,Fe}$), except for higher polarization % and lower surface trap concentration, i.e., when ($n_s \sim n_{c,Fe}$) e-field was partially shared by drain edge too. On the other hand, the gate field plate does not affect the breakdown voltage in the latter case.

Another observation here is that for $n_s > n_{c,Fe}$, in the presence of the gate field plate, the additional space charge region formed below the field plate suppresses the gate

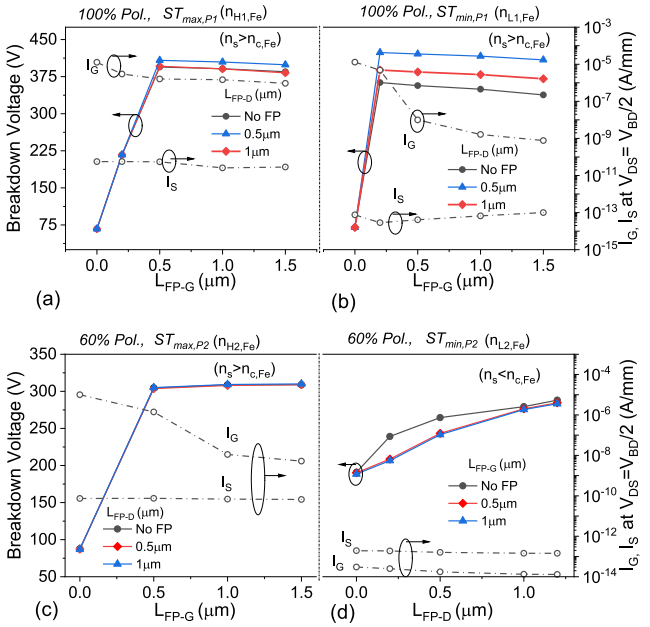

FIGURE 4. Breakdown voltage scaling (Fe-doped stack) with gate field plate in case of (a) $n_{H1,Fe}$, (b) $n_{L1,Fe}$, (c) $n_{H2,Fe}$ and with drain field plate in case of (d) $n_{L2,Fe}$. The off-state gate and source currents are extracted at V_{DS}=V_{BD}/2.

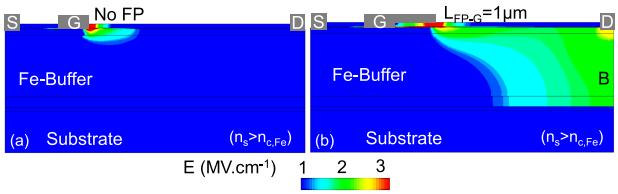

FIGURE 5. Electric field contours at breakdown for $n_s > n_{c,Fe}$ in case of (a) no field plate (b) $L_{FP-G} = 1.5\mu m$.

injection. The depletion region now extends to a farther distance from the gate towards the drain contact. As the drain bias is increased, the space-charge region expands and depletes the entire channel. Consequently, in addition to the gate and field plate edge, another peak in the electric field is observed at the drain contact edge, as shown in Fig.5. The physical location of breakdown and strength of gate injection depends upon the relative magnitude of carrier generation rates at these points and e-field strength at the gate, respectively. Source leakage was mostly insensitive to field plate design and was set by the buffer doping. Implementing a drain field plate in addition to the gate field plate may further suppress the drain field, but it does not always hold, as discussed below.

The additional drain field plate does not yield any significant improvement in breakdown voltage for cases with high surface trap concentration, as seen in Fig. 4(a) and (c), respectively. Whereas for low surface trap concentration, where the Fermi level is not pinned, further improvement with a drain field plate is observed (Fig. 4(b)). As explained earlier, Fermi level pinning caused by high surface traps

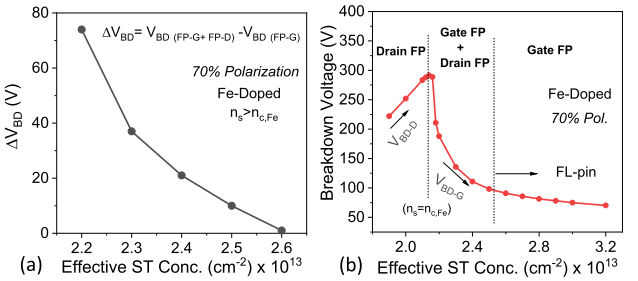

FIGURE 6. (a) The net improvement in breakdown voltage by employing a drain field plate in addition to gate field plate as a function of surface trap concentration. The gate and drain field plate lengths are $L_{FP-G} = 1.5\mu m$ and $L_{FP-D} = 2\mu m$, respectively. (b) Breakdown voltage as a function of surface traps with proposed field plate design strategies. V_{BD-D} and V_{BD-G} represent the breakdown at the drain and gate edge, respectively. The inset represents that the surface trap concentration is varied to neutralize the surface hole gas.

results in ionization of excess surface traps near the gate edge leading to a higher gate electric field. Hence, the drain field plate does not result in any further improvement in breakdown voltage. This is further verified by arbitrarily assuming 70% polarization and observed the breakdown voltage as a function of gate field plate, drain field plate and surface traps, as shown in Fig. 6(a). ΔV_{BD} denotes the net improvement in breakdown voltage by employing a drain field plate in addition to a gate field plate. It is evident that as the surface trap concentration increases, the dual field plate configuration becomes less effective. The breakdown voltage dependence as a function of surface traps is shown in Fig. 6(b) as derived earlier. The figure illustrates the three regions of interest in choosing an optimum field plate strategy.

We, therefore, establish that gate field plate can be employed in all the cases with $n_s > n_{c,Fe}$ and drain field plate to be used for $n_s < n_{c,Fe}$, as illustrated in Fig.7(a) and (b), respectively. The surface trap concentration necessary to induced 2DEG density increases with polarization to neutralize the surface hole gas. Hence, the gate electric field also increases proportionally when $n_s > n_{c,Fe}$, leading to an inverse relation of breakdown voltage with polarization. On the other hand, when $n_s < n_{c,Fe}$, the breakdown voltage improves with polarization as breakdown depends upon the rate at which the depletion region extends to the drain contact. In the case of p-GaN and MIS gate stacks, we found that the spatial field distribution in the two cases has similar dependence on 2DEG density, as shown in Fig.7(a) and (b). Hence, the field plate design rules can be applied to any HEMT irrespective of gate stack nature. However, it should be noted that the absolute values of breakdown voltage in the case of MIS and p-GaN stack differ from what has been shown for the Schottky gate, which is attributed to the difference in relative field strengths and injection rates.

2) BREAKDOWN VOLTAGE SCALING

The usual practice to increase the breakdown voltage in HEMTs is by increasing the gate to drain distance (L_{gd}) and buffer thickness (t_{Buffer}), which mitigates the electric field

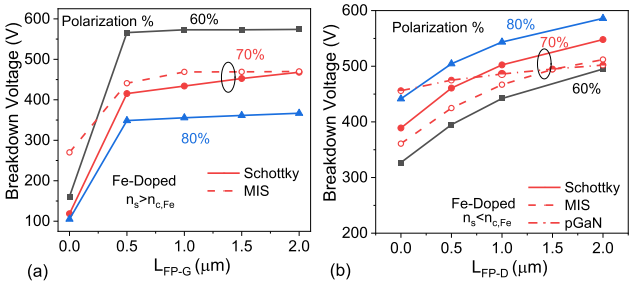

FIGURE 7. Effectiveness of gate and drain connected field plates for varying polarization in case of (a) $n_s > n_{c,Fe}$ and (b) $n_s < n_{c,Fe}$ respectively. Here $L_{gd} = 10\mu m$ and $t_{buffer} = 3\mu m$ have been used for simulations.

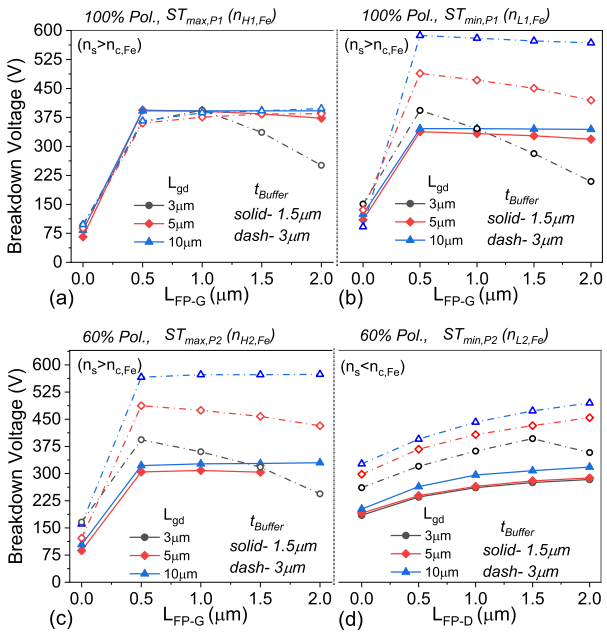

FIGURE 8. Breakdown voltage scaling with gate to drain distance and buffer thickness in case of (a) $n_{H1,Fe}$, (b) $n_{L1,Fe}$, (c) $n_{H2,Fe}$ and (d) $n_{L2,Fe}$ for Fe doped stack.

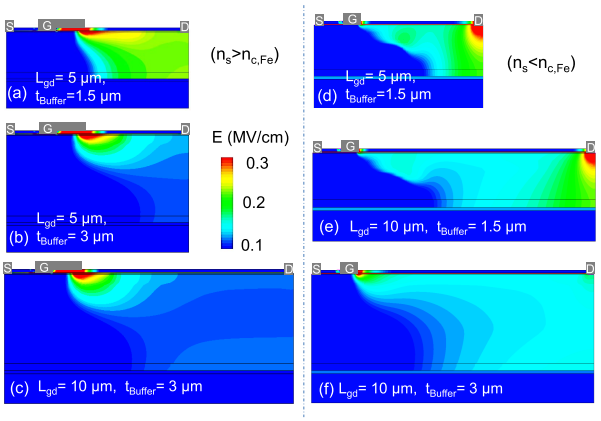

FIGURE 9. Electric field contours in case of $n_s > n_{c,Fe}$ and $n_s < n_{c,Fe}$ for Fe stack. For $n_s > n_{c,Fe}$, (a) L_{gd}=5μm, t_{Buffer}=1.5μm, (b) L_{gd}=5μm, t_{Buffer}=3μm, (c) L_{gd}=10μm, t_{Buffer}=3μm. For $n_s < n_{c,Fe}$, (d) L_{gd}=5μm, t_{Buffer}=1.5μm, (e) L_{gd}=10μm, t_{Buffer}=1.5μm, (f) L_{gd}=10μm, t_{Buffer}=3μm. The contours are extracted at 120V.

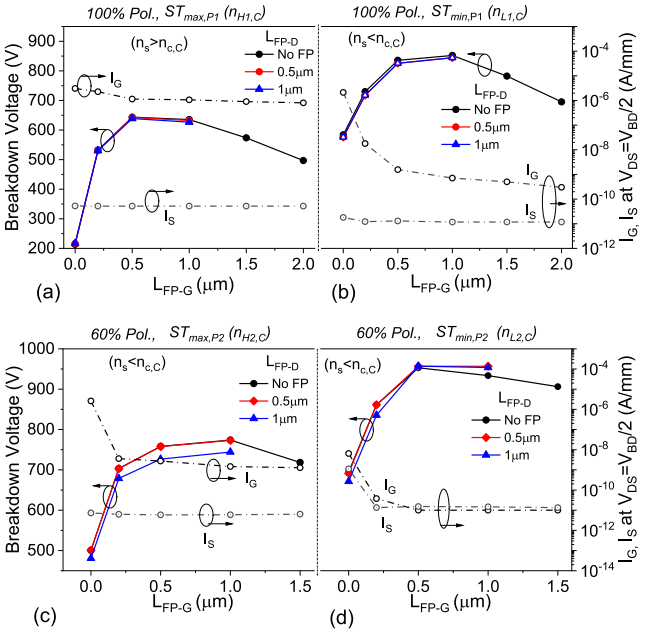

FIGURE 10. Breakdown voltage scaling (C-doped stack) with gate field plate in case of (a) $n_{H1,C}$, (b) $n_{L1,C}$, (c) $n_{H2,C}$ and (d) $n_{L2,C}$. The off-state gate and source currents are extracted at $V_{DS}=V_{BD}/2$.

localization. However, in our studies, we observed that it does not hold in all cases. For Fe doped buffer, the breakdown voltage does not scale substantially as a function of L_{gd} and t_{Buffer} if the Fermi level is pinned, as depicted in Fig. 8(a). It implies that the breakdown voltage is independent of device dimensions for maximum sheet density and instead limited by the Schottky gate leakage due to dominating gate injection. As the 2DEG density falls, the electric field peak at the gate also reduces, enabling the effect of lateral and vertical scaling in the device, as shown in Fig. 9(a)-(c). Similarly, for $n_s < n_{c,Fe}$, the vertical field at the drain is relaxed by increasing the buffer thickness. As shown in Fig. 9(d)-(e), if the breakdown is limited by the space charge below the drain region, lateral scaling does not affect the device breakdown. However, if space charge is allowed to extend vertically in the thick buffer ($3\mu m$), breakdown voltage improves in proportion to L_{gd}.

B. SELF-COMPENSATING C-DOPED BUFFER

1) FP DESIGN

For self-compensating C-Doped buffer, the breakdown voltage improves as a function of the gate field plate for the complete range of n_s, as depicted in Fig. 10(a)-(d). In the case of 100% polarization with maximum ST, as shown in Fig. 10(a), gate leakage was found to be higher and insensitive of the gate field plate. In this case, additional e-field peak at the field plate edge caused breakdown voltage improvement, while gate leakage remained insensitive due to consistent high e-field at the gate edge. Implementing a gate field plate in this case results in reduction in the peak electric field near the gate edge and also shifts the peak away. The reduced

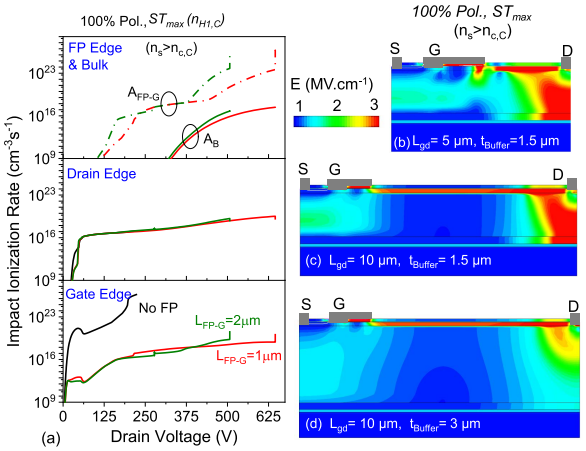

FIGURE 11. (a) Impact ionization rate for $n_s > n_{c,C}$ as a function of field plate length and breakdown voltage. Electric field at breakdown conditions contours for (b) L_{gd}=5μm, t_{Buffer}=1.5μm, (c) L_{gd}=10μm, t_{Buffer}=1.5μm, (d) L_{gd}=10μm, t_{Buffer}=3μm. Increased L_{gd} and buffer thickness relax the field distribution at gate, improving the breakdown voltage.

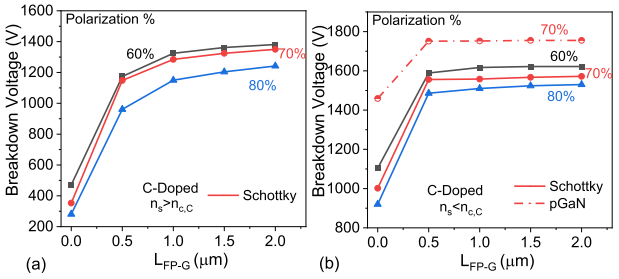

FIGURE 12. Effectiveness of gate connected field plates for varying polarization in case of (a) $n_s > n_{c,C}$ and (b) $n_s < n_{c,C}$ respectively. Here L_{gd} = 10μm and t_{buffer} = 3μm have been used for simulations.

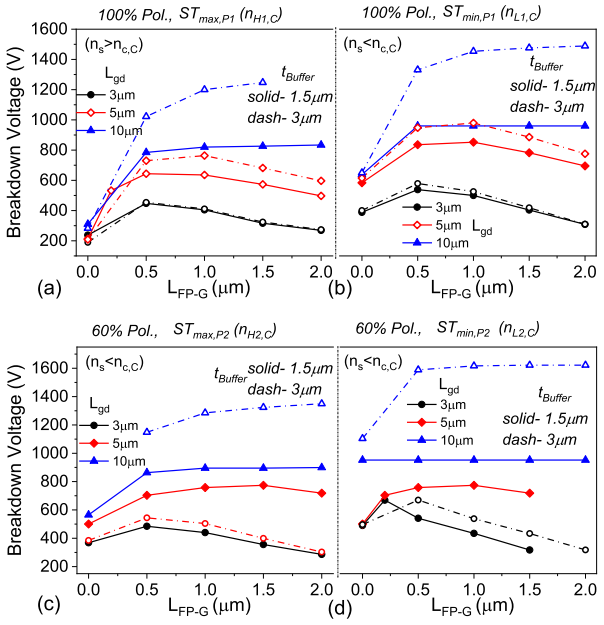

FIGURE 13. Breakdown voltage scaling with gate to drain distance and buffer thickness in case of (a) $n_{H1,C}$, (b) $n_{L1,C}$, (c) $n_{H2,C}$ and (d) $n_{L2,C}$ for C doped stack.

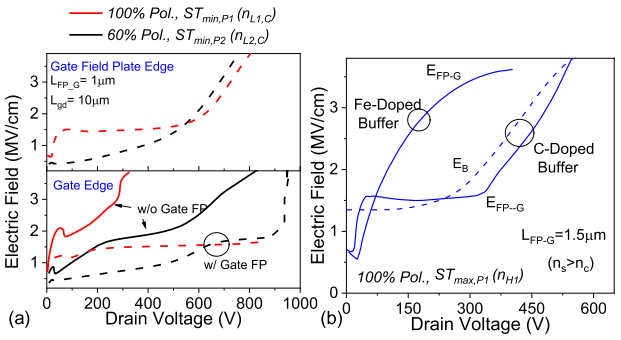

FIGURE 14. (a) Electric field versus drain voltage in case of $n_{L1,C}$ and $n_{L2,C}$ with and without gate field plate. (b) Comparison of electric field at the gate edge in case of Fe-doped buffer and C-doped buffer.

electric field lowers the impact ionization rate, improving the breakdown voltage.

For $n_s < n_{c,C}$, as shown in Fig. 10 (b)-(d), the gate leakage falls with gate field plate. In these cases, the breakdown voltage was maximum and improves with the gate field plate because of mitigated gate field component and gate injection, allowing buffer region field to grow and sustain additional drain voltage. As discussed in [21], without a field plate, before the buffer field reaches the critical field for breakdown, the gate started leaking due to the dominant peak e-field.

However, it is observed in all the cases that the breakdown voltage falls as the field plate length is increased above an optimum length. As shown in Fig. 11(a), while the reduction in impact ionization rates is observed for $L_{FP-G} = 1\mu$m when compared to without field plate, a further increase in the gate field plate initiates early impact ionization at the gate field plate edge. Since the electric field at the breakdown in C-doped buffer is primarily distributed across the GaN buffer under the drain contact, increasing field plate length above an optimum brings the field plate edge closer to the peak field region, which enhances the total field strength at the field plate corner and causes early impact ionization. Therefore, for the shorter gate to drain spacing ($L_{gd} < 5\mu m$), the breakdown voltage falls when the gate field plate length is significantly increased. However, this phenomenon can be mitigated by increasing the lateral and vertical dimensions of the device, as discussed later.

The proposed field plate design for C-doped buffer is verified for arbitrary polarization as shown in Fig.12(a) and (b) for $n_s > n_{c,C}$ and $n_s < n_{c,C}$. It can be seen that the position of the electric field peak is independent of the polarization. Hence, the gate field plate improves the breakdown voltage of the device in all cases. In the MIS and p-GaN stack case, electric field distribution was found to be similar to the Schottky gate case. Hence, the breakdown voltage improves in these gate stacks as a function of the gate field plate.

2) BREAKDOWN VOLTAGE SCALING

Fig. 13(a)-(d) shows the breakdown voltage scaling trends with drift region length and buffer thickness for different

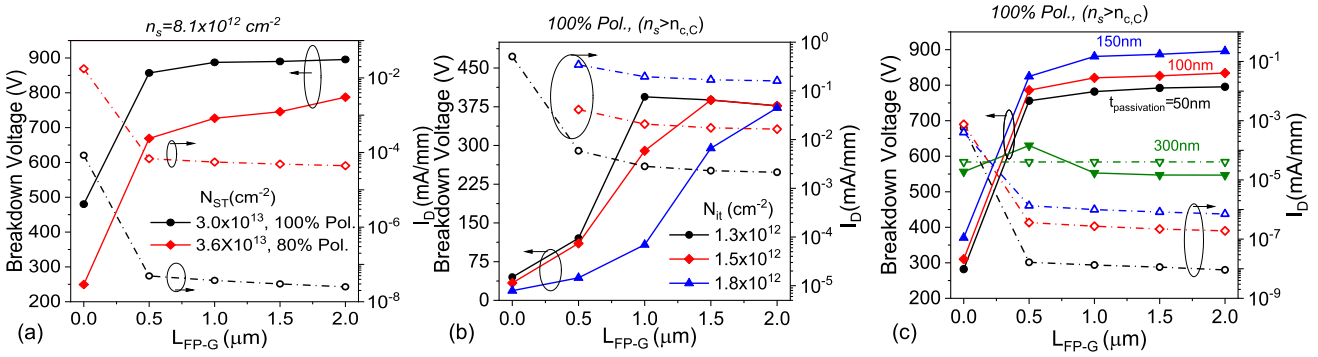

FIGURE 15. (a) For sheet density of 8.2 × $10^{12}cm^{-2}$, breakdown voltage scaling with field plate length for 100% and 80% polarization. Higher polarization charge concentration allows better breakdown voltage scaling with gate field plate. (b) Effect of interface traps at the Schottky gate (higher interface traps imply higher gate leakage) on the breakdown voltage scaling with field plate. Leaky gate contact leads to poor breakdown scaling with field plate. (c) Effect of passivation thickness on breakdown voltage scaling with field plate. The off-state drain current is extracted at V_{DS}=50V.

field plate lengths. Increasing the L_{gd} and buffer thickness effectively separates the buffer field from the gate and field plate corner field, as depicted in Fig. 11(b)-(d), which allows the implementation of longer field plates without any degradation in breakdown voltage. Thick buffers relax the space charge in the vertical direction, hence lower the vertical field at the drain edge and in the buffer. In case of the more extended gate to drain spacing, i.e., L_{gd}=10μm, no breakdown voltage scaling with field plate is observed for thin buffer (1.5μm), as depicted in Fig. 13(d). This is because the gate electric field is relatively low and becomes comparable to the drain field at the breakdown. Therefore field plate does not yield any improvement in the breakdown voltage, as shown in Fig. 14(a). However, the breakdown voltage scales as the buffer thickness is increased due to relaxation in the drain electric field. It can be concluded that below a certain buffer thickness, the field plate may not result in breakdown voltage scaling if the gate and drain fields are comparable at the breakdown.

The C-doped buffer shows significant breakdown voltage scaling with L_{gd} as well as buffer thickness for all values of n_s. Whereas, for Fe doped buffer, the improvement in breakdown voltage is not observed when 2DEG density is maximum. Comparing the electric field evolution with drain bias for C-doped and Fe-doped cases, as depicted in Fig. 14(b), increase in the electric field as a function of drain bias is found to be slower in C-doped buffer when compared to Fe-doped buffer. This is attributed to a uniform distribution of space charge into the buffer, in case of C-doping, which mitigates the peak field strength at the gate edge.

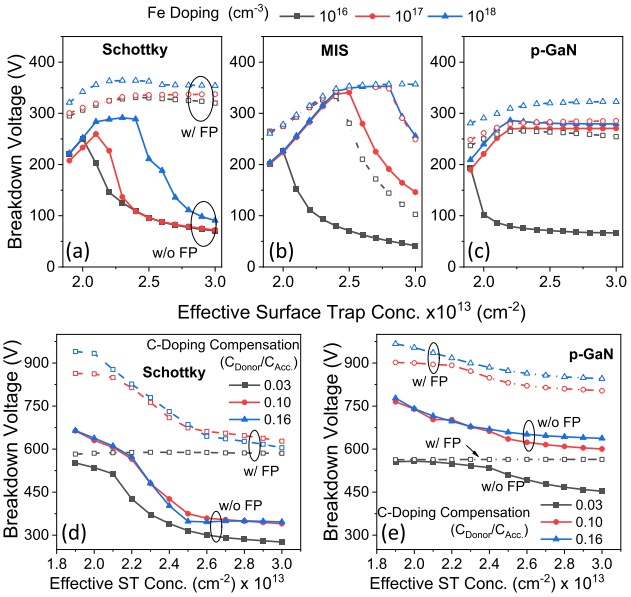

FIGURE 16. Impact of buffer doping on the breakdown voltage, in correlation with surface trap concentration for (a)–(c) Fe and (d)–(e) C doped buffers, for HEMTs with and without field plate. For this study 70% polarization in the AlGaN layer has been considered.

IV. OTHER DESIGN PARAMETERS & CHARGE SOURCES

A. POLARIZATION CHARGE AND SURFACE STATES

Earlier, we had learned how polarization charges could modify the spatial field distribution in the device. It also affects the breakdown voltage scaling with field plate, as shown in Fig. 15(a). Here breakdown voltages of two devices with the same n_s but different sets of polarization and surface charges (N_{ST}) are compared. Improved breakdown voltage scaling with a gate field plate is observed in case of complete polarization and low surface traps. Partial polarization and high surface trap concentration result in a high electric field at the gate field plate edge, and hence lower breakdown voltage is observed for a given field plate length compared to the complete polarization case. Hence, if the Fermi level at the AlGaN surface is pinned due to the high number of donor states, it leads to poor breakdown voltage scaling as a function of the field plate length.

B. SCHOTTKY GATE LEAKAGE

Based on the earlier discussions, we can establish that the gate stack plays an indispensable role in determining

the breakdown voltage of HEMT. To further validate the statement, we studied the breakdown voltage trend as a function of field plate for the Schottky gate having different interface trap concentration, as shown in Fig. 15(b). Higher donor-like states at the Schottky gate are responsible for an increase in gate leakage/injection. Fig. 15(b) shows that the breakdown voltage scaling with field plate length and effectiveness of field plate is improved when Schottky gate leakage is mitigated by lower interface trap concentration. Hence optimizing the gate stack for low leakage can significantly boost the breakdown voltage even at lower field plate lengths.

C. PASSIVATION THICKNESS

The passivation layer separates the field plate from the top AlGaN barrier surface. The breakdown voltage scaling as a function of field plate length for different passivation thickness is shown in Fig. 15(c). It can be seen that for higher passivation thickness (300nm), breakdown voltage was insensitive to field plate lengths as thicker passivation suppresses the field strength below the gate field plate and therefore does not allow electric field to effectively redistribute between gate and field plate edge. On the other hand, when the passivation thickness was reduced below a critical thickness (<150nm), the electric field strength at the field plate edge increases above the e-field at the gate edge, making the electric field re-distribution less effective. Hence a critical passivation thickness must be chosen for designing field plate. The optimum passivation thickness is also a function of dielectric constant, 2DEG density, buffer type, and gate stack, as the capacitive coupling of the field plate is dependent on these parameters.

D. BUFFER DOPING

The inter-dependency of breakdown voltage on the surface and buffer doping was discussed in earlier report [21]. It was shown that the improvement in breakdown voltage as a function of buffer doping is significantly correlated to surface trap concentration. For higher surface trap concentration, the breakdown is found to be limited by gate injection. Employing a field plate suppresses the electric field at the drain side of the gate edge. It mitigates the field-dependent non-uniform trap ionization near the gate edge. Attributed to this effect, the breakdown voltage dependency on surface traps is greatly suppressed when field plates are used. This is shown in Fig. 16(a)-(c) and (d)-(e) for Fe and C doped buffers, respectively. It should be noted that the improvement in the breakdown with field plate, for an optimum surface and buffer doping concentrations, is relatively higher in the case of Fe-doped buffer when compared with the C-doped buffer. This is attributed to the observations made in [21], that the breakdown in Fe-doped buffer is surface field limited, whereas, for C-doped buffer, a significant portion of the field is shared by the buffer.

V. CONCLUSION

The design strategy for drain and gate connected field plates in AlGaN/GaN HEMTs is developed while keeping in mind the interplay of various charge sources across AlGaN/GaN epi-stack, as discussed in [21], which was found to govern the electric field distribution across HEMT. Investigations carried out for Schottky, MIS and p-GaN gate stacks reveal that the field plate design strategy remains independent of gate design. However, the role of gate and drain field plates was found to be different in the Fe-doped buffer compared to the C-doped buffer. Unlike Si technologies, in the case of HEMTs with high (low) polarization & low (high) ST, instead of observing suppression in avalanche generation, mitigation of gate injection by shifting the peak electric field position away from gate edge was found to be the dominant cause of breakdown voltage improvement when gate field plate was adopted. However, in few other cases, particularly in C-doped buffer, widening of depletion region near the gate (high polarization & high ST) or dominance of buffer field (low polarization & low ST) was the reason for breakdown voltage improvement with a gate field plate. On the other hand, the drain field plate was found to be effective only for lower polarization % and lower surface trap concentration, only for Fe-doped buffer. A combination of gate and drain field plate further improves the breakdown voltage if the high concentration of donor states does not pin the Fermi level at the AlGaN surface. It was found that while buffer trap parameters set the upper limit of achievable breakdown voltage, the adoption of a well-designed field plate, as discussed in this work, is the only way to push the HEMT breakdown voltage close to maximum achievable. While the breakdown voltage was in general improved with field plate, its roll-off with surface/passivation trap concentration was by and large missing except C-doped buffer with high polarization %. Moreover, interface traps at the gate were detrimental to breakdown voltage, which was mitigated with the gate field plate. Only an optimum field plate design, keeping in mind various aspects discussed to mitigate gate injection, would allow a proportionate increase in breakdown voltage with increasing gate-to-drain spacing and buffer thickness.

REFERENCES

[1] Y.-F. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar, T. Wisleder, U. Mishra, and P. Parikh, "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004, doi: 10.1109/LED.2003.822667.

[2] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. DenBaars, and U. K. Mishra, "High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates," *IEEE Electron Device Lett.*, vol. 27, no. 9, pp. 713–715, Sep. 2006, doi: 10.1109/LED.2006.881020.

[3] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 161–163, Apr. 2004, doi: 10.1109/LED.2004.824845.

[4] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1515–1521, Aug. 2001, doi: 10.1109/16.936500.

[5] A. Chini, D. Buttari, R. Coffie, S. Heikman, S. Keller, and U. K. Mishra, "12 W/mm power density AlGaN/GaN HEMTs on sapphire substrate," *Electron. Lett.*, vol. 40, no. 1, pp. 73–74, Jan. 2004, doi: 10.1049/el:20040017.

[6] M. T. Hasan, T. Asano, H. Tokuda, and M. Kuzuhara, "Current collapse suppression by gate field-plate in AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1379–1381, Nov. 2013, doi: 10.1109/LED.2013.2280712.

[7] V. Kumar, G. Chen, S. Guo, B. Peres, I. Eliasevich, and I. Adesida, "Field-plated 0.25 μm gate-length AlGaN/GaN HEMTs on 6H-SiC with power density of 9.1 W/mm at 18 GHz," *Electron. Lett.*, vol. 41, no. 19, pp. 1080–1081, 2005, doi: 10.1049/el:20052051.

[8] J. Wong, K. Shinohara, A. L. Corrion, D. F. Brown, Z. Carlos, A. Williams, Y. Tang, J. F. Robinson, I. Khalaf, H. Fung, A. Schmitz, T. Oh, S. Kim, S. Chen, S. Burnham, A. Margomenos, and M. Micovic, "Novel asymmetric slant field plate technology for high-speed low-dynamic R_{on} E/D-mode GaN HEMTs," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 95–98, Jan. 2017, doi: 10.1109/LED.2016.2634528.

[9] S. Karmalkar, J. Deng, and M. S. Shur, "RESURF AlGaN/GaN HEMT for high voltage power switching," *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 373–375, Aug. 2001, doi: 10.1109/55.936347.

[10] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1825–1830, Aug. 2007, doi: 10.1109/LED.2010.2048741.

[11] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, "Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 659–661, Jul. 2010, doi: 10.1109/LED.2010.2048741.

[12] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High breakdown voltage AlGaN-GaN power-HEMT design and high current density switching behavior," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Dec. 2003, doi: 10.1109/TED.2003.819248.

[13] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, and T. Ogura, "Design and demonstration of high breakdown voltage GaN high electron mobility transistor (HEMT) using field plate structure for power electronics applications," *Jpn. J. Appl. Phys.*, vol. 43, no. 4S, p. 2239, 2004.

[14] Y.-W. Lian, Y.-S. Lin, H.-C. Lu, Y.-C. Huang, and S. S. H. Hsu, "Drain E-field manipulation in AlGaN/GaN HEMTs by Schottky extension technology," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 519–524, Feb. 2015, doi: 10.1109/TED.2014.2382558.

[15] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Design optimization of high breakdown voltage AlGaN-GaN power HEMT on an insulating substrate for $R_{ON}A - V_B$ tradeoff characteristics," *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 106–111, Jan. 2004, doi: 10.1109/TED.2004.841338.

[16] B. Liao, Q. Zhou, J. Qin, and H. Wang, "Simulation of AlGaN/GaN HEMTs' breakdown voltage enhancement using gate field-plate, source field-plate and drain field plate," *Electronics*, vol. 8, no. 4, p. 406, 2019, doi: 10.3390/electronics8040406.

[17] W. Mao, W.-B. She, C. Yang, J.-F. Zhang, X.-F. Zheng, C. Wang, and Y. Hao, "Reverse blocking characteristics and mechanisms in Schottky-drain AlGaN/GaN HEMT with a drain field plate and floating field plates," *Chin. Phys. B*, vol. 25, no. 1, Jan. 2016, Art. no. 017303, doi: 10.1088/1674-1056/25/1/017303.

[18] Y. W. Lian, Y. S. Lin, H. C. Lu, Y. C. Huang, and S. S. H. Hsu, "AlGaN/GaN HEMTs on silicon with hybrid Schottky–ohmic drain for high breakdown voltage and low leakage current," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 973–975, Jul. 2012, doi: 10.1109/LED.2012.2197171.

[19] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Influence of surface defect charge at AlGaN-GaN-HEMT upon Schottky gate leakage current and breakdown voltage," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 159–164, Feb. 2005, doi: 10.1109/TED.2004.842710.

[20] A. Soni, A. Singh, and M. Shrivastava, "Novel drain-connected field plate GaN HEMT designs for improved $V_{BD} - R_{ON}$ tradeoff and RF PA performance," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1718–1725, Apr. 2020, doi: 10.1109/TED.2020.2976636.

[21] A. Soni and M. Shrivastava, "Interplay of various charge sources in AlGaN/GaN epi-stack governing HEMT breakdown," *IEEE Trans. Electron Devices*, vol. 68, no. 5, pp. 2378–2386, May 2021.

[22] V. Joshi, S. P. Tiwari, and M. Shrivastava, "Part I: Physical insight into carbon-doping-induced delayed avalanche action in GaN buffer in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 561–569, Jan. 2019, doi: 10.1109/TED.2018.2878770.

[23] V. Joshi, S. P. Tiwari, and M. Shrivastava, "Part II: Proposals to independently engineer donor and acceptor trap concentrations in GaN buffer for ultrahigh breakdown AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 570–577, Jan. 2019, doi: 10.1109/TED.2018.2878787.

[24] V. Joshi, A. Soni, S. P. Tiwari, and M. Shrivastava, "A comprehensive computational modeling approach for AlGaN/GaN HEMTs," *IEEE Trans. Nanotechnol.*, vol. 15, no. 6, pp. 947–955, Nov. 2016, doi: 10.1109/TNANO.2016.2615645.

[25] A. Soni, S. Shikha, and M. Shrivastava, "On the role of interface states in AlGaN/GaN Schottky recessed diodes: Physical insights, performance tradeoff, and engineering guidelines," *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2569–2576, Jun. 2019, doi: 10.1109/TED.2019.2912783.

[26] A. Soni and M. Shrivastava, "Computational modelling-based device design for improved mmWave performance and linearity of GaN HEMTs," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 33–41, Dec. 2020, doi: 10.1109/JEDS.2019.2958915.

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