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Origin of electrically induced defects in monolayer MoS_2 grown by chemical vapor deposition

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Defects in MoS_2 play substantial role in determining the performance of MoS_2-based field-effect transistors. Typically, growth/synthesis process conditions determine the type and concentration of defects. Here, we show that defects are also introduced by prolonged operation of single crystal chemical vapor deposition-grown monolayer MoS_2 transistors which hinder the overall performance. Depending on the electrical stress conditions, these defects result in threshold voltage instabilities, enhanced channel conductance, improved screening of charged impurity scattering sites and possibly better thermal management in MoS_2 transistors. It turns out that a piezoelectric response in MoS_2 leads to permanent change in the material's molecular configuration thereby causing other effects like suppressed hopping transport within the channel, increased free electron concentration, prominent metal-insulator transition and reduction in channel potential with or without increasing sulfur vacancy concentration. As these defects are progressively introduced in the channel, the thermal dissipation capability of our MoS_2 transistors improved due to enhanced channel-dielectric coupling. Such variations in the device performance due to spontaneous response to high electric field trigger a need to reconsider supply voltage requirements of MoS_2-based electronic circuits for low-power logic applications.

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As the silicon transistor technology looks to transcend into the more-than-Moore era, research on 2D materials-based electronics has become substantially critical. Among 2D materials, MoS_2 is known to be ideal for ultra-low channel transistors for logic applications, owing to its favorable electronic bandgap and large effective mass. Moreover, a highly feasible synthesis process makes chemical vapor deposition (CVD)-grown MoS_2 the ideal choice of channel material in wafer-scale complementary metal-oxide-semiconductor (CMOS) electronics. In principle, a defect-free CVD MoS_2 channel offers low charge-carrier scattering, high carrier mobility and high ON-current values in transistors. While a large number of reports on CVD growth of MoS_2 have surfaced, realizing defect-free MoS_2 films has remained far-fetched primarily because of the thermodynamically-stable sulfur vacancy defects that form inadvertently during the growth process. Besides, chemical vapor deposition (CVD)-grown MoS_2 films suffer from defects of varying nature[1–4]. Point defects like single atom vacancies occur due to non-uniform vapor pressure of precursors whereas line defects like grain boundaries are a result of large nucleation density during the growth process[5,6]. Sulfur vacancies found in MoS_2 are thermodynamically more favorable and determine the polarity of operation in MoS_2-based field-effect transistors (FETs). Although thermodynamic favorability results in inadvertent introduction of sulfur vacancies, controlled growth conditions also result in desirable Mo/S vacancy concentration[7,8]. While vacancy type and concentration determine the polarity and transport mechanism in FETs[4,9], line defects impose serious performance limitations due to inter-grain charge transport[10]. Charge transport across grain boundaries and in single crystal channels has been investigated thoroughly[10–14] and is found to be affected significantly by existing defects in MoS_2. Studies on charge transport in MoS_2 suggest that charges trapped at the channel-dielectric interface act as charged impurity (CI) scattering sites and degrade carrier mobility especially at lower carrier density[10,15]. The coulomb potential posed by these scattering sites is screened out at large carrier density. However, when the Fermi level is aligned below the mobility edge, low carrier concentration fails to completely screen the coulomb scattering potential and carrier transport happens through thermally activated variable range hopping (VRH) via localized energy states lying below the conduction band[15]. Typically, when the carrier concentration is increased in a channel, these states become weakly localized due to screening and therefore fail to induce significant mobility degradation. The presence of grain boundaries and sulfur vacancies is found to increase carrier localization in the VRH regime of conduction and therefore exhibit a stronger dependence of channel conductance on temperature[10,16]. Besides defects that are intrinsic to material, defects introduced by electrical stress have been shown to raise serious material-device reliability concerns. It has been observed earlier that high and low field DC electrical stress on CVD-grown monolayer MoS_2 FETs results in loss of gate control, huge threshold voltage variation and degraded overall performance[17]. Other reports on high-field transport have presented remarkable results on avalanche breakdown, dependence of breakdown voltage on channel thickness, large current density values before permanent device breakdown and negative differential conductance due to inter-valley scattering at low-temperature[18–20]. While these reports discuss about standard breakdown and high-field phenomena found in typical semiconductors, none discuss about the nature of defects introduced in the material due to high-field transport.

In this work, impact of prolonged high-field operation of MoS_2 FETs on the defect profile and resulting perturbations in the fundamental properties of MoS_2 channel is investigated. Negative shift in threshold voltage and higher channel conductance are found to be the two major effects of a long-term electrical stress (LTES). In order to evaluate the progressive impact of electrical stress on transistor behavior and material quality, it is important to observe device characteristics before and after LTES. Therefore, the devices used during our experiments are stressed for longer durations without exhibiting permanent breakdown, unlike other reports on high-field breakdown of transistors. Low-temperature current-voltage characteristics, Raman spectroscopy and Kelvin probe force microscopy (KPFM) data are captured before and after LTES along with room temperature characteristics. While temperature variations reveal about the impact of LTES-induced defects on charge transport mechanism, Raman and KPFM analyses elucidate its possible impact on molecular configuration and work function of MoS_2, respectively. In general, LTES induces a unique piezoelectric response in MoS_2 channel and/or contact in which the molecular configuration of the material is perturbed under the effect of the electric field. Such perturbation has been identified through Raman spectroscopy, like in other reports[21], and validated using arguments on work function variations and KPFM. These perturbations, naturally, modify the defect profile and hence result in an enhanced screening of the existing CI sites. This has been validated through low-temperature transport measurements where stressed FETs exhibit enhanced screening, prominent metal-insulator transition at lower temperature and large localization lengths for the same carrier concentration in the channel. Furthermore, LTES-induced defect states are found to impact the thermal transport in our devices. Current saturation before and after stress along with current-time dynamics and low-temperature Raman spectra reveal that LTES-induced alterations in the material result in suppressed self-heating possibly due to improved thermal conductivity and/or improved channel-substrate coupling. These results clearly explain and advance our perspective on electrical stress-induced changes in MoS_2 that affect electrical and thermal transport properties, substantially. Moreover, such insights not only oblige one to reconsider device and circuit design strategies on MoS_2 but also embark us with strategies to possibly develop future thermoelectric and efficient thermal management systems with MoS_2.

Results and discussions

FETs on CVD-grown monolayer MoS_2 are fabricated in the back-gated configuration as shown in Fig. 1a. The as-fabricated back-gated transistor is shown in Fig. 1b. Raman spectra of the channel reveal ~19 cm^{-1} separation between the out-of-plane (A_{1g}) and in-plane (E_{2g}) Raman modes, Fig. 1c. This is used to verify that the channel is single-layer thick MoS_2.

Impact of LTES on transistor characteristics. As observed in our previous work[17], high-field operation results in severe loss of gate control and formation of localized regions with large conductance within the channel. However, the devices used during this work are much smaller in size along with a thicker gate dielectric layer. Therefore, a low to high field sweep is performed to identify the high-field regime (HFR) of operation in our smaller devices, as shown in Fig. 2a. It is observed that, unlike in larger devices with the same channel length where current saturation starts to occur at $V_{DS} = 10$ V[17], these devices exhibit onset of current saturation at $V_{DS} = 5$ V. Such a variation in the critical field for current saturation with channel width implies that velocity saturation is the primary mechanism behind observed saturation in our devices, and not field assisted channel pinch-off, reported elsewhere[11]. The ON and OFF state of our devices is determined by a gate voltage sweep with a low drain-to-source field. As shown in Fig. 2b, our devices exhibit n-type behavior with a threshold voltage (V_{TH}) of 0 V along with ON state at $V_{GS} = 100$ V. After determining conditions for the

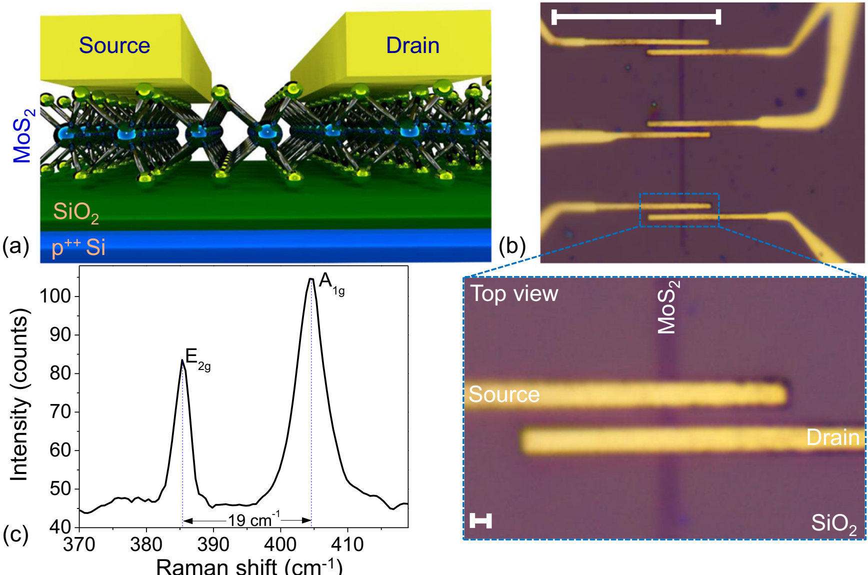

Fig. 1 Device configuration and monolayer identification. a Schematic of the back-gated transistor configuration used in this work. **b** Optical image of the top view of as-fabricated back-gated devices on MoS_2 (scale bar: 20 µm). Inset: magnified image of the bottom-most device (scale bar: 1 µm). **c** Preliminary material characterization through Raman spectra of the MoS_2 channel showing a separation of ~19 cm^{-1} between in-plane (E_{2g}) and out-of-plane (A_{1g}) modes that implies the presence of monolayer MoS_2 channel.

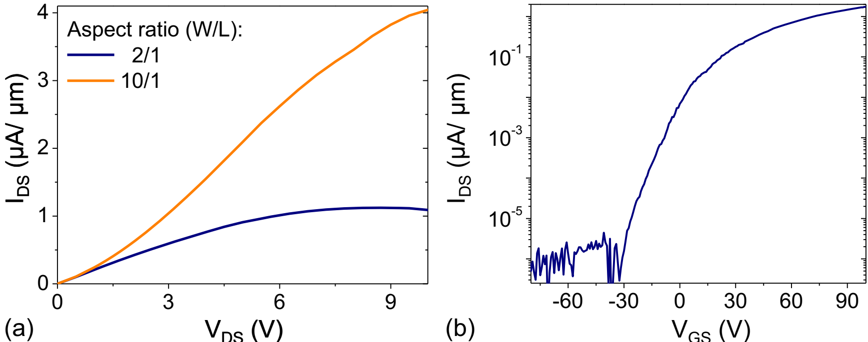

Fig. 2 Identifying different regimes of operation. a Current saturation, at $V_{GS} = 100$ V, observed in FETs with a different aspect ratio (W/L). FET with 1 µm channel width exhibits current saturation at $V_{DS} = 5$ V unlike 10 µm wide channel FET that undergoes current saturation at a much higher field, $V_{DS} = 9$ V. This observation suggests that current saturation in our devices occurs because of electron–phonon scattering-induced velocity saturation which is much more suppressed in wider devices than that in narrow channel devices. **b** Representative transfer characteristics of a monolayer MoS_2 transistor with $W/L = 2/1$ at $V_{DS} = 1$ V. All devices discussed during this work have $L_{ch} = 1$ µm and $T_{ox} = 285$ nm.

high field-ON state operation, FETs are subjected to LTES under certain electrical stress conditions for several seconds. As shown in Fig. 3a, current monotonically decreases with time and eventually saturates after 50 s of continuous operation. A monotonic decay in current is attributed to self-heating-induced enhanced electron–phonon scattering which has been validated in our previous work[17].

Impact on electrical transport. In order to determine the effect of LTES on transistor behavior, transfer characteristics are captured before and after the stress cycle, Fig. 3b, details of electrical device characterization are provided in the methods. It is observed that FET before stress, virgin device-VD, exhibits $V_{TH} = 20$ V while stressed FET, stressed device-SD, has $V_{TH} = 0$ V. This result is consistent with previously observed shift in V_{TH}[17], also verified for other devices during this work (see Supplementary Note 1 and Supplementary Fig. S1). Unlike in larger devices shown in previous work[17], gate control in these devices is intact, with current modulation (I_{ON}/I_{OFF}) as high as 10^8, after electrical stress cycle(s). It is important to note that devices fabricated in our previous work are bigger devices with $W/L = 10/1$ while these devices have a much smaller aspect ratio of 2/1. Such a difference in device dimensions is expected to introduce a large density of grain boundaries (GBs) in the channel of devices with $W/L = 10/1$ which may respond differently to the applied electrical stress. Therefore, we believe the complete loss of gate voltage in devices with huge density of GBs is attributed to an electrical stress-induced drastic change in the transport mechanism across GBs which is widely absent in smaller devices. Nonetheless, this needs to be experimentally verified as a separate work. In order to understand how the defect profile of the channel is affected by LTES, conductance (G) versus temperature (T) relationship is obtained at different overdrive gate voltages, shown in Fig. 3c, d. It is worth mentioning that obtaining conductance as function of temperature at different overdrive voltages is necessary instead of absolute gate voltage. This is done to eliminate the effect of additional carrier concentration on enhanced screening and channel conductance at the same gate

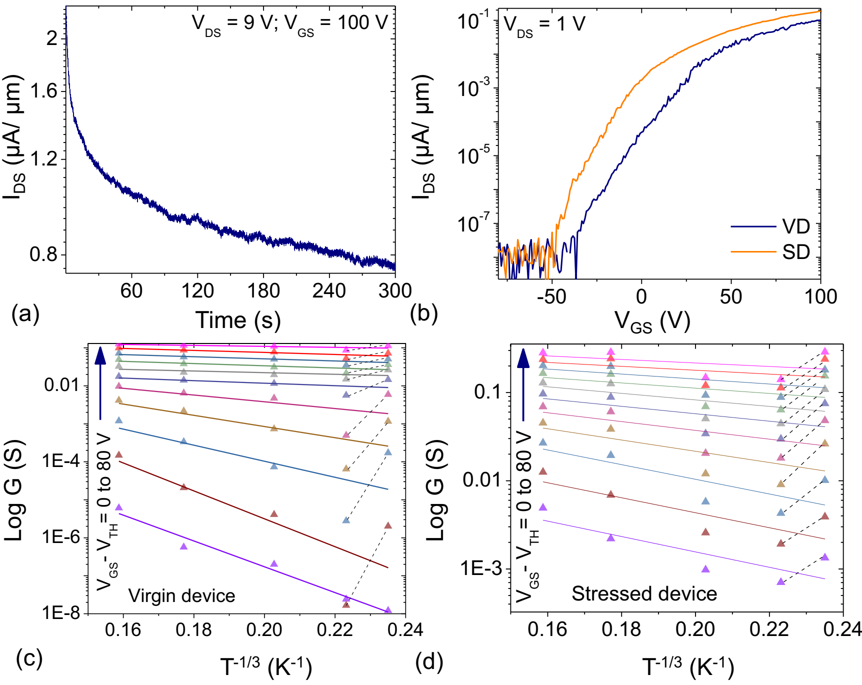

Fig. 3 Long-term electrical stress (LTES)-induced variations in the electrical properties of MoS_2. a Current versus time characteristics during a prolonged operation in the high field regime and ON state. Monotonic decay in current is attributed to self-heating and eventual establishment of thermal equilibrium between electrons and lattice which shows up as the onset of saturation after 50 s. **b** Negative shift in the threshold voltage and an increase in the overall conductance are found to be two major fallouts of LTES. Temperature dependence of conductance in **c** virgin (VD) and **d** stressed device (SD) at different gate overdrive voltage values. The temperature-dependent data from VD and SD are fitted to Mott VRH model, in Eq. (1), and are denoted by straight lines. Stress-induced defects seem to have weakened hopping transport in SD while improving the overall device conductance and resulting in enhanced screening at the same carrier concentration. Note: dotted lines represent the onset of metal-insulator transition, more prominent in SDs than that in VDs.

voltage in stressed devices. By doing this, we ensure to account only for the impact of electrically stressed channel's configuration on device conductance and charge screening phenomenon. It is well known that charge transport through MoS_2 is attributed to VRH mechanism which is given as follows[11,14]:

$$G = G_0 e^{\left(-\frac{T_0}{T}\right)^{1/3}} \tag{1}$$

Where

$$T_0 = 13.8/k\xi^2 D(E) \tag{2}$$

is a characteristic temperature determined by $k =$ Boltzmann constant, $\xi =$ localization length and $D(E) =$ density of trap states.

From Eq. (1), it is clear that the slope of G versus $T^{-1/3}$ is T_0 which in turn can be used to calculate the localization length (ξ) from Eq. (2). The larger the value of ξ, weaker is the localization of charge carriers which implies weaker hopping transport, considering constant density of states in the channel without additional dopants, and hence show up as weaker temperature dependence or smaller T_0.

As shown in Fig. 3c, temperature dependence of conductance of a virgin device weakens with increasing gate voltage. This is attributed to enhanced screening and transport through conduction band at higher gate voltages due to which carriers are largely delocalized and do not experience significant scattering due to CI sites. In SD, weaker temperature dependence at lower gate voltage is observed as shown in Fig. 3d. Moreover, SD exhibits 3–2 orders of magnitude higher conductance at the same gate voltage than VD. While weaker temperature dependence implies enhanced screening of CI scattering sites offered by the channel-dielectric interface, higher overall conductance values are not trivial to contemplate, though consistent with our previous study[17].

Moreover, in the lower temperature range ($T^{-1/3} \geq 0.22$) of Fig. 3, conductance decreases as a function of temperature[22] for both VDs and SDs. This metallic behavior is more pronounced in SDs than VDs. Poorer metallic behavior in VDs, at higher gate voltages, is possibly a result of the poor quality of pristine channel material. However, a more pronounced metal-insulator transition (MIT) in SDs, implies poorer phonon-assisted and thermally activated hopping transport in the channel[22]. Such an observation suggests that transport in VDs is strongly limited by SV-assisted hopping transport while a strong metallic character for the complete range of gate bias in SDs implies weaker hopping transport, possibly because of the anticipated piezoelectric response of MoS_2. Furthermore, the MIT behavior is strongly tuned by gate bias in VDs than in SDs, as indicated by the slopes of dotted lines in Fig. 3. Typically, gate voltage tunability of transport in the channel suggests how effectively the scattering sites are screened out by increasing carrier concentration in the channel with increasing gate voltage. A poorer dependence of screening on gate voltage and a strong metallic behavior in the low-temperature regime are fallouts of stress-induced enhanced intrinsic screening in the channel which can only be mildly further tuned by the gate voltage. This has also been identified as the result of stress-induced defects in MoS_2, as discussed later in the text.

We find that the impact of long-term electrical stress on the transfer characteristics of large area (W/L: 10/1) devices is temperature dependent. As shown in Supplementary Fig. S6, devices stressed under high-field regime and $T = 150$ and 77 K exhibit positive voltage shifts, unlike those stressed at room temperature. However, devices stressed for different time duration exhibit similar monotonically decaying current versus time behavior, Supplementary Fig. S7. Furthermore, the impact of shorter electrical stress

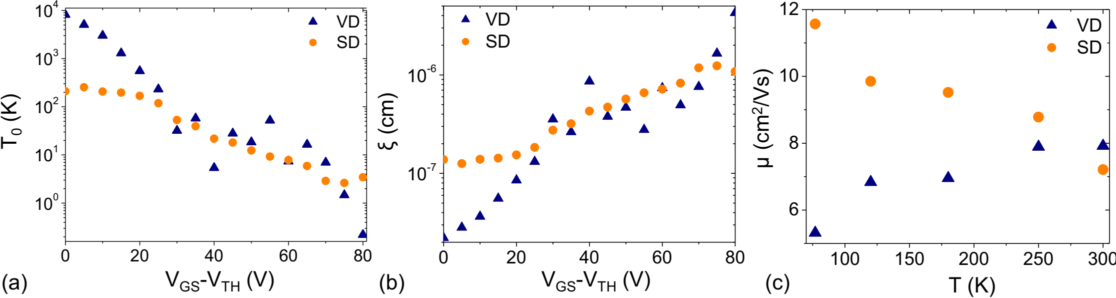

Fig. 4 Effect of LTES on screening, carrier localization and carrier mobility in the channel. a The characteristic temperature is plotted against gate overdrive voltage. A typical drop in T_0 with overdrive voltage is observed. However, T_0 values for SD are more than an order smaller than those for VD. This implies weaker temperature dependence of G which means LTES results in weaker hopping transport in MoS_2. **b** Localization length is plotted as a function of gate overdrive voltage. As a result of LTES, carriers are found to be weakly localized which is inferred from the observed increase in the localization length in SD. **c** Field-effect mobility is shown as a function of temperature for virgin and stressed device. SD exhibit much higher mobility at low temperature which suggests that CI scattering is suppressed as a result of LTES. Moreover, high-temperature mobility remains mostly unaffected.

events at the same drain-to-source field and gate bias result in a negative shift in threshold voltage as well as enhanced channel conductance, as observed in all our devices during this work. As shown in Supplementary Fig. S8a–f, stress events of different time durations: $t = 5$ ms, 10 ms, 50 ms, 5 s, 10 s and 30 s at $V_{DS} = 10$ V and $V_{GS} = 100$ V; result in a negative shift in threshold voltage, higher ON state current along with higher 2-terminal channel conductance, Supplementary Fig. S9a–f. It is important to note that, duration of the stress event does not seem to have had any impact. Moreover, multiple levels of current have been achieved during stress as can be seen from Supplementary Figs. S6–S9 and other observations in this manuscript, besides our previous work[17]. None of these conditions of current appear to strongly impact the stress-induced conductance variation. Therefore, we can say that, temperature and electric field during the stress contribute to the observed "piezoelectric response", we have not been able to identify a threshold condition that does not result in such a change. Apart from low-temperature stress, all other stress conditions have resulted in enhanced device conductance. We believe, all these factors have a combined effect on the overall material re-configuration during stress and need a more comprehensive, dedicated set of experiments to be performed, potentially a subsequent work on the same topic. Besides, we find that electrical stress with negative polarity, Supplementary Fig. S10a, results in a smaller device current and more positive threshold voltage, shown in Supplementary Fig. S10b, unlike a stress cycle with positive polarity. Therefore, an electrical stress of opposite polarity could be one of the ways by which the impact of long-term electrical stress could be reversed, at least to some extent. Moreover, we find that a stressed device exhibits reasonably robust transfer characteristics, as shown in Supplementary Fig. S11, at least till 2 h after the stress event.

In order to qualitatively understand the effect of stress on carrier localization in the channel, T_0 and ξ for VD and SD are plotted as functions of overdrive voltage, Fig. 4a, b. Using Eqs. (1) and (2) and experimental data on conductance versus temperature, T_0 and ξ are calculated. As expected, the characteristic temperature, T_0, and localization length are strong functions of gate voltage as increased carrier screening, due to large carrier concentration at higher gate voltage, tend to delocalize charge carriers and weaken hopping transport. It is observed that SD exhibits ~97 % decrease in the temperature dependence of G than VD at $V_{GS}–V_{TH} = 0$ V, Fig. 4a. Moreover, from Fig. 4b it is clear that LTES leads to ~2 orders of magnitude increase in the localization length at zero gate overdrive voltage. At high gate overdrive voltage, SD behaves like VD by exhibiting weaker temperature dependence of conductance and carrier delocalization, Fig. 4a, b. These results imply that LTES on MoS_2 results in a certain change in the channel that leads to substantial delocalization of charge carriers due to which transport near the subthreshold region of operation follows weak VRH. This is consistent with the earlier observed increase in channel conductance and a negative shift in the threshold voltage[16]. Interestingly, this has been observed in another device that is stressed at different stress conditions, as shown in Supplementary Fig. S2. In this case, the device is stressed while it is in the near-threshold regime of operation ($V_{GS} = -10$ V) and it is found that the current does not decay monotonically with time, as discussed in our previous work, but remains constant throughout the stress cycle, see Supplementary Fig. S1e, g. However, such a stress too results in a significant negative shift in threshold voltage, as shown in Supplementary Fig. S1f, h. Also, it is observed that a relatively small change in T_0 is observed for devices stressed in the near-threshold regime, Supplementary Fig. S2. It appears that the impact on transistor behavior could be stress-dependent and is discussed later in the text.

Such an improvement in the charge screening capability of MoS_2 channel can only occur if the defect creation process results in excess free electrons in the channel. Excess free electrons in the channel are possible if the concentration of sulfur vacancy increases. Therefore, it is reasonable to anticipate the formation of sulfur vacancies upon high-field LTES operation of MoS_2 FETs. The fact that our samples are not subjected to any kind of external material-related process and only electrical stress is applied to the material, implies that high-field-induced avalanche-like soft breakdown of the material may have occurred due to LTES which could possibly have triggered disruption of Mo-S bonds to induce additional sulfur vacancies leaving behind S atoms at non-lattice sites. Such an effect is expected to cause severe mobility degradation, especially at low temperature, due to enhanced scattering from unbonded S atoms that act as CI scattering sites. Interestingly, it is observed that stressed devices do not experience mobility degradation and exhibit similar mobility values at room temperature, Fig. 4c. Contrary to the expected drop in low-temperature mobility due to increased CI scattering by unbonded S atoms, it is found that low-temperature mobility actually improves after stress, see Fig. 4c. Mobility versus temperature trends clearly imply that stressed devices do not suffer from enhanced CI scattering-induced mobility degradation. This result does not support the possibility of LTES-induced formation of sulfur vacancies. Moreover, sulfur vacancies (SVs) are known to result in enhanced localization of charge carriers thereby resulting in stronger dependence of conductance on temperature[16]. This is in contrast with the observed weaker temperature dependence of G after stress, already shown in Fig. 3a, b. Hence, the hypothesis that

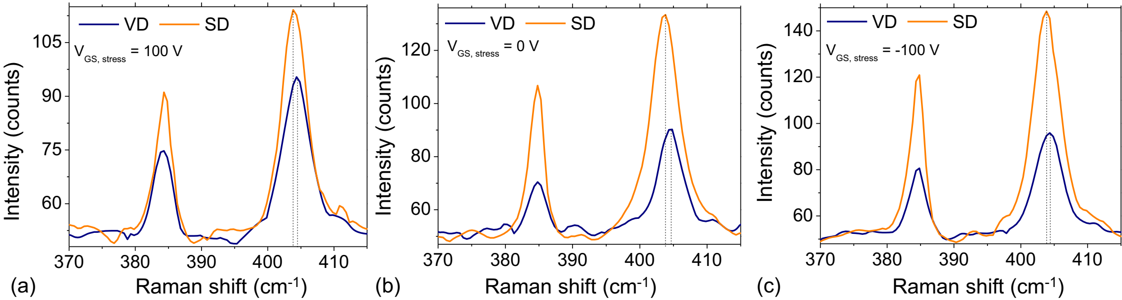

Fig. 5 Impact of LTES on Raman spectra of MoS_2. Red shift is observed in the out-of-plane A_{1g} mode consistently for all three regimes of device operation —**a** ON state, **b** near-threshold region and **c** OFF state for stress voltage V_{DS} = 9 V. Along with red shift in A_{1g} mode, substantial increase in the Raman intensity is also observed which implies that stressed MoS_2 exhibits stronger polarizability.

additional SVs form in MoS_2 after a prolonged high-field operation of FETs turns out to be invalid. It appears that LTES-induced defects are similar to SVs as far as their effect on V_{TH} is concerned but are of different nature when it comes to influencing the charge transport mechanism in the channel. While SVs help in localizing charge carriers in the channel and result in a stronger temperature-dependent hopping mechanism[16], LTES-induced defects tend to delocalize charge carriers thereby weakening the hopping mechanism and making G a relatively passive function of temperature.

Although the impact of LTES-induced defects on the electrical properties of MoS_2 can be fairly visualized through arguments based on electrical transport presented above, the physical picture at the atomic scale is still not clear. In order to decipher the physical meaning of LTES-induced defects, its impact on crystal structure is analyzed through changes observed in the Raman active modes of MoS_2.

Material perturbations due to LTES. In Fig. 5, Raman spectra of monolayer MoS_2 are shown which are captured before and after the application of LTES at $V_{DS} = 9$ V. It is important to note that Raman data has been calibrated with respect to the silicon Raman peak observed at 520.7 cm^{-1}, details of Raman setup and calibration are provided in methods. It is observed that the out-of-plane mode A_{1g} of stressed MoS_2 red-shifts by ~0.6 cm^{-1} from its unstressed counterpart, Fig. 5a. A similar red shift is observed when the channel is stressed at $V_{DS} = 9$ V near the threshold region with $V_{GS} = 0$ V and in the OFF state with $V_{GS} = -100$ V, Fig. 5b, c, respectively. The in-plane E_{2g} mode is also found to have red shifted but this result has not been very consistent for different devices, Fig. 5a. Such a shift in the A_{1g} mode implies lower energy of out-of-plane phonon vibrations. A classical analysis of Raman signal is typically performed by treating the molecule as a mass-spring model[21] where the phonon energy is a function of frequency and this frequency of oscillation is found to be a function of spring constant and total mass of the system—Hooke's law, as shown below:

$$E_{phonon} = \hbar\omega \quad (3)$$

$$\omega = \sqrt{\frac{k}{m}} \quad (4)$$

Where, E_{phonon} = energy of phonon mode, $\hbar$ = reduced Plank's constant, ω = frequency of phonon vibration, k = spring/force constant or restoration force and m = mass of the system.

A direct analogy between spring-mass model and MoS_2 molecule suggests that Mo-S covalent bond, which holds the molecule together, acts as a spring between atoms of different masses. Any outward vibration in the crystal is followed by a restoration force applied by the bond in order to keep the molecule intact. Any change in the restoration force and/or the total mass of the system results in a different frequency of vibration, Eq. (4). And a modified frequency of oscillation leads to a change in the energy of the phonon vibration. In case of electrically stressed MoS_2, the energy of the out-of-plane mode, and that of in-plane mode in some cases like Fig. 5b, c, is observed to have reduced by 0.06 meV. This decrease in phonon energy must be a result of the change in the frequency of phonon vibration, 0.5 cm^{-1} observed in Raman spectra, which in turn depends on the spring constant and mass of the system i.e. bond strength and mass of atoms respectively. Assuming that the mass of Mo and S atoms remains unchanged before and after the stress and putting the above argument in perspective along with Eqs. (3) and (4), it is argued that a prolonged DC operation or LTES on MoS_2 FET reduces the effective spring constant/restoration force of Mo-S bond which eventually results in red shift in the energy of phonon mode(s). Smaller restoration force implies a more stretched-out/weaker Mo-S bond. It is interesting to note that the Raman spectra of stressed MoS_2, shown in Fig. 5a–c (orange curve), contain Raman characteristic peaks with greater intensity than those observed in the spectra of unstressed MoS_2 (blue curve). Intensity of the Raman signal is a function of change in polarizability of the molecule and intensity of incident laser[23], as shown below:

$$I_{scattered} \propto |P \cdot E_0|^2 = |(d\alpha/dq_i)_0|^2 I_0^2 \quad (5)$$

Where $I_{scattered}$ = intensity of Raman signal, P = polarizability of the molecule and E_0 = electric field amplitude of incident laser which is proportional to the square of incident laser intensity (I_0).

As the laser intensity is kept constant during all experiments, the only way the intensity of Raman peaks may increase after electrical stress is an increase in the polarizability of MoS_2 molecule. Typically, it becomes relatively easier to alter the electron cloud or polarize a molecule if the electron cloud is being weakly shared by the constituent atoms. Weaker sharing of electron cloud occurs due to a reduction in the bond strength of the molecule. Therefore, an increase in polarizability, is directly linked with a reduction in bond strength which in turn means an increase in the bond length of covalent molecules. As a result, an increase in the intensity of Raman signal due to LTES implies that electron cloud of MoS_2 molecule is indeed perturbed for which weaker/elongated Mo-S bonds, present in electrically stressed MoS_2 channel, are found responsible.

Large FWHM in D2 and D3 could be a result of increased local density of SVs. These SVs may alter the effective mass of the mass-spring model analogous to the MoS_2 molecule and result in red shift in the A_{1g} mode frequency. However, the FWHM for D1, device stressed in the ON state, remains similar to that of virgin channel along with higher intensity and red shift in the A_{1g} mode. Moreover, poor hopping transport in the device stressed

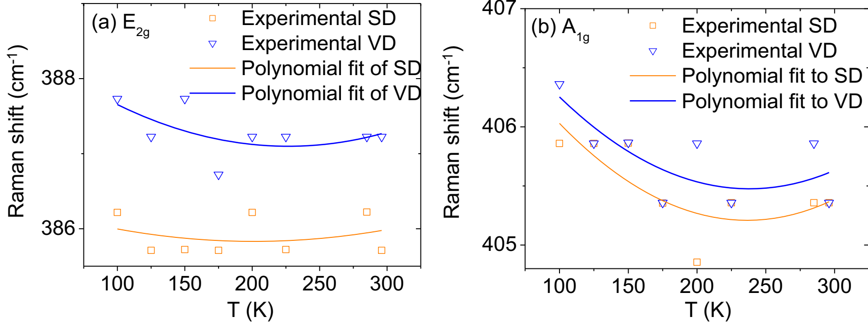

Fig. 6 Temperature coefficient of Raman modes. Temperature-dependent Raman shift of the **a** in-plane E_{2g} and **b** out-of-plane A_{1g} modes of virgin (VD) and stressed (SD) CVD monolayer MoS_2 channel. Polynomial fit to the experimental data, shown here, is used to extract the first-order temperature coefficient and Raman shift at absolute zero temperature for both the characteristic modes of monolayer MoS_2. Discussed, in detail, in Supplementary Note 4.

during ON state suggests no increase in the SV concentration. These three observations imply that (i) when the device is stressed in the ON state, a piezoelectric response kicks in which results in bond stretching throughout the channel, in line with previous observations[21]; (ii) when it is stressed in the OFF, subthreshold and threshold regime of operation, piezoelectric response triggers at the contact which in turn results in either subsequent piezoelectric effect in the channel or increase in the SV concentration due to soft breakdown or both. The stress-dependent impact on the device has been addressed later in the text.

Nonetheless, this classical analysis of the Raman spectra of stressed and unstressed MoS_2 channel suggests that electrical stress results in a permanent stretch of the Mo-S bond which essentially converges with the concept of piezoelectricity. It is important to note that a similar observation of electric field-induced red shift in A_{1g} mode of MoS_2 has been reported earlier[21]; however, a discussion on its impact on channel properties is missing. Similarly, although piezoelectricity in MoS_2 has been known since 2014[24] after which other reports surfaced[25,26] but none of these reports discuss about the impact of piezoelectricity on electrical and thermal properties of MoS_2. The stretched Mo-S bonds are, essentially, defects that result from such a piezoelectric response.

It is important to realize that piezoelectric effect in a material occurs at the same electric field. Therefore, during OFF state, threshold regime and subthreshold regime the channel should not undergo a piezoelectric change because most of the voltage drops across one of the contacts. It is possible that during OFF state, threshold and subthreshold regime, the Mo-S bonds beneath that contact get stretched owing to the piezoelectric effect at the contact. This would also increase the overall conductance and lower the threshold voltage of the stressed device. Moreover, consistent red shift in the Raman A_{1g} mode of the channel suggests that the out-of-plane Mo-S bonds in the channel do get stretched which could be a result of either subsequent piezoelectric effect in the channel[21] or increase in the electron concentration due to higher SV concentration, manifesting as wider FWHM of Raman modes for these devices and stronger temperature dependence of conductance in Supplementary Fig. S2. We believe, in the ON state the channel and contact both exhibit a piezoelectric response whereas, in the "low-current" scenario the contacts exhibit stronger piezoelectricity which in turn results in either piezoelectric response of the channel[21] or soft breakdown-induced SVs or both. Such a stress-dependent behavior is however not understood properly and requires more investigations in terms of drain-to-source field and gate voltage. Nonetheless, from Fig. 2, Supplementary Figs. S1 and S2 and Supplementary Note 2, it is clear that, a prolonged transistor operation results in defects in the channel that result in significant carrier delocalization and enhanced screening of CI even at similar carrier concentration which in one case (ON state) is a result of piezoelectric response in the channel and contacts, while in another case (OFF, threshold or subthreshold) is a result of initial piezoelectric response at one of the contacts followed by subsequent piezoelectricity in the channel or soft breakdown-induced SVs or both, as discussed earlier.

It is observed that Raman data at multiple locations in the stressed channel exhibit a lower frequency of the A_{1g} mode than that in a virgin channel, Supplementary Fig. S12. This is consistent with the observations made in smaller devices and in other reports. However, the intensities vary with the position which could be a result of grain boundaries within the channel and therefore should not be considered for the bond stretching explanation used for smaller devices. Although Raman spectroscopy fails to determine the exact bond length, we have used it for qualitative analysis and comparison with the data from a virgin device.

Migration of atomic species under the effect of electric field is a common phenomenon in MoS_2. It is possible that species like metal ions get incorporated into the channel[27] during electrical stress and result in increased doping in the channel. While temperature-dependent mobility does not suggest such an effect, one cannot be sure about the presence of such species unless direct observation is made[27]. We believe the observed variation in the channel conductance is a combined effect of bond stretching and other atomic species, if present.

We also perform temperature-dependent Raman measurements, Supplementary Note 4 and Supplementary Fig. S3, that too suggest a similar deviation from the equilibrium crystal structure of the virgin channel. As shown in Fig. 6, both the characteristic modes, E_{2g} and A_{1g}, of virgin (VD) and stressed (SD) MoS_2 channel are presented as functions of temperature. They are found to be non-linear functions of temperature, as discussed in few other reports[28,29]. A polynomial fit to the experimental data, discussed in Supplementary Note 4, is obtained in Fig. 6. The fitted curve is then used to extract the first- (χ_1) and second-order (χ_2) temperature coefficients of both the Raman modes along with their Raman shift values for absolute zero temperature (ω_0), shown in Table 1. ω_0 for the out-of-plane and in-plane modes is found to have reduced from $388.88 \pm 1.12\ cm^{-1}$ and $407.79 \pm 0.99\ cm^{-1}$ to $386.48 \pm 1.06\ cm^{-1}$ and $407.67 \pm 0.93\ cm^{-1}$, respectively, upon LTES. This red shift in the Raman modes for absolute zero temperature implies that electrically stressed MoS_2 exhibits lower Raman mode energies than virgin MoS_2 channel and therefore suggests possible permanent weakening of Mo-S bonds upon LTES, as pointed out by previous discussions. We also observe significant reduction in the first-order temperature coefficient (χ_1) of the in-

Table 1 Temperature coefficients of Raman modes.

	E_{2g}			A_{1g}		
	χ_1	χ_2	ω_0	χ_1	χ_2	ω_0
VD	−0.015 ± 0.019	3.4e-5 ± 2.9e-5	388.88 ± 1.12	−0.019 ± 0.01	4.08e-5 ± 2.5e-5	407.79 ± 0.99
SD	−0.0066 ± 0.011	1.6e-5 ± 2.78e-5	386.48 ± 1.06	−0.021 ± 0.01	4.41e-5 ± 2.5e-5	407.67 ± 0.93

First- and second-order temperature coefficients along with the absolute zero Raman shift value for both the Raman modes before (VD) and after (SD) electrical stress are extracted from Fig. 6 using the polynomial equation discussed in Supplementary Note 4.

plane mode (E_{2g}) along with marginally reduced χ_1 for the out-of-plane mode. χ_1 for E_{2g} (A_{1g}) mode reduces from −0.015 to −0.006 (−0.019 to −0.02) cm^{-1}/K upon LTES. The values of χ_1 for both the modes of virgin channel are close to other reports discussed elsewhere[28,29]. These observations on the first-order temperature coefficients of Raman modes find relevance while studying the heat dissipation properties of our devices and hence are discussed later in the text. Significant variation in the Raman data as a function of temperature could result in false fitting of the data. However, it is important to note that fitting is performed using the same method for both virgin and stressed devices. Therefore, a relative analysis is still reliable. Moreover, the first-order temperature coefficients for virgin devices are close to values reported earlier[28,29], which validates the reliability of the method used for fitting.

It is interesting to note that, although, LTES-induced defects are not exactly SV defects but may play a similar role in shifting the threshold voltage of our devices. Moreover, unlike SVs, LTES-induced defects can potentially suppress the effect of carrier localization by screening the CI potential offered by channel-dielectric interface, as discussed in the subsequent text.

It is believed that electrons from the d-orbital of Mo atoms take part in the n-type current conduction, typically observed in MoS_2[30]. In case of defect-free MoS_2, these d-orbital electrons are not available for conduction because of complete sharing of electrons between Mo and S atoms[31]. When SVs are introduced, depending on the SV concentration, d-orbital electrons of Mo become relatively free to conduct and result in a significant n-type current. Moreover, it is observed that passivation of SVs leads to a positive shift in threshold voltage which validates the role of SVs in determining the threshold for channel conduction. Intuitively, when Mo-S bond is stretched, the Coulombic force of the highly electronegative S atom on shared d-orbital electrons of Mo weakens which results in the easy availability of electrons for conduction when compared with MoS_2 with unstretched bonds. In other words, LTES on MoS_2 channel leads to a weaker Mo-S bond due to which d-orbital electrons become relatively free, unlike in unstressed MoS_2 channel with a stronger Mo-S bond. Naturally, such a change in the electron cloud distribution around Mo should result in an increase in the average channel potential. This is observed in Fig. 7 in which KPFM scans of stressed and unstressed MoS_2 channel are compared. The details of KPFM measurements are provided in Supplementary Note 2. Three different devices are stressed at the same drain-to-source voltage, i.e., $V_{DS} = 9$ V but under different states of operation—$V_{GS} = 100$ V (D1—ON state), 0 V (D2—near-threshold regime) and −100 V (D3—OFF state), see Fig. 7a–f. The features observed in the stressed devices are the fallout of the electrical stress itself and therefore need further investigations to uncover the cause of these features. Details of KPFM measurement and extraction of channel potential are discussed in Supplementary Note 4 and Supplementary Figs. S13–S18. Here, we assume that metal contacts have the lowest potential present on the sample and all other surfaces on the sample, in principle, are at a higher potential than metal contacts. Therefore, instead of comparing the absolute values of the potential of MoS_2 before and after stress, difference between channel and metal potential for virgin devices is compared with that for stressed devices. Such an approach eliminates the effect of inconsistencies observed during KPFM measurements. Following this approach, it is observed that, irrespective of the state of operation, the difference between average metal and channel potential is lower in case of stressed channel than that for virgin/unstressed channel, Fig. 7g. This result is found to be consistent with the observed stress-induced enhancement in channel conductance, discussed in our previous work[17]. Stressed channel with lower potential should, in principle, experience enhanced screening of CI sites and weaker hopping transport which has been shown earlier in Figs. 2 and 3. Therefore, it is validated that LTES on MoS_2 results in unique defects which are essentially weaker Mo-S bonds that not only result in excess free electrons in the channel, like SVs, but also weaken hopping transport, unlike SVs, which is otherwise a prominent transport mechanism in MoS_2. Besides, it is found that weaker Mo-S bonds result in non-zero density of states (DOS) in the forbidden energy bandgap of MoS_2, shown in Supplementary Fig. S4. As discussed in Supplementary Note 5, the midgap states may result in metal Fermi level to pin farther from the conduction band minimum which results in a negative shift in the threshold voltage observed in our devices. The simulation details and further discussion on the introduction of midgap states due to weaker Mo-S bonds are presented in Supplementary Note 5. It is important to note that the simulation of bandstructure of MoS_2 with weaker Mo-S bonds is performed arbitrarily as a proof of concept to validate the possibility of the occurrence of midgap states closer below the conduction band minimum that pins the Fermi level at lower energy and eventually leads to the lower threshold voltage. A comprehensive study correlating electric stress and bond strength is an interesting topic to pursue but has not been discussed in this manuscript anymore.

LTES-induced variations in thermal transport. Apart from its impact on electrical transport properties of MoS_2 channel, it is found that a prolonged electrical stress also affects thermal transport in our MoS_2 transistors. It is observed that onset of current saturation in VD occurs at $V_{DS} = 5$ V. However, the same device exhibits current saturation at $V_{DS} = 7.5$ V after an LTES cycle for 300 s, Fig. 8a.

It has been discussed earlier that current saturation in our devices is a result of velocity saturation that occurs at a critical electric field. Velocity saturation is a high-field phenomenon that occurs due to enhanced electron–phonon scattering beyond a critical field which prevents charge carriers from attaining higher kinetic energy[32]. Higher critical field of SD, observed in Fig. 8a, implies that the phonon scattering-induced velocity saturation occurs at a higher electric field. This clearly suggests that a stressed channel is able to dissipate heat more efficiently than when it is unstressed. Another evidence of LTES-induced perturbation in the thermal transport properties of MoS_2 channel is shown in Fig. 8b. It is observed that the current saturates after 50 s of continuous operation in the high-field regime of operation. The monotonic decay in current with current decay time constant

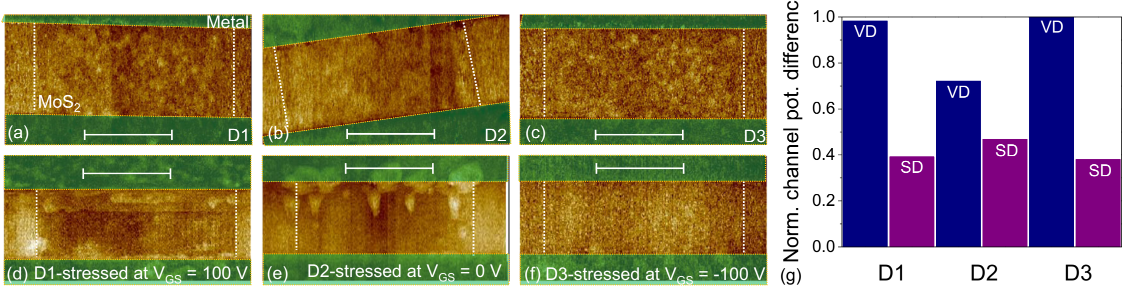

Fig. 7 Impact of LTES at different gate voltages on channel potential. a–c KPFM scans of three different VDs which are eventually stressed at $V_{DS} = 9$ V different regimes of operation—**d** ON state, **e** near-threshold region and **f** OFF state. Regions shown in green are metal fingers that are placed on top of MoS_2 present within the white dotted lines. The difference in the average potential of metal and MoS_2 for these three devices is shown in (**g**). Irrespective of the stress conditions, SDs exhibit substantially lower channel potential. Scale bar: 1 µm.

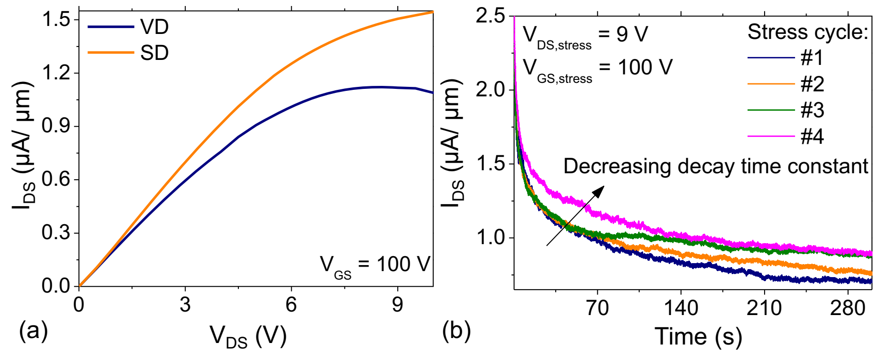

Fig. 8 Evidence of LTES-triggered perturbations in thermal transport properties of MoS_2. a MoS_2 FET exhibits current saturation at a higher critical field after being subjected to LTES. This implies that electrically stressed MoS_2 dissipates heat generated by electron–phonon scattering better than its virgin counterpart and therefore velocity saturation occurs at a higher critical field. **b** Electron–phonon scattering-induced self-heating is suppressed in MoS_2 after multiple LTES cycles. This is inferred from the observed monotonic decrease in the current decay time constant and perpetual increase in the saturation current value after every stress cycle. This suggests that MoS_2 channel becomes a better heat spreader after experiencing long-term electrical stress.

(τ) is observed due to enhanced electron–phonon scattering-induced self-heating in the channel[17]. Interestingly, subsequent LTES cycles result in higher saturation current and smaller current decay time constant, Fig. 8b. This implies that after every stress cycle, phonon scattering-led self-heating is suppressed due to which current saturates at a higher value and much faster in time. Such improvement in the heat dissipation capacity of the channel is attributed to a possible increase in the thermal conductivity of the material during every stress cycle. This result is particularly interesting because it suggests that MoS_2 exhibits a unique property where the material adapts to electrical stress conditions and becomes a better heat spreader every time it is subjected to high field conditions. Another possible mechanism by which MoS_2 may dissipate heat is through the substrate. Significant and marginal reduction in the χ_1 of E_{2g} and A_{1g}, respectively, observed in Table 1, have been previously reported to be fallouts of improved MoS_2-substrate coupling[28]. This complements the observed electrical stress-induced reduction in the current decay time constant and verifies that an LTES does improve the heat-dissipating capabilities of our MoS_2 field-effect transistors on SiO_2 substrates.

These findings seriously affect the roadmap and technological predictions on MoS_2 and other TMDCs. In particular, high-field transport-induced lattice deformation and its impact on threshold voltage pose serious questions on the supply voltage requirements for "more-than-Moore" technologies like 2D materials. Therefore, it is critical to establish a generalized understanding of the high-field stress-induced reliability of MoS_2 and TMDCs. While the findings of this work offer a glimpse of the limitations of 2D TMDCs' electrical reliability, detailed investigations must be performed on various TMDCs and how the synthesis methods affect the presented high-field response. Certain aspects of the high field reliability may change if the defect density, growth conditions/process, and MoS_2/dielectric interface quality are changed, which must be explored in future works to generalize these findings.

Conclusion

We report an unusual effect in CVD-grown monolayer MoS_2 where long-term electrical stress (LTES) or prolonged transistor operation introduces material and device perturbations. It turns out that intrinsic piezoelectricity in MoS_2 is responsible for the creation of electrically triggered defects, especially during ON state operation. These defects result in a negative shift in threshold voltage along with suppressed hopping transport within the channel. Poor dependence on temperature, prominent metal-insulator transition and large localization length implies the presence of unique defects that on one hand increase free electron concentration, like SVs, while on the other hand weaken the hopping mechanism, unlike SVs. The physical nature of such defects is identified through a classical treatment of observed Raman spectra of stressed and unstressed channel. Analysis of Raman spectra suggests that the observed red shift in the energy of Raman modes, particularly the out-of-plane A_{1g} mode, along with substantial increase in Raman intensity in ON state-stressed MoS_2 channel are results of weaker Mo-S bonds of MoS_2. Moreover, comparing VD and SD-Raman shift values of both the modes extracted for absolute zero temperature suggest a permanent change in the crystal structure due to

LTES. Intuitive reasoning and KPFM data validate the presence of such defects in the stressed channel which not only lower the channel potential but also suppress hopping transport, observed earlier. Electrical stress in the subthreshold, threshold and OFF state regimes of operation, delivers most of the voltage drop across one of the contacts for a long time, leading to piezoelectric response at the contact, subsequent piezoelectric response in the channel and/or increase in the channel-SV concentrations, as suggested by the large FWHM of Raman peaks and stronger temperature dependence of the conductance of devices stressed in the "low-current" regime. Besides its effect on electrical transport, there is evidence that LTES also perturbs thermal transport in MoS_2 field-effect transistors. Large critical field for velocity saturation, smaller current decay time constant during LTES of stressed MoS_2 devices and reduced temperature coefficients of Raman modes of stressed MoS_2 channel suggest that MoS_2 adapts to subsequent high field electrical stress cycles in a way that its heat-dissipating capability improves. These findings unveil a unique property observed in our MoS_2 devices due to which prolonged transistor operation weakens Mo-S bonds that modify both electrical and thermal transport properties.

Methods

Device fabrication. Monolayer CVD MoS_2 film grown on Sapphire is transferred onto a 285-nm thick thermally grown SiO_2 on Si substrate and cleaned in acetone and IPA to ensure minimum organic residue on the film. The sample is patterned (using electron beam lithography) in order to define regions for device fabrication. By using Oxygen plasma, unwanted MoS_2 is etched out inside a reactive ion etching (RIE) chamber followed by patterning (via electron beam lithography) of regions for source/drain electrode (Ni/Au: 10/50 nm) deposition inside an electron beam evaporator. Subsequent metal lift-off and vacuum anneal for 10 min at 250 °C ensure the removal of unnecessary metal from the sample and the formation of a high-quality metal-MoS_2 interface.

Electrical characterization. All devices are electrically characterized inside an in-house developed vacuum probe station at 10^{-7} torr to eliminate effects of atmospheric species like moisture and oxygen on device performance. Transistors are characterized before (VD) and after (SD) electrical stress cycles for a more legitimate comparison. Low-temperature measurements are also performed in the same vacuum probe station using an LN2-based open-loop cryogenic setup that reaches a temperature as low as 77 K.

Raman characterization. Raman spectra have been captured using a Horiba micro-Raman setup with a 532-nm laser and groove density/grating of 1800 g/mm. Raman spectra of monolayer MoS_2 of virgin and stressed devices have been obtained after calibrating the setup for a 520.7 cm^{-1} peak representing the signature Raman mode of silicon. Moreover, the Raman peak intensity values have also been normalized with respect to the silicon peak at 520.7 cm^{-1}.

Data availability

The data to support the findings of this work are available from the corresponding authors upon reasonable request.

Materials availability

The materials can be requested from ansh@iisc.ac.in.

Code availability

The codes to support the findings of this work are available from the corresponding authors upon reasonable request.

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Author contributions

A.A. and A.M. fabricated all the devices. A.A. performed electrical and KPFM measurements. A.A. and U.P. performed low-temperature Raman measurements. J.K. performed simulations in Quantumwise ATK. A.A. and M.S. analyzed the data and wrote the paper.

Competing interests

The authors declare no competing interests.

Additional information

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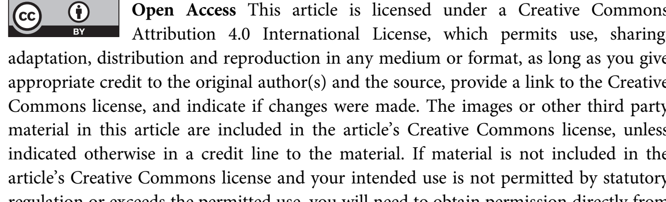

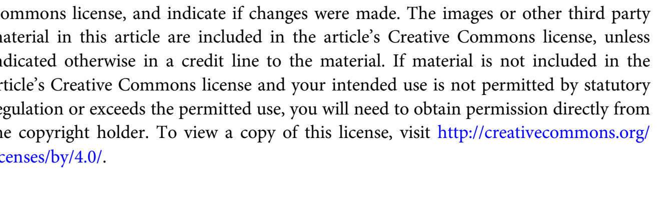

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