This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

Observations and Physical Insights Into Time-Dependent Hot Electron Current Confinement in AlGaN/GaN HEMTs on C-Doped GaN Buffer

Rajarshi Roy Chaudhuri, *Graduate Student Member, IEEE*, Vipin Joshi, Sayak Dutta Gupta, *Member, IEEE*, and Mayank Shrivastava, *Senior Member, IEEE*

***Abstract*—In this work, we report a unique time-dependent evolution of drain current and hot electron distribution along the width of AlGaN/GaN HEMTs on C-doped GaN buffer during semi-ON state stressing. The drain current evolution with stress time exhibited two distinct phases, i.e., first, drain current reduction at lower stress times, which, second, is followed by an increase in the magnitude for longer stress times. Electroluminescence (EL) measurements revealed this to be accompanied by a transition in the hot electron distribution along the device width, from being uniform (during the current reduction phase) to being confined near the center of the device (during current increase phase). Detailed experiments involving measure-stress-measure (M-S-M) routine showed a gate-stack-dependent threshold voltage shift in SiN_x-gated MISHEMTs to be responsible for the reduction in the drain current. On the other hand, increase in the drain current and hot electron confinement were observed in Schottky as well as MIS-gated devices. Furthermore, in situ thermoreflectance-based temperature monitoring showed a nonuniform temperature distribution along the device width. Detailed computations, taking into account the nonuniform temperature distribution, established heating induced nonuniform hole emission along the device width and their subsequent lateral redistribution to be responsible for the experimentally observed current increase and hot electron confinement.**

***Index Terms*—AlGaN/GaN HEMTs, buffer traps, carbon doped GaN buffer, drain current transient, electroluminescence (EL), hot electrons, reliability.**

Manuscript received 12 August 2022; revised 6 October 2022; accepted 6 October 2022. This work was supported by the Department of Science and Technology (DST), Government of India, and carried out at the Indian Institute of Science, Bengaluru, under Project SP/DSTO-21-035. The review of this article was arranged by Editor M. Meneghini. *(Rajarshi Roy Chaudhuri and Vipin Joshi contributed equally to this work.) (Corresponding author: Rajarshi Roy Chaudhuri.)*

The authors are with the Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: rajarshiroy@iisc.ac.in; mayank@iisc.ac.in).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3213627.

Digital Object Identifier 10.1109/TED.2022.3213627

I. Introduction

THE excellent electrical properties of AlGaN/GaN HEMTs make them suitable candidates for high-power and high-frequency switching applications, thereby enabling the design of efficient power conversion systems [1], [2]. However, several reliability challenges pose an obstacle to their wide scale industrial deployment [3]. Among the various reliability concerns, semi-ON state reliability is of particular importance, especially for developing reliable GaN HEMT switches. The semi-ON state is frequently encountered during switching, where, the HEMT is exposed to a high drain bias and a semi-ON gate bias simultaneously. The high drain bias leads to the presence of a high electric field and the semi-ON gate bias results in a significant number of electrons in the channel. Simultaneous presence of high field and channel carriers leads to the generation of high energy electrons (known as hot electrons) [4]. These hot electrons have a detrimental effect on the dynamic and static performance of the device [4], [5], [6], [7], [8]. The physics of hot electron-induced degradation has been extensively explored by monitoring and correlating electric field, carrier density, surface, and buffer trap ionization distribution [9], [10]. However, the analysis till now has been restricted to only 1-D, i.e., along the device length (from source to drain) [9], [10]. The power devices employed in the converter circuits, however, are typically wide devices (electrical width ranging from few 100's of μm to few mm), to enhance their ON-current carrying capability [11], [12]. Moreover, reliability studies carried out under ON-state stress [13] and electrostatic discharge (ESD) stress regime [14] have shown the device response to be nonuniform along the device width. Such nonuniform device response can significantly influence the device lifetime [15]. Thus, it is important to analyze the impact of semi-ON state stress on the device response along the width of the device.

In this work, we discuss impact of semi-ON state stressing on AlGaN/GaN HEMT device behavior, while considering its impact along the length as well as width of the device. To capture the impact of semi-ON state stress, the device characteristics including drain current and threshold voltage are

0018-9383 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 22,2022 at 05:39:23 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

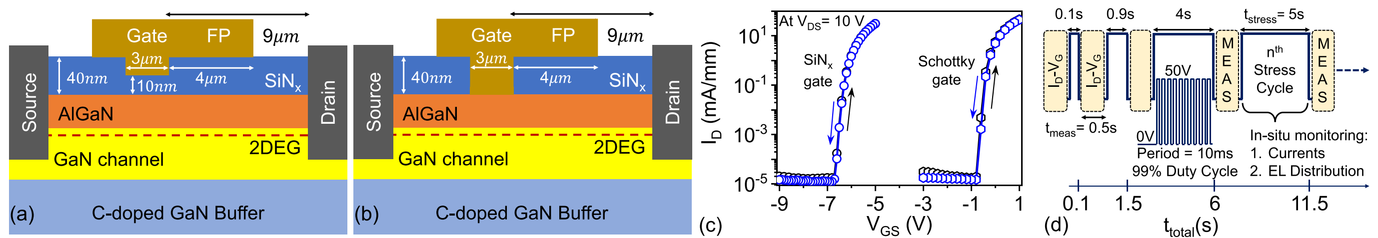

Fig. 1. Device schematic of the AlGaN/GaN HEMTs with (a) SiN_x-gate and (b) Schottky-gate, used for the investigation. (c) Typical dual-sweep transfer characteristics of the HEMTs. (d) Schematic describing the M-S-M waveform and the associated parameters monitored during the stress cycle.

monitored during the stress cycle. To evaluate the presence and distribution of hot electrons along the length as well as width of the device, on-the-fly electroluminescence (EL) mapping of the entire gate–drain (G-D) access region is done. The analysis reveals a unique behavior of drain current ($I_{\text{DS-Stress}}$) and hot electron distribution with stress time. $I_{\text{DS-Stress}}$ initially reduced with increasing stress time and then showed a significant increase in magnitude as stress time was increased further. The increase in $I_{\text{DS-Stress}}$ was accompanied by a confinement of hot electrons in the center of the device width. In situ temperature monitoring during stress and detailed computational analysis are used to probe the underlying physical mechanism. This article is structured as follows. The device structure and the experimental setup are discussed in Section II. The experimental observations of the effect of semi-ON stress on device parameters, including drain current, threshold voltage and hot electron distribution is presented in Section III. The detailed physical insights into the current transient behavior and the observed hot electron confinement phenomena are discussed in Section IV. Finally, Section V concludes the work.

II. Experimental Setup

SiN_x and Schottky-gated AlGaN/GaN HEMTs, as shown in Fig. 1(a) and (b), respectively, were fabricated on GaN on Si epi-stack, using a well-optimized process flow [16], [17]. The 100-μm-wide HEMTs were simultaneously processed, thereby reducing any process induced variability amongst these devices. The transfer characteristics of the HEMTs, shown in Fig. 1(c), reveal excellent ON-state behavior and significantly low OFF-state leakage (<25 nA/mm) with negligible hysteresis, irrespective of the gate-stack design. The semi-ON state characteristics of the devices were analyzed using a measure-stress-measure (M-S-M) routine. The routine, as shown in Fig. 1(d), begins with a measure cycle where the I_D-V_{GS} characteristics of the device were measured for $V_{\text{DS}} = 10$ V. It was followed by a stress cycle wherein the device was stressed in semi-ON state by biasing the gate at $V_{\text{GS-Stress}} = V_{\text{Th}} + 0.5$ V. V_{Th} was defined as V_{GS} for which $I_D = 1$ μA/mm. On the other hand, the drain stress voltage ($V_{\text{DS-Stress}}$) was pulsed from 0 to 50 V with pulses having a period of 10 ms and ~99% duty cycle (it then allowed us to monitor temporal evolution of $I_{\text{DS-Stress}}$). The number of such pulses was varied to modulate the stress cycle period. During the stress cycle, the source and substrate terminals were grounded. The stress cycle was immediately followed by a measure cycle, similar to the one preceding it. Thus, the total time for which the device is subjected to the M-S-M routine, defined as t_{total}, includes both measure cycle time (t_{meas}) and stress cycle time (t_{stress}). To investigate the device reliability under stress, in situ measurements of current transients, EL intensity distribution, and GaN channel temperature were carried out.

3-D computations were carried out on the Schottky-gated device, as shown in Fig. 1(a), using a well-calibrated computational framework based on our earlier works in [18], [19], and [20]. Schottky contact with tunneling model to estimate leakage current was used as a gate electrode. On the other hand, Schottky contact with lower work function and highly doped region in the contact proximity were used to estimate behavior of source/drain contacts [20]. Donor type traps at the AlGaN/SiN_x interface were considered to calibrate n_s and gate leakage [20]. C-doping-induced traps in the GaN buffer were modeled as both acceptor and donor traps, with a higher concentration of acceptor traps. The acceptor traps were considered to have an activation energy of $E_V + 0.9$ eV and donor traps were considered to have an activation energy of $E_C - 0.11$ eV. The acceptor/donor trap concentration of $3 \times 10^{18}/2 \times 10^{17}$ cm^{-3} was considered [19]. Substrate terminal was grounded for all the computations. For simplicity of computations in the 3-D domain, lattice and carrier heating were neglected. However, as will be discussed later in this work, neglecting the same does not affect the analysis presented in this work. Further details about the computational framework can be found in our earlier works [18], [19], [20].

III. Device Response to Semi-ON Stress

Devices were subjected to semi-ON state stress and its impact on electrical parameters, including drain current, threshold voltage, and hot electron distribution is discussed here.

A. Capturing Dynamic Processes During the Stress Cycle

1) Drain Current: To observe how device characteristics evolve dynamically, $I_{\text{DS-Stress}}$ was measured during the stress cycle and is shown in Fig. 2. Fig. 2(a) shows that $I_{\text{DS-Stress}}$ for SiN_x-gated devices initially reduces with t_{total}, marked as phase P1. However, as t_{total} is increased further, $I_{\text{DS-Stress}}$ starts increasing. This regime of device operation is marked

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 22,2022 at 05:39:23 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

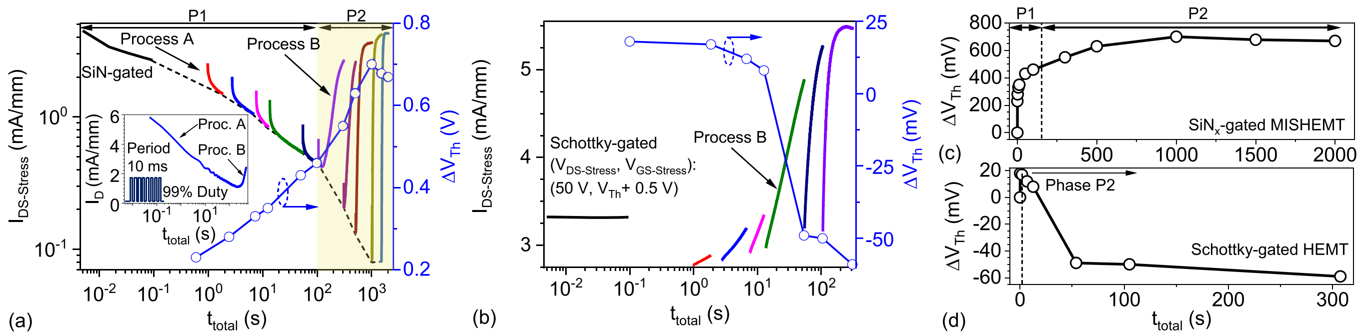

Fig. 2. Transient evolution of drain current during stress ($I_{DS\text{-}Stress}$) in (a) SiN_x-gated and (b) Schottky-gated HEMT, showing the two phases P1 and P2. While, phase P1 is constituted by process *A*, phase P2 is constituted by both processes *A* and *B*. The stress-induced shift in threshold voltage ($\Delta V_{Th} = V_{Th,Poststress} - V_{Th,Pristine}$) is shown. V_{Th} is evaluated in the measure cycle present between two stress cycles. The ΔV_{Th} transient for (c) SiN_x-gated and (d) Schottky-gated HEMT depicted in linear timescale. Inset of figure (a): $I_{DS\text{-}Stress}$ transient due to an uninterrupted stress cycle.

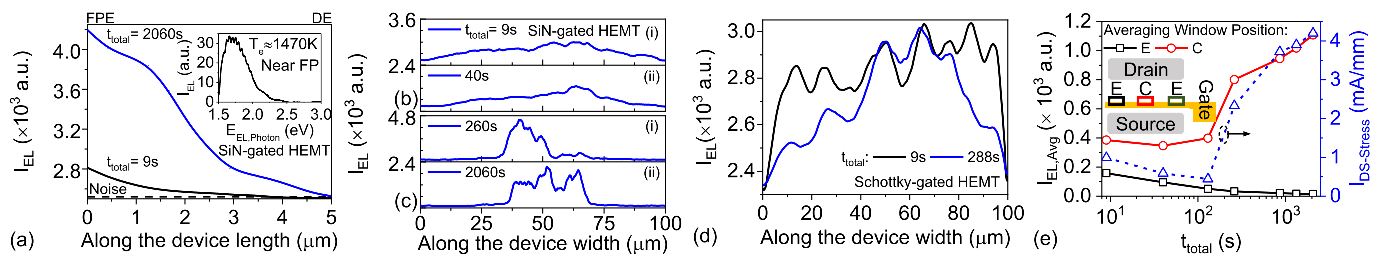

Fig. 3. (a) Lateral distribution of EL intensity (I_{EL}), measured at the device center in SiN_x-gated device, showing peak near FPE. Inset: EL spectra measured near FPE showing presence of hot electrons. Electron temperature (T_e) is measured from the high energy slope of the EL spectra. Temporal evolution of I_{EL} along the device width at the FPE in (b) and (c) SiN_x-gated, and in (d) Schottky-gated HEMT shows the confinement of EL signal as stress time increases. (e) Temporal evolution of average EL intensity ($I_{EL,Avg}$) at various locations (edges "*E*" and central region "*C*") along FPE and their relationship with $I_{DS\text{-}Stress}$ is shown for the SiN_x-gated device.

as phase P2. The physical process governing $I_{DS\text{-}Stress}$ reduction(increase) in phase P1(P2) is labeled as process A(B). While Schottky-gated devices did not exhibit process A, they showed distinct increase in $I_{DS\text{-}Stress}$ (process B), as t_{total} was increased, as shown in Fig. 2(b). This suggests process B to be independent of the gate-stack, while process A is a function of the gate-stack. It should be noted here that the current transients also included measure cycle between different stress cycles. Although this resulted in a partial recovery of $I_{DS\text{-}Stress}$ leading to a higher $I_{DS\text{-}Stress}$ at the beginning of each stress cycle, insertion of measure cycle does not affect the device behavior. This is validated by the presence of processes A and B even in the absence of the measure cycle, as can be seen in the inset of Fig. 2(a).

2) Threshold Voltage: Along with $I_{DS\text{-}Stress}$, measurements of I_D–V_{GS} as per the routine shown in Fig. 1(d), allowed us to measure the evolution of V_{Th} of the device during stress. V_{Th} evolution of the devices measured as $\Delta V_{Th} = V_{Th,Poststress} - V_{Th,Pristine}$, is shown in Fig. 2(a) and (b) on a scale similar to that of $I_{DS\text{-}Stress}$ for a comparison of $I_{DS\text{-}Stress}$ and V_{Th} evolution. Similar V_{Th} evolution is also plotted on a linear time scale for SiN_x and Schottky-gated devices, as shown in Fig. 2(c) and (d), respectively, for a better representation of V_{Th} evolution with stress time. V_{Th} of the SiN_x-gated device, as shown in Fig. 2(c), exhibited a significant positive shift (>200 mV) after the first stress cycle. The magnitude of positive V_{Th} shift increased initially with t_{total} and then showed a gradual reduction as t_{total} was increased beyond $\sim 10^3$ s. On the other hand, V_{Th} of the Schottky devices, as shown in Fig. 2(d), exhibited a marginal positive shift (∼25 mV) initially. However, magnitude of this positive shift reduced and finally V_{Th} exhibited a negative shift as t_{total} was increased. It is worth highlighting here that the magnitude of V_{Th} shift in the Schottky device is much lower (maximum ΔV_{Th} of 25 mV) as compared to that for the SiN_x-gated device (maximum ΔV_{Th} of 700 mV). Any impact on V_{Th} is a direct measure of trapping in the gate-stack and in the buffer region under the gate. These observations thus suggest time-dependent trapping process to occur in the gate-stack or in the buffer region under the gate, during stress.

3) Hot Electron Generation and Distribution: Apart from the electrical parameters, EL signals from the device were also captured to monitor the evolution of hot electron distribution and to identify the hotspots. Fig. 3(a) shows one such EL intensity (I_{EL}) distribution along the length of the SiN_x-gated device. I_{EL} shows a peak near the field plate edge (FPE), which gradually reduces as we move toward the drain edge (DE) finally reaching the noise floor at the DE. This establishes EL hotspot to be near FPE. Moreover, electron temperature (T_e) analysis of EL spectra acquired from the location of EL hotspot [see inset of Fig. 3(a)] shows EL to be associated with high T_e of ∼1470 K. This establishes the presence of hot electrons and the observed EL signal to be a direct measure of the same. Considering the EL hotspot to be near FPE, I_{EL} distribution along the device width was then extracted near FPE to understand how it evolves with t_{total}.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 22,2022 at 05:39:23 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

The results are shown in Fig. 3(b) and (c). Fig. 3(b) and (c) shows that initially hot electron distribution is uniform along the device width. However, as the device is subjected to longer stress cycles, I_{EL} or, in other words, hot electron population starts increasing in the center of the device. On the other hand, it reduces in the edge regions, leading to a strong hot electron confinement in the center of the device. EL intensity distribution for Schottky-gated devices, as shown in Fig. 3(d), also exhibits a similar EL confinement, showing this effect to be gate-stack independent.

B. Relationship Between the Drain Current, Threshold Voltage, and Hot Electron Distribution

Both $I_{DS\text{-}Stress}$ and V_{Th} show a stress time dependence, as shown in Fig. 2. For SiN_x-gated devices, a significant positive V_{Th} shift is observed initially. This reduces the effective gate overdrive (V_{GS}-V_{Th}) for a given fixed V_{GS}, reducing $I_{DS\text{-}Stress}$. This explains the observed reduction in $I_{DS\text{-}Stress}$, i.e., process A, for SiN_x-gated devices. On the other hand, Schottky devices, which exhibited a marginal positive V_{Th} shift, did not exhibit process A. This further establishes process A to be associated with gate-stack dependent V_{Th} shift, which could be associated with trapping/detrapping in the gate-stack.

On the other hand, the involvement of gate-stack in controlling process B in SiN_x-gated devices, i.e., an increase in $I_{DS\text{-}Stress}$, can only be explained if V_{Th} completely recovers or a negative V_{Th} shift is observed. However, Fig. 2(a) shows that process B is accompanied neither by a V_{Th} recovery nor a negative V_{Th} shift. Moreover, the presence of process B in a completely different Schottky-gate-stack, as seen in Fig. 2(b), establishes process B to be independent of the gate-stack. While V_{Th} does not recover in SiN_x-gated devices, it does exhibit a reduction in the magnitude of positive shift when the device exhibits process B followed by a gradual reduction for $t_{total} > 10^3$ s, as shown in Fig. 2(c). Similarly, Schottky devices also show a reversal in sign of V_{Th} shift as a device exhibits process B, as shown in Fig. 2(d). A gate-stack independent change in the behavior of V_{Th} shift suggests a change in channel conductivity, which is induced by factors other than the gate-stack. Detrapping of charges from the GaN buffer can be one such factor and will be discussed later.

Furthermore, Fig. 3(b) and (c) shows the hot electron distribution to be time dependent. The $I_{DS\text{-}Stress}$ transient [shown in Fig. 2(a)] and hot electron distribution [shown in Fig. 3(c)] show that the process of increase in $I_{DS\text{-}Stress}$, i.e., process B, and hot electron confinement along the device width are observed only after device has been stressed for longer durations. To probe further into the time dependence of hot electron distribution, the device width was divided into two observation windows—E (at the two edges) and C (at the center), as shown in the inset of Fig. 3(e). In these windows, the EL distribution was integrated and then averaged to obtain $I_{EL,Avg}$. Fig. 3(e) shows that $I_{EL,Avg}$ reduces at the device edges (window E) as t_{total} is increased. On the other hand, $I_{EL,Avg}$ in the device center (window C) initially decreases and then starts to increase as t_{total} is increased. To determine any correlation between the time dependence of $I_{EL,Avg}$ and $I_{DS\text{-}Stress}$, $I_{DS\text{-}Stress}$ as a function of t_{total} is also plotted in Fig. 3(e). It shows that t_{total} beyond which $I_{EL,Avg}$ in the central region starts to increase coincides with t_{total} beyond which $I_{DS\text{-}Stress}$ increases and process B is observed. This suggests the onset of increase in $I_{EL,Avg}$ in the central region of the device, i.e., hot electron confinement, to be correlated with the onset of process B.

IV. Physical Mechanism Governing Increase in $I_{DS\text{-}Stress}$ and EL Confinement

A. Understanding Sources of Increase in $I_{DS\text{-}Stress}$ and EL Confinement

As discussed earlier, increase in $I_{DS\text{-}Stress}$ (process B) and EL confinement were found to be accompanied by a change in the V_{Th} behavior. This suggested a change in channel conductivity during process B. In semi-ON state, the channel conductivity is least under the gate region. Under such operating conditions, channel conductivity can be improved by an increase in the channel electron density (n_s) underneath the gate electrode. As discussed earlier, gate-stack independent nature of the process suggests trapping/detrapping of carriers in the C-doped GaN buffer. Furthermore, an increase in n_s and $I_{DS\text{-}Stress}$ should lead to an increase in the hot electron population and hence EL intensity should increase. A nonuniform increase in EL intensity, along the device width (seen in Fig. 3), thus suggests the increase in n_s to be nonuniform.

1) Mechanism Affecting Trapping/Detrapping of Carriers in the C-Doped GaN Buffer: Electron trapping [17]/hole emission [21] in the C-doped GaN buffer are known to reduce n_s and $I_{DS\text{-}Stress}$. However, process B cannot be directly explained by these processes. Another factor that can affect trapping/detrapping of carriers in the C-doped GaN buffer, especially under semi-ON stress, is the interaction of hot electrons with phonons. Such an interaction results in a significant increase in the device temperature in the G-D access region [8]. To analyze device temperature-induced changes in $I_{DS\text{-}Stress}$ and EL distribution, temperature distribution along the device width was also monitored during the stress cycle. The temperature profile, shown in Fig. 4(a), shows the temperature at the edges to be significantly higher than that at the device center for both SiN_x-gated and Schottky-gated HEMTs. Furthermore, Fig. 4(a) shows that the Schottky devices have a higher temperature in the device center as compared to SiN_x gated devices. This can be attributed to higher current levels in the Schottky device and the absence of process A, as seen from the current transients shown in Fig. 2(b).

2) Impact of Temperature Distribution on n_s: The nonuniform increase in device temperature along the device width can give rise to nonuniform trapping/detrapping processes within the GaN buffer. As discussed in [21], temperature rise enhances hole emission from the C-doping induced acceptor traps. This increases negatively charged ionized buffer acceptor trap concentration (IBATC), which results in channel depletion. Higher temperature in the edge of the device can thus increase IBATC in these regions. This will reduce n_s in the edges, leading to current confinement in the center of the device. This explains the process of EL confinement.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 22,2022 at 05:39:23 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

An increase in current flow through the center of the device should now lead to an increase in temperature in the center of the device. However, the experimental setup used to measure temperature does not allow us to probe this condition. The experimental setup used a thermo-reflectance imaging technique which employed a 365-nm UV LED source to measure the GaN channel temperature. Exposing the device to UV was found to eliminate process B, as shown in Fig. 4(b). As process B and EL confinement were found to be correlated, an absence of process B also suggests an absence of EL confinement. Hence, the impact of EL confinement on channel temperature cannot be probed experimentally. As exposure to 365-nm UV is known to enhance detrapping in the C-doped GaN buffer, the absence of process B under UV exposure further suggests trapping in the GaN buffer to be responsible for process B. It should be noted that although UV exposure would affect trapping/detrapping processes, however, it does not affect the interaction of hot electrons with phonons. Thus, it will have a negligible impact on the channel temperature measurements.

It is worth highlighting here that, as discussed above, the process of hot electron confinement can itself modulate the temperature distribution. The temperature distribution can in turn affect the hot electron confinement. The overall process can cause movement of the confinement region along the device width. Such a process can lead to moving current filament as observed in Si devices [22].

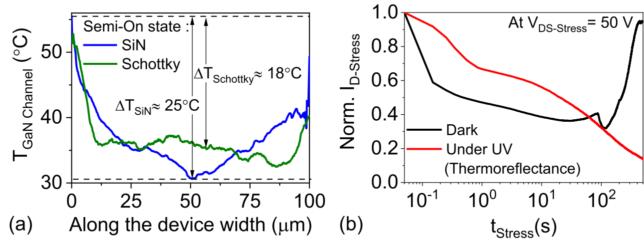

Fig. 4. (a) GaN channel temperature ($T_{\text{GaN Channel}}$ during semi-ON state stress) distribution in Schottky-gated and SiN_x-gated HEMTs, extracted near FPE. The dissipated power was kept constant at 65 mW. (b) Temporal evolution of drain current during UV thermoreflectance run compared with that in dark, shows process B to be suppressed under UV.

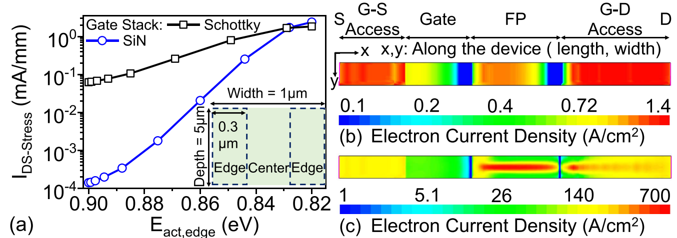

Fig. 5. Evaluation of the impact of nonuniform heating on device behavior using 3-D computations. (a) Effect of buffer acceptor trap activation energy ($E_{\text{act,edge}}$) on drain current of Schottky and SiN_x-gated HEMTs during semi-ON state stress at $V_{\text{DS-Stress}} = 50$ V and $V_{\text{GS-Stress}} = V_{\text{Th}} + 0.5$ V. Inset: three regions defined along the width of the GaN buffer. The activation energy $E_{\text{act,edge}}$ was varied in the two edges and was kept fixed at 0.9 eV in the central region. Electron current density distribution, in the Schottky device, extracted for $E_{\text{act,edge}}$ of (b) 0.9 and (c) 0.82 eV. This was extracted by taking a cut-plane along the channel.

B. Probing Further Using Computations

1) Capturing the EL Confinement and Drain Current Increase:

Given the limitations of the experimental setup to further probe into the underlying mechanisms, computational analysis was carried out. However, precise modeling and simulation of the impact of hot electrons and the consequent nonuniform rise in lattice temperature [seen in Fig. 4(a)] is nontrivial. Hence, to model the same in the computations, the activation energy of the C-doping induced acceptor traps (E_{act}) in the GaN buffer was varied. This modeling is based on the dependence of emission rate (e) from a trap on its E_{act} and lattice temperature T, which can be expressed as

$$e \propto T^2 \exp\left(\frac{-E_{\text{act}}}{kT}\right). \tag{1}$$

Here, E_{act} is the trap activation energy calculated as $E_{\text{act}} = E_{\text{BT}} - E_V$, where, E_{BT} denotes trap energy level and E_V represents valence band energy level. In the temperature range of interest [temperature variation from 300 to 325 K as seen in Fig. 4(a)], the T^2 dependence is less dominant than the exponential term. Hence, the effect of rise in T on e can be approximated as follows:

$$\frac{e_1}{e_2} = \frac{\exp(-E_{\text{act}}/kT_1)}{\exp(-E_{\text{act}}/k(T_1+a))}. \tag{2}$$

Here, e_1 and e_2 corresponds to the emission rates at $T = T_1$ and $T = T_1 + a$ ($a > 0$), respectively,

$$\frac{e_1}{e_2} = \exp\left(\frac{-\beta E_{\text{act}}}{kT_1}\right), \quad \text{where,} \quad \beta = \frac{a}{T_1+a} < 1. \tag{3}$$

Now, the variation in E_{act} (from E_{act} to $E_{\text{act},1}$), keeping temperature fixed at T_1, which would emulate the effect of temperature variation on e is derived as follows:

$$\frac{e_1}{e_2} = \frac{\exp(-E_{\text{act}}/kT_1)}{\exp(-E_{\text{act},1}/kT_1)}. \tag{4}$$

Thus, by equating (3) with (4), we obtain

$$E_{\text{act},1} = (1-\beta)E_{\text{act}}. \tag{5}$$

Thus, the effect of increase in lattice temperature from T_1 to $T_1 + a$ on emission rate e can be captured by reducing the activation energy from E_{act} to $E_{\text{act},1} = (1-\beta)E_{\text{act}}$ [refer to (4) and (5)]. Above numerical analysis yields a reduced $E_{\text{act},1}$ of 0.82 eV for $E_{\text{act}} = 0.9$ eV and a ~25-K increase in temperature.

3-D computations were carried out to evaluate the impact of stress on current distribution along the device width. Schottky and MIS-gated device structures, as shown in Fig. 1(a) and (b), with a width of 1 μm was used to analyze the device behavior. A smaller device width was used for ease of computations without affecting the overall mechanism. Computations accounted for nonuniform heat or E_{act} distribution along the device width by splitting the C-doped GaN buffer in three regions, as shown in the inset of Fig. 5(a). While E_{act} in the center region ($E_{\text{act,center}}$) was kept constant at 0.9 eV, the same was ramped in the edge regions ($E_{\text{act,edge}}$) from 0.9 to 0.82 eV after biasing the device in semi-ON state with $V_{\text{DS}} = 50$ V. Irrespective of the gate-stack,

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 22,2022 at 05:39:23 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

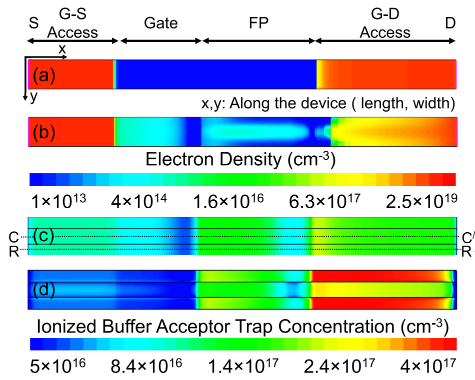

Fig. 6. Channel electron density distribution as $E_{act,edge}$ is varied from (a) 0.9 to (b) 0.82 eV. The 2-D distribution of IBATC for $E_{act,edge}$= (c) 0.9 and (d) 0.82 eV is also shown. The IBATC distribution was analyzed by taking a 2-D cut-plane along the device length at the top of C-doped GaN buffer.

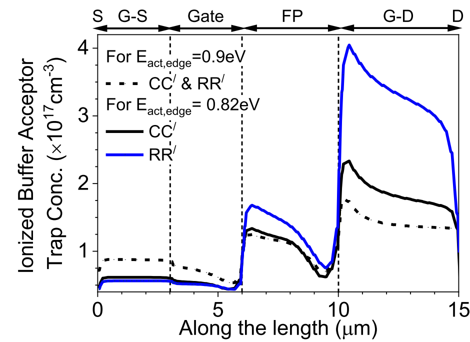

Fig. 7. IBATC for $E_{act,edge}$ of: 1) 0.9 and 2) 0.82 eV, extracted along two cross-sectional cut-lines (Center-CC$^{/}$ and Right Edge- RR$^{/}$ marked in Fig. 7), at the top surface of C-doped GaN buffer, along the device length.

$I_{DS\text{-}Stress}$ shows an increase in magnitude as $E_{act,edge}$ is reduced, as shown in Fig. 5(a). This further validates the process of $I_{DS\text{-}Stress}$ increase (process B) to be independent of the gate-stack. Taking advantage of this gate-stack independence, further analysis is carried out on SiN_x-gated devices. The current density distribution extracted at $E_{act,edge}$ of 0.9 and 0.82 eV, as shown in Fig. 5(b) and (c), respectively, shows current confinement along the device width with an increased current density in the central region, as $E_{act,edge}$ is lowered to 0.82 eV [see Fig. 5(c)]. This current confinement effect is similar to the EL confinement observed experimentally (shown in Fig. 3) and the increase in $I_{DS\text{-}Stress}$ is similar to process B observed experimentally in $I_{DS\text{-}Stress}$ transient (see Fig. 2). The above discussion establishes the nonuniform distribution of temperature (modeled as nonuniform distribution of E_{act}) along the device width in semi-ON state operation to be responsible for the observed EL confinement as well as increase in $I_{DS\text{-}Stress}$. Further, these observations highlight that nonuniform distribution of E_{act}, emulating nonuniform device heating, could capture the experimentally observed processes. This allows us to neglect the lattice and carrier heating, thereby reducing computation complexity, without affecting the underlying physical mechanism.

2) Probing the Underlying Physical Mechanism: Given that computations were able to reproduce the experimental observations, computational analysis was used to further analyze the underlying physical mechanism. To understand the factors affecting current distribution, electron density distribution within the device before and after the $E_{act,edge}$ ramp was extracted and is shown in Fig. 6(a) and (b), respectively. It shows that electron density in the G-D access region reduces as $E_{act,edge}$ is reduced from 0.9 to 0.82 eV. Further, the observed reduction in electron density is found to be nonuniform along the device width with larger reduction observed in the edge regions. The observed reduction in electron density can be attributed to increased ionization of buffer acceptor traps in the G-D access region when $E_{act,edge}$ is reduced from 0.9 to 0.82 eV, as shown in Fig. 6(c) and (d), respectively. To clearly understand the $E_{act,edge}$ dependent variation of IBATC, along the device length, observations were made by taking two cutlines [marked in Fig. 6(c)], as shown in Fig. 7. Figs. 6(d) and 7 shows a larger increase in IBATC in the edge regions as compared to the central region. This corroborates well with the hole emission theory [21], which predicts an increase in IBATC as the temperature is increased or E_{act} is reduced.

Despite the observed reduction in electron density, Fig. 5(a) showed an increase in $I_{DS\text{-}Stress}$ as $E_{act,edge}$ was reduced. To explain this $I_{DS\text{-}Stress}$ behavior, it is important to identify the different channel resistance components determining $I_{DS\text{-}Stress}$. To understand the same, the channel electron density profile is extracted at $E_{act,edge}$ = 0.9 eV, as shown in Fig. 8(a). It indicates that the net channel resistance can be considered to be a series combination of the resistance offered by the gate–source (G-S) access region (R_{GS}), channel region under the gate (R_{UG}) and field plate (FP) (R_{UFP}) and the G-D access region (R_{GD}). Fig. 8(a) shows R_{UG} and R_{UFP} to be significantly greater than R_{GS} and R_{GD}. The net channel resistance and hence the current flowing through the device will then be determined by the value of R_{UG} and R_{UFP}. Fig. 8(a) further shows that electron density under the gate and FP increases significantly as $E_{act,edge}$ is reduced. This explains the observed increase in $I_{DS\text{-}Stress}$. Furthermore, Fig. 6(a) and (b) show the electron density increase to be nonuniform along the device width under the FP. The increase in electron density in the channel region under the FP is higher in the central region as compared to edge regions. This nonuniform distribution of electron density under the FP explains the observed EL confinement.

Experimental observations from the V_{Th} study, shown in Fig. 2, also supports this observed increase in electron density under the gate and FP region. Fig. 2(a) and (c) show that positive increase in ΔV_{Th} starts reducing as t_{total} is increased. A reduction in the positive V_{Th} shift for SiN_x-gated devices, seen in Fig. 2(a) and 2(c), and a negative V_{Th} shift for Schottky-gated devices, seen in Fig. 2(b) and (d), was observed at higher t_{total}. Both these observations suggest an increase in n_s under the gate.

3) Sources of Increase in Channel Electron Density Under the Gate and Field Plate: An increase in channel electron density

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 22,2022 at 05:39:23 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

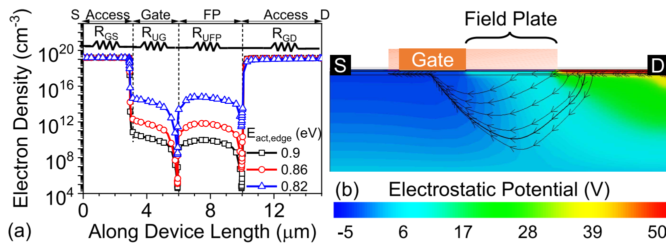

Fig. 8. (a) Lateral channel electron density profile showing significant increase in electron density, under the gate and FP, as trap activation energy ($E_{\mathrm{act,edge}}$) is reduced from 0.9 to 0.82 eV. Various components of the total channel resistance have been indicated using a schematic. (b) Distribution of electrostatic potential extracted along device length. The streamlines represent hole current density direction.

under the gate upon reducing $E_{\mathrm{act,edge}}$ can be explained by comparing IBATC under the gate for different $E_{\mathrm{act,edge}}$ values, as shown in Figs. 6(c) and (d) and 7. Figs. 6(c) and (d) and 7 show that IBATC under the gate reduces as $E_{\mathrm{act,edge}}$ is reduced from 0.9 to 0.82 eV. This directly explains the observed increase in electron density in the channel region under the gate.

On the other hand, IBATC under the FP remains unchanged in the central region and shows an increase in the edge regions with a reduction in $E_{\mathrm{act,edge}}$. Owing to the IBATC profile, electron density under the FP should have remained unchanged in the central region and should have reduced at the edges. However, Fig. 6(b) shows that electron density under the FP shows an increase in the central region. This can be explained by noting that Fig. 6(b) shows electron density distribution in the device in nonequilibrium condition, wherein net channel resistance is determined by the channel electron density under the gate electrode [as seen in Fig. 8(a)]. An increase in channel electron density under the gate will thus result in an increase in $I_{\mathrm{DS\text{-}Stress}}$. This, in turn, will cause electron density under the FP to increase to maintain current continuity. The nonuniform IBATC profile under the FP, as shown in Figs. 6(d) and 7(a), results in a nonuniform increase in the electron density and electron current under the FP, as seen in Figs. 5(c) and 6(b), respectively.

The above discussion establishes a reduction in IBATC under the gate to be responsible for the increase in channel electron density there, which leads to an $I_{\mathrm{DS\text{-}Stress}}$ increase, as seen in Fig. 5(a). On the other hand, nonuniform buffer acceptor trap ionization under the FP results in the EL confinement effect seen in Fig. 3.

4) Sources of Reduction in IBATC Under the Gate: A reduction in IBATC under the gate was accompanied by an increase in IBATC in the G-D access region, as seen in Figs. 6(c) and (d) and 7(a). While hole emission explains the behavior in the access region, the mechanism controlling IBATC reduction under the gate is discussed here.

A reduction in IBATC under the gate requires the emission of electrons from the ionized acceptor traps. The emission of electrons can be either from the conduction band or to the valence band. However, given that the trap energy levels considered in these computations are deep with $E_{\mathrm{act}} = E_v + 0.9$ eV, an emission to the conduction band will require transfer of a significant amount of energy to the trap. Provided that computations do not account for temperature or any other external excitation, electron emission to the conduction band will be negligible. On the other hand, electron emission to the valence band would require holes in the valence band for recombination to happen. One of the possible sources of the increase in hole density under the gate is a lateral redistribution of holes emitted from the G-D access region. To evaluate the possibility of lateral hole redistribution, the electrostatic potential distribution and the direction of the hole current are shown in Fig. 8(b). Fig. 8(b) shows the presence of higher electrostatic potential in the G-D access region due to the applied positive drain bias. The potential falls under the FP edge and further reduces near the gate electrode due to negative gate bias. This creates conditions favorable for the lateral redistribution of holes, which can then accumulate under the gate electrode and in the G-S access region. This is further evident from Fig. 8(b), which shows the direction of flow of hole current to be from the G-D access region through the buffer region under the gate electrode. Hole emission from the G-D access region thus triggers the electron emission under the gate. This results in an increase in the electron density under the gate and hence triggers an increase in $I_{\mathrm{DS\text{-}Stress}}$. Furthermore, nonuniform heating of the device in semi-ON state accelerates the process of hole emission and results in the observations of an increase in drain current and hot electron confinement along the device width.

V. Conclusion

Detailed experiments on AlGaN/GaN HEMTs under semi-ON state stressing were carried out while monitoring drain current, hot electron, and temperature distribution during the stress cycle. Temporal evolution of drain current in SiN_x-gated HEMTs showed a gradual reduction for lower stress times. A positive threshold voltage shift and absence of the process in Schottky devices established the reduction in drain current to be a gate-stack-dependent phenomenon. On the other hand, stressing the device for longer durations resulted in a unique increase in the drain current. This increase was found to be independent of the gate-stack. In situ EL analysis along the device width revealed the increase in drain current to be accompanied by unique confinement of hot electrons in the center of the device. In situ temperature measurements showed a nonuniform temperature distribution along the device width, which was found to result in the observed nonuniform hot electron distribution. Detailed computations established this nonuniform temperature distribution to result in nonuniform hole emission. Redistribution of these holes from the G-D access region to the region under the gate allowed for hole accumulation and subsequent reduction in ionized trap charges in the GaN buffer under the gate. The resulting increase in electron density under the gate led to the observed increase in drain current.

Acknowledgment

The authors would like to thank MNCF and NNFC at IISc, Bengaluru. Student authors Rajarshi Roy Chaudhuri and Sayak Dutta Gupta would also like to thank DST INSPIRE for their fellowship.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 22,2022 at 05:39:23 UTC from IEEE Xplore. Restrictions apply.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

References

[1] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, 2017, doi: 10.1109/TED.2017.2657579.

[2] M. Meneghini, G. Meneghesso, and E. Zanoni, *Power GaN Devices*. Cham, Switzerland: Springer, 2017, doi: 10.1007/978-3-319-43199-4.

[3] M. Meneghini et al., "Reliability and failure analysis in power GaN-HEMTs: An overview," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 1–8, doi: 10.1109/IRPS.2017.7936282.

[4] I. Rossetto et al., "Evidence of hot-electron effects during hard switching of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3734–3739, Sep. 2017, doi: 10.1109/TED.2017.2728785.

[5] M. Meneghini et al., "Negative bias-induced threshold voltage instability in GaN-on-Si power HEMTs," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 474–477, Apr. 2016, doi: 10.1109/LED.2016.2530693.

[6] I. Hwang et al., "Impact of channel hot electrons on current collapse in AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1494–1496, Dec. 2013, doi: 10.1109/LED.2013.2286173.

[7] Y. S. Puzyrev et al., "Dehydrogenation of defects and hot-electron degradation in GaN high-electron-mobility transistors," *J. Appl. Phys.*, vol. 109, no. 3, 2011, Art. no. 034501, doi: 10.1063/1.3524185.

[8] R. R. Chaudhuri, V. Joshi, S. D. Gupta, and M. Shrivastava, "On the channel hot-electron's interaction with C-doped GaN buffer and resultant gate degradation in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 4869–4876, Oct. 2021, doi: 10.1109/TED.2021.3102469.

[9] A. Minetto et al., "Hot-electron effects in AlGaN/GaN HEMTs under semi-on DC stress," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4602–4605, Nov. 2020, doi: 10.1109/TED.2020.3025983.

[10] N. Modolo et al., "A physics-based approach to model hot-electron trapping kinetics in p-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 673–676, May 2021, doi: 10.1109/LED.2021.3067796.

[11] B. Hassan et al., "Large periphery GaN HEMTs modeling using distributed gate resistance," *Phys. Status Solidi A*, vol. 216, no. 1, 2019, Art. no. 1800505, doi: 10.1002/PSSA.201800505.

[12] S. Singhal et al., "Reliability of large periphery GaN-on-Si HFETs," *Microelectron. Rel.*, vol. 46, no. 8, pp. 1247–1253, 2006, doi: 10.1016/J.MICROREL.2006.02.009.

[13] M. Meneghini et al., "Secondary electroluminescence of GaN-on-Si RF HEMTs: Demonstration and physical origin," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1032–1037, Mar. 2017, doi: 10.1109/TED.2017.2654859.

[14] J. Kuzmík, D. Pogany, E. Gornik, P. Javorka, and P. Kordoš, "Electrostatic discharge effects in AlGaN/GaN high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 83, no. 22, pp. 4655–4657, Feb. 2003, doi: 10.1063/1.1633018.

[15] A. A. Villanueva, J. A. del Alamo, T. Hisaka, K. Hayashi, and M. Somerville, "Degradation uniformity of RF-power GaAs PHEMTs under electrical stress," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 283–288, Jun. 2008, doi: 10.1109/TDMR.2008.920304.

[16] S. D. Gupta et al., "Positive threshold voltage shift in AlGaN/GaN HEMTs and E-mode operation by Al_xTi_{1-x} O based gate stack engineering," *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2544–2550, Jun. 2019, doi: 10.1109/TED.2019.2908960.

[17] S. D. Gupta, V. Joshi, R. R. Chaudhuri, and M. Shrivastava, "Part I: Physical insights into dynamic R_{ON} behavior and a unique time-dependent critical stress voltage in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5720–5727, Nov. 2021, doi: 10.1109/TED.2021.3109847.

[18] V. Joshi, S. P. Tiwari, and M. Shrivastava, "Part II: Proposals to independently engineer donor and acceptor trap concentrations in GaN buffer for ultrahigh breakdown AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 570–577, Jan. 2019, doi: 10.1109/TED.2018.2878787.

[19] V. Joshi, S. P. Tiwari, and M. Shrivastava, "Part I: Physical insight into carbon-doping-induced delayed avalanche action in GaN buffer in alGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 561–569, Jan. 2019, doi: 10.1109/TED.2018.2878770.

[20] V. Joshi, A. Soni, S. P. Tiwari, and M. Shrivastava, "A comprehensive computational modeling approach for AlGaN/GaN HEMTs," *IEEE Trans. Nanotechnol.*, vol. 15, no. 6, pp. 947–955, Nov. 2016, doi: 10.1109/TNANO.2016.2615645.

[21] N. Zagni et al., "'Hole redistribution' model explaining the thermally activated R_{ON} stress/recovery transients in carbon-doped AlGaN/GaN power MIS-HEMTs," *IEEE Trans. Electron Devices*, vol. 68, no. 2, pp. 697–703, Feb. 2021, doi: 10.1109/TED.2020.3045683.

[22] M. Denison et al., "Moving current filaments in integrated DMOS transistors under short-duration current stress," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1695–1703, Oct. 2004, doi: 10.1109/TED.2004.835978.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 22,2022 at 05:39:23 UTC from IEEE Xplore. Restrictions apply.