Effect of Source & Drain Side Abutting on the Low Current Filamentation in LDMOS-SCR Devices

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***Abstract*— The concept of abutting source/body and drain/anode junctions is studied in detail in a high voltage LDMOS-SCR with 2D and 3D TCAD simulations. The SCR turn-on and low current filament formation are strongly influenced by the isolation at the anode and cathode side in the LDMOS-SCR. While the anode side isolation impacts the filament-induced failures at low currents, the cathode side isolation has a minor impact. Physical insights are given on the SCR turn-on degradation with abutting and its influence on the filament formation and spreading. The obtained understanding helps to build an ESD robust, self-protected LDMOS-SCRs.**

I. Introduction

LDMOS/DeNMOS devices used in high voltage applications are prone to ESD failure due to space charge modulation (SCM) induced current filamentation at low current levels [1]. A self-protecting input/output driver can be designed by forming an SCR in the LDMOS [2]. This is generally done by implanting a p+ diffusion in the N-Well of the LDMOS. Most LDMOS designs have body diffusion a butted to the source to save the layout area and reduce the body resistance, which improves the SOA.

If the LDMOS layout is used for implementing the SCR, the same design strategy of abutting diffusion to the cathode and anode to save SCR layout area needs to be well thought out. Abutting affects the SCR strength of the resultant device severely. Another significant failure mechanism reported in LMDOS-SCR devices is low-current filament driven failure during snapback in these devices affecting their power scalability [3]-[4]. It has been shown previously that the severity of the power scalability issues is a strong function of the overall SCR strength. The importance of strong uniform SCR turn-on at low current levels has been highlighted for various system-level ESD protection applications [5]. While the effect of abutting on SCR strength has been reported in the literature, there isn't any work that gives insights into the underlying physics. In this work, this gap is addressed by developing physical insights into the working of LDMOS-SCR devices under different abutting configurations.

In this work, the TCAD setup used is the same as that used in our earlier publications [1][4][6]. Both 100ns and 1000ns TLP pulse widths are used to demonstrate and understand power-scalability issues in LDMOS-SCR. The rise time for either case (100ns and 1000ns) is kept at 10ns. This paper is arranged as follows. The second section describes the reference devices used and the variations of the reference devices explored as a function of abutting the contacts. In the third section, using detailed 2-D TCAD simulations, the SCR turn-on and the impact of abutting at the anode and cathode sides are discussed. In the fourth section, the 3-D TCAD simulations of LDMOS-SCR are discussed. Here, the turn-on and eventual low-current failure are described as a function of abutting at the anode and cathode contacts. Finally, this work is concluded by summarizing the key findings in the last section.

II. Device Under Test

Fig. 1(a) depicts the cross-section of an abutted LDMOS-SCR. The starting layout of abutting at cathode and anode sides reduces the layout area of the LDMOS devices. This is expected to improve the ESD robustness of the device. However, due to a low-current filament-driven failure, these devices exhibit a window failure effect during snapback (**Figs. 1(b)-(c)**) as reported in [3],[5]. The peak maximum lattice

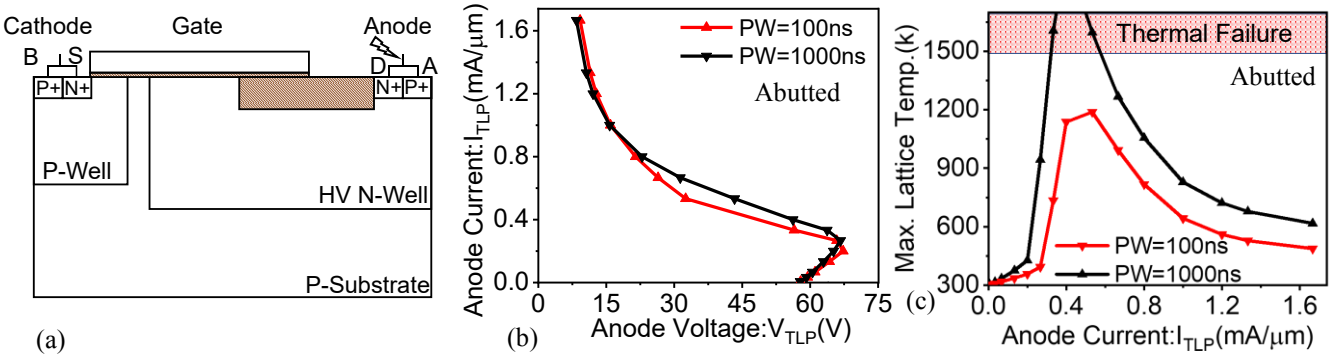

Fig. 1. (a) Cross-section of a 40V STI based abutted LDMOS SCR. (b) TLP-IV and (c) TLP-IT extracted from 3D TCAD simulations. Under longer pulse width, a window failure appears during snapback. Within the window failure, the injected current is not large enough cause an SCR turn-on. At larger injected currents, the SCR turns on, reducing the electric field within the hot spot and relaxing temperature within the hot spot [4],[5].

temperature attained is a function of pulse width. The collapse in failure current at longer pulse widths meant that the developed SCR no longer follows the Wunsch-bell curve. Since more Impact Ionization-generated carriers are available for bipolar turn-on at higher injected currents, these devices survive the high current regime. At this point, it's worth highlighting that the simulations in these devices were done only around the snapback region to probe into the window failure effect. Therefore, the lattice temperature will continue to increase at higher injected currents, and eventually, the device will fail at higher injected currents. **Figs. 2(a)-(c)** depicts the cross-sections of LDMOS-SCRs with isolation on the anode side (anode and drain), source side (source and body), and on both the anode and source sides. These variants of contact abutting are explored in this work to understand the effect of abutting on the SCR strength. Both 2-D and 3-D variants are discussed to understand the effect of butting. **Figs. 3(a), (b)** depict the TLP-IV graphs of LDMOS SCR with the three isolation combinations for a 100ns TLP pulse and a 1000ns TLP pulse, respectively. The increase in maximum lattice temperature still exists in the snapback phase (**Figs. 3(c), (d)**). However, the window failure is eliminated once the anode contacts are isolated from the drain. This difference in the impact of abutting on the anode and cathode sides on power scalability is discussed in the next section.

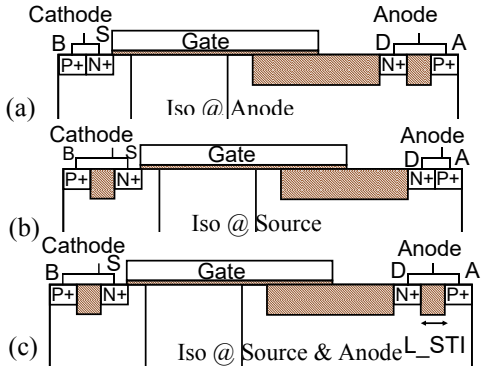

Fig. 2. Cross-section of STI-based LDMOS SCRs with (a) Isolation @ Anode (b) Isolation @ Source (c) Isolation @ Source & Anode.

III. Insights Into SCR Turn-on

The 3D TLP data (**Figs. 1(b)-(c)**) show very high lattice temperature in the abutted device compared to STI isolated designs. The negative differential resistance (NDR) caused by space charge modulation triggers current filament formation during snapback. This increases the current density within the filamentary region, resulting in a sharp rise in maximum lattice temperature. 2D-TCAD simulations are used to understand the impact of abutting on SCR turn-on independent of the current filament behaviour. The breakdown voltage decreases once the P+ anode diffusion is isolated (**Fig. 4(a)**). This is due to improved PNP strength in these devices resulting in an early vertical junction breakdown. The anode contact isolation reduces the peak temperature formed during snapback (**Fig. 4(b)**). In **Figs. 5(a)-(d)**, the hole current density in the N-Well is plotted as a function of different abutment configurations. **Fig. 4** and **Fig. 5** were extracted

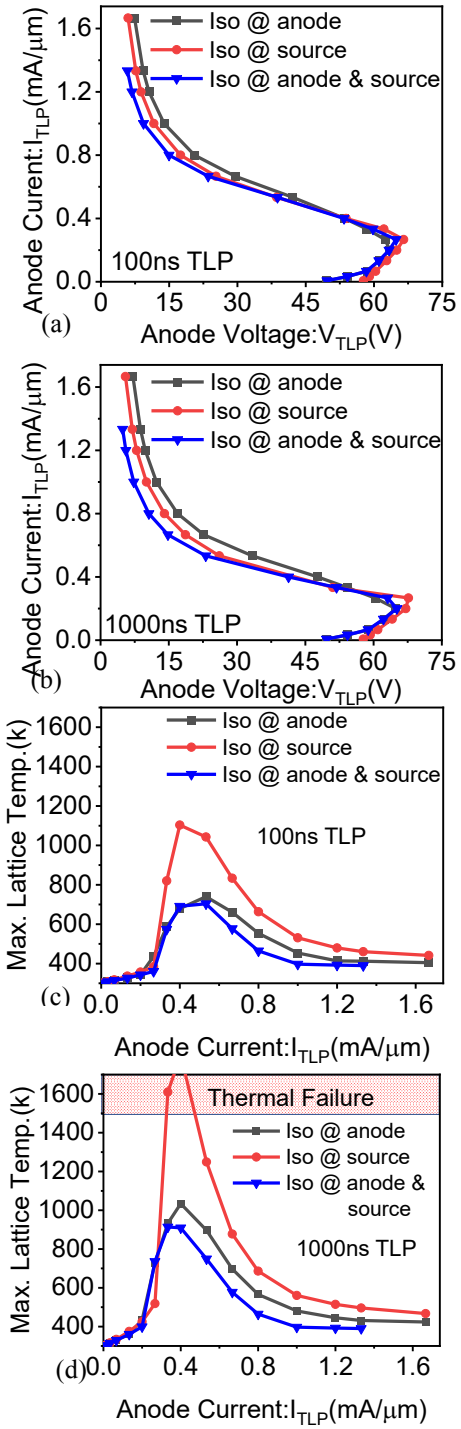

Fig. 3. TLP-IV from 3D TCAD simulations extracted for (a) 100 ns TLP and (b) 1000ns TLP. Maximum lattice temperature for (c) 100ns TLP and (d) 1000ns TLP. For longer pulse widths, the window failure effect is avoided once anode isolation is introduced. Source isolation does not seem to impact the window failure effect significantly.

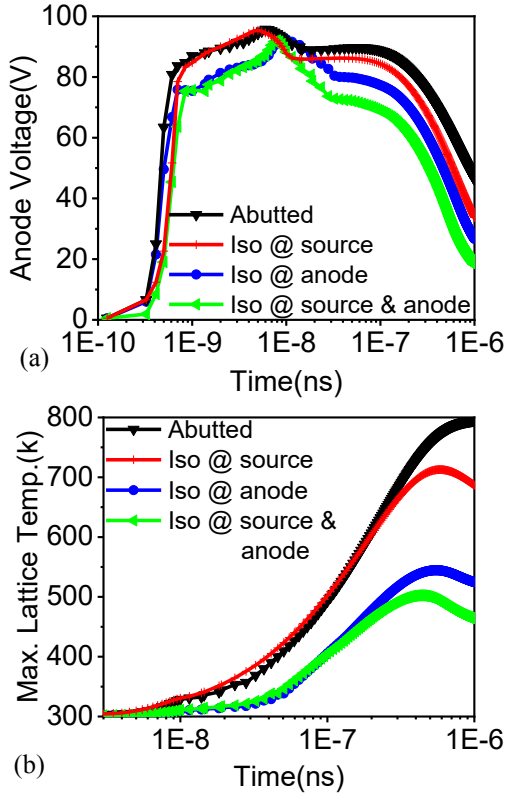

Fig. 4. (a) Transient anode voltage and (b) transient maximum lattice temperature in the device extracted from 2-D TCAD @ I_{TLP}=0.6 mA/um. Due to the stronger PNP strength there is an early breakdown once the anode side is isolated. This also improves over all SCR action resulting in a smaller increase in temperature.

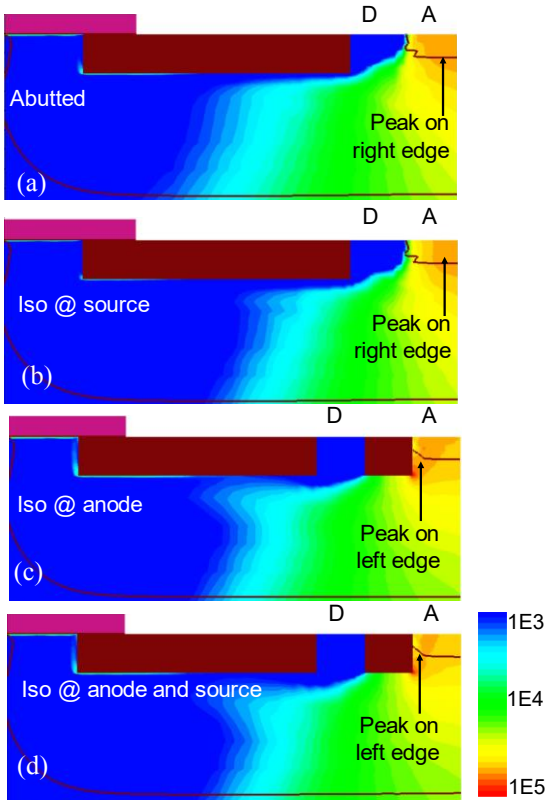

Fig. 5. Hole current density in the N-Well of LDMOS-SCR with (a) Abutted (b) Isolation @ source (c) Isolation @ anode (d)Isolation @ anode & source. Once the anode side is isolated the peak hole current density shifts from the right edge of the anode contact to the left edge. This shift could be attributed to either of the two reasons mentioned below. 1. Increased distance from the drain contact, decreasing the N-Well pick up efficacy or 2. The overlap of the highly doped N+ drain and P+ anode resulting in the left edge of the anode having a lighter P+ doping.

after snapback with injected current equal to the holing current and @ 100ns. Two important observations can be made from **Fig. 3**, **Fig. 4**, and **Fig. 5**.

1. Isolating anode side improves the SCR strength in LDMOS-SCR devices:

Once the anode contact is isolated, the N-Well pick up decreases since the distance between the P+ anode and the N+ drain (N-Well pick up) increases. This improves the PNP strength and, thereby, the overall SCR strength. Another

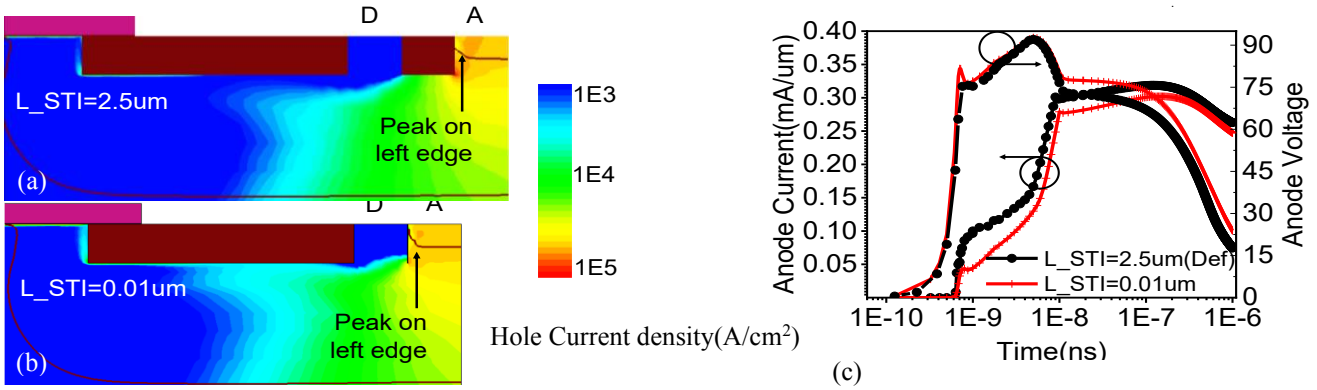

Fig. 6. Hole current density in the N-Well of an LDMOS-SCR with STI isolation distance @ anode of (a) 2.5um and (b) 0.01um. (c) Corresponding transient anode voltage and anode current in these devices. Despite having negligible STI-isolation, the peak hole current doesn't shift, indicating that the overlap of the highly doped P+ and N+ regions in the abutted device is the dominating effect for the shift in peak hole current density in the anode.

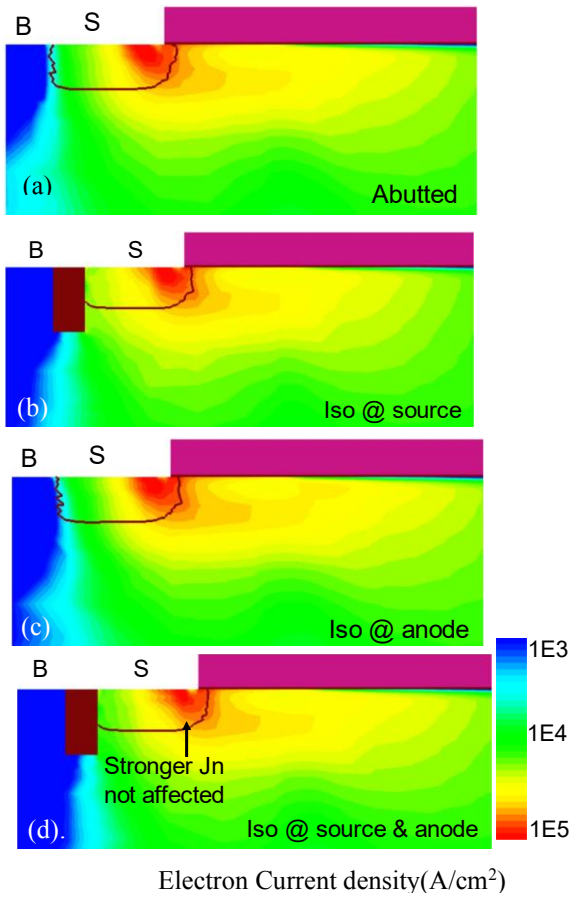

Fig. 7. Electron current density in the P-Well of LDMOS-SCR with (a) Abutting (b) Isolation @ Source (c) Isolation @ anode (d) Isolation @ source & anode. After source abutting, since the highly doped junction happens on the side of the contact that already carries lower distribution of the total source current, there is not any significant improvement in the SCR turn-on.

reason for this improvement is avoiding the high doped base junction formed when the STI is removed. Such a high doped base region degrades the overall PNP's bipolar strength.

2. Isolating anode side shifts the peak current density to the left edge of the anode contact:

This shift can be possibly attributed to two effects of anode isolation:

a). The increased distance between N-well pick-up and anode due to the STI region improves the bipolar action of the anode contact

b). The absence of the overlap of highly doped N+ drain and P+ anode results in a severely degraded base region associated with the bipolar on the left edge of the anode contact.

A device with an STI of 0.01 µm at the anode side is simulated to precisely probe the dominating effect of the above-mentioned physical mechanisms. Please note that the device with ultra-narrow STI is only considered to understand the underlying physics and is practically not feasible. There is not any significant difference in the location of the peak current density (**Fig. 6(a),(b)**) or the PNP efficiency (**Fig. 6(c)**). We can conclude that the absence of the abutted junction formed by the N+ drain and the P+ anode is the dominating effect for the shift in the peak hole current density. At this point, it is noteworthy to mention that while the peak current density is still at the right edge of the anode contact, the SCR strength in these ultra-thin STI degrades compared to the devices with regular STI. The N-Well pick-up increases due to the reduced distance between the P+ anode and the N+ drain, resulting in the SCR degradation.

When isolation at the source is introduced, the highly doped junction between the body and the source happens at the left side of the source contact. This side of the junction already carries a much smaller proportion of the total current(**Figs. 7(a)-(d)**) injected through the source contact. Therefore, the degradation of bipolar that happens at the junction of source and body contact has a much smaller impact on the bipolar strength. Due to this, having source-side isolation does not significantly improve the power scalability issue in the LDMOS-SCR. Therefore the source contact side in the LDMOS-SCR can be abutted to decrease the overall layout area of the device. It is noteworthy that while the impact of source-side butting might not offer any improvement in LDMOS-SCR, they can provide a significant improvement in HV-Junction SCR's. This is because in the case of HV-Junction SCR's, the body contact can be placed close to the well-junction, i.e. the source and body contacts can be swapped. In that case, the body-source contact junction can modulate the SCR strength. This could not be done in an LDMOS-SCR since the source must always be placed closer to the well-junction for the transistor to work properly.

IV. Current Filament Dynamics

3-D TCAD simulations have been used in this section to understand the turn-on and current filament dynamics in LDMOS-SCR as a function of anode or cathode side butting. Initially, after the junction breakdown, most of the injected current is through the N+ drain and the P+ body, which forms a reverse bias diode. At this point, the current density is uniform along the device width. As the injected current is further increased, the amount of impact ionization generated carriers available for bipolar turn-on increases. Once the bipolar is turned on, the number of majority-carriers injected in the respective wells increase. Once the concentration of injected majority carriers dominates the respective well's background doping, an NDR is observed. This NDR triggers a non-uniform current conduction state along the device's width, which is called a current filament [7]. The current filament formation results in a very high current density through a smaller section along the device's width. This has two significant effects on LDMOS-SCR devices. The first one is a sharp rise in the maximum lattice temperature since there is a sharp increase in current density within the filamentary region. This can be destructive if the electric field is not relaxed fast enough. The second one is the increased availability of impact ionization generated carriers to support bipolar turn-on and subsequent SCR turn-on. This SCR turn-on can relax the electric field within the filamentary region, relaxing the maximum lattice temperature. If the SCR turn-on doesn't happen fast enough after filament formation, the lattice temperature within the

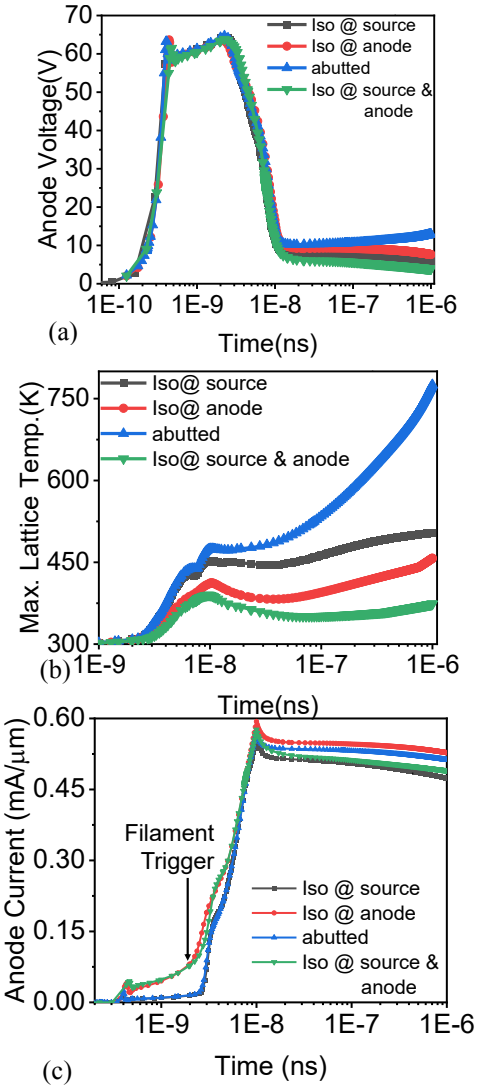

Fig. 8. 3D-TCAD simulated (a) transient anode voltage across the SCR (b) transient maximum lattice temperature and (c) transient anode current. The isolated source contact device seems to have a lower voltage @ saturation than the device with anode isolation. However, in the maximum lattice temperature plot the isolated source contact devices seem to have higher temperature. From the anode current plot, the filament trigger (/anode hole current) increases as soon as the anode is isolated. This is because once anode STI isolation is removed, the lateral PNP degrades and therefore, most of the injected hole current is forced through the vertical PNP.

filamented region increases rapidly, resulting in the device's failure.

The trends among the devices in various abutting configurations remain the same as that of the 2-D simulations (**Fig. 8(a), (b)**). However, the filament trigger happens first in devices with anode isolation (**Fig. 8(c)**). The filament in the LDMOS-SCR is triggered by SCM either in the N-Well or the

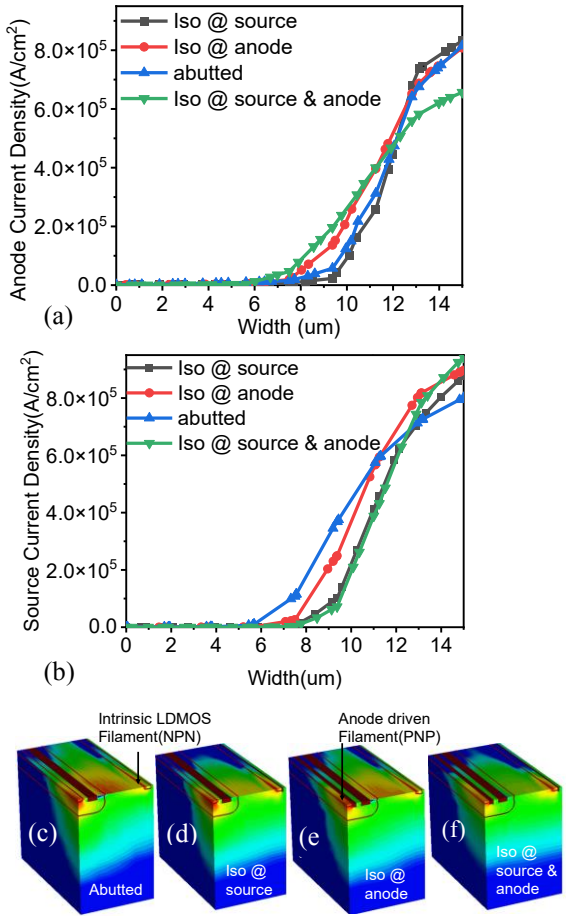

Fig. 9. Conduction current density extracted along the device width in (a) the source contact and (b) the anode contact. (c)-(f) Conduction current density contours @I_{TLP}=1.35mA/um. The intrinsic LDMOS filament is most severe in devices with isolation on both sides. This is because of the early SCR turn-on which results in the increased electron current conduction by the NPN (source).

P-Well. The high anode current in devices with anode isolation increases the P-Well hole current density, which results in SCM and, therefore, early filamentation. While early filamentation can result in low current filament-driven failure in LDMOS devices, it provides more time for the SCR turn-on to happen in LDMOS-SCR devices. This further improves the window failure in these devices. The anode triggered filament is more relaxed (**Figs. 9(c)-(f)**) in anode isolated devices due to high anode hole current injection resulting in an early bipolar turn-on (**Fig. 9(a)**) and, therefore, faster filament spreading. The intrinsic LDMOS filament is most severe (**Fig. 9(b)**) in devices without source isolation because of increased electron current injection by the NPN (source to drain).

V. Conclusions

Abutting source/body and drain/anode junctions in LDMOS-SCRs degrades the SCR action at low current levels. This severe SCR degradation worsens the device's power scalability. Anode isolation was found to restore the SCR action

significantly. This improvement is due to the increased anode to drain contact distance reducing the N-well pickup resulting in an improved PNP action. Furthermore, the absence of a high doped base-emitter junction (Between the N+ drain and P+ anode) further strengthens the PNP. These two effects improve the PNP strength and, therefore, the overall SCR strength. Another impact of introducing STI is the shift of peak anode current density to the left edge of the anode contact. This was found to be due to the absence of a high doped base-emitter junction which degraded the bipolar efficiency associated with the left edge of the anode contact. Source isolation did not significantly improve the SCR strength since the abutment happens at the edge of the source contact carrying a much lower current. Early filamentation triggered by higher hole current in anode isolated devices was found to improve their power scalability performance. The severity of the intrinsic LDMOS filament and the anode-triggered filament was found to be a function of abutting. This work can be extended to any HV SCR device since the field plate action by the gate does not affect the abutted junctions.

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