HV-LDMOS Device Engineering Insights for Moving Current Filament to Enhance ESD Robustness

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***Abstract*— In this article, a novel design approach for improving electrostatic discharge (ESD) robustness of high-voltage laterally double-diffused MOS (LDMOS) devices is presented using detailed 3-D TCAD simulations. The proposed method considers engineering both static filament and dynamic/moving current filaments in LDMOS design. Physical insights and engineering approaches for moving filaments at higher stress current levels are presented. Dynamic filament motion and its relation to n-p-n turn-on engineering with an optimum p-well profile and substrate biasing are revealed. A unique window failure in LDMOS near snapback is discussed for the first time. A detailed analysis is presented on filament width engineering by using optimum drain diffusion length (DL) and its influence on static filament-induced window failures. This approach resulted in ten-time improvement in ESD robustness for self-protecting concepts. Finally, different fundamental questions related to the origin of filament motion are explored (using 3-D TCAD) with the help of engineered LDMOS Designs.**

***Index Terms*— Current filaments, electrostatic discharge (ESD), laterally double-diffused MOS (LDMOS).**

I. Introduction

THE laterally double-diffused MOS (LDMOS) devices are vital for building various systems on chips (SoC). LDMOS devices are critical elements in implementing high-voltage functionalities in different automotive applications. High-voltage input–output (I/O) drivers in SoC can get exposed to various electrostatic discharge (ESD) events often during manufacturing, packaging, and assembly at the board level [1], [2]. High-voltage LDMOS drivers must be protected against component-level ESD events, such as human body model (HBM) and charge device model (CDM). While the component-level ESD events (HBM and CDM) occur in the ESD controlled environments, system-level International Electrotechnical Commission (IEC) ESD events occur at uncontrolled environments in the end-user application with discharge currents up to 20–30 A [3].

However, high-voltage LDMOS I/O devices were found to be vulnerable against ESD stress [4]–[6]. High charge modulation effects were found to cause device failure at a significantly lower current level during ESD events [6]. Very low ESD failure current requires a larger footprint to provide sufficient protection against ESD. Especially in automotive ICs, where the on-chip ESD protection levels are significantly high, the protection area becomes a concern. This will also substantially impact the capacitance budget of I/O pins and signal loss during the chip's normal functioning. Various high-voltage device options, such as LDMOS-SCR [7], [8] and bidirectional HV-SCR [9], can be used as standalone ESD protection devices providing high it2. However, these devices require additional silicon area for protection. Though they are compact with very high It2, different triggering circuits and their sensitivity to signaling speeds on the protection pins make it challenging. To add to latch-up problem, recently, the power scalability under long-duration pulses was also found to be a design concern [9], [10]. Hence, a self-protection design with LDMOS failing at high It2 levels is still a better solution.

Achieving self-protection I/O with LDMOS is challenging. It is widely reported that LDMOS fails at the onset of voltage snapback is due to nonuniform current conduction/static filament formation [6]. There were efforts to improve the ESD robustness of LDMOS primarily focused on engineering the static filament. Drain engineering has been the central area of research in LDMOS ESD. For example, in [11], drain diffusion length (DL) increased to reduce the current density inside the n-well. It pushes the onset of current filament formation to high current levels, and a 5× improvement in it2 is obtained. Highly doped n-wells are proposed in [12]. This will increase the current level at which space charge modulation (SCM) occurs, hence the filament formation. However, this will compromise breakdown voltage. The silicide blocking technique is studied first in LDMOS in [13]. Selective drain-side silicide blocking was found to increase the failure current with safe snapback [13]. However, the silicide blocking length required to obtain a high failure current is very high and impractical. The source-side layout was also engineered in [14] and drain contact layout to achieve safe snapback and higher failure current.

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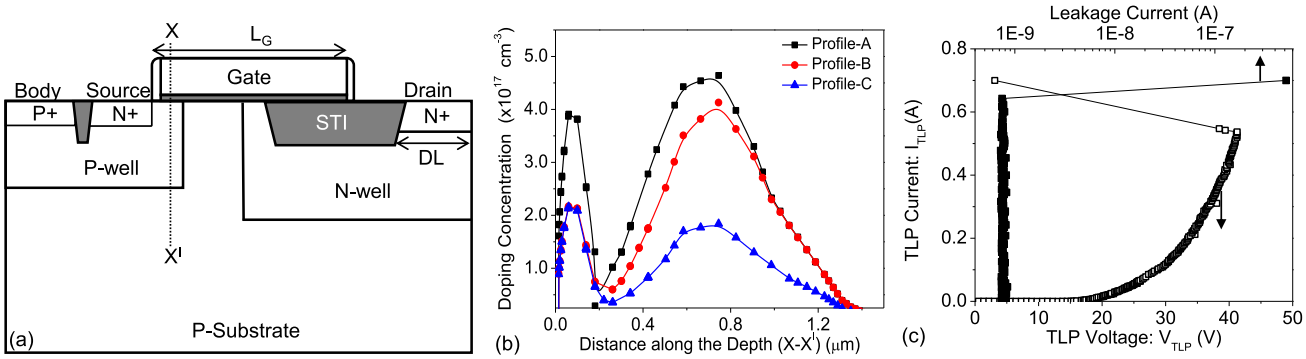

Fig. 1. (a) Cross-sectional view of high-voltage LDMOS. (b) Doping profiles of different p-wells in LDMOS under study. Note: X-axis of the plot represents the XX' line of the cross section in (a), starting from the silicon surface. (c) Measured TLP I–V characteristics of typical LDMOS (pulse width (PW) = 100 ns). Inset: leakage current as a function stress current. Typical LDMOS devices fail at the onset of voltage snapback and provide a very low ESD failure current.

On the other hand, the current filament motion was first studied in [15], in drain extended NMOS (DeNMOS) devices. It is found that filament motion before static filament induces localized failures can mitigate the device failure, and high failure current can be achieved [15]. The experimental demonstration of moving current filaments is mostly on vertical drain extended MOS (DMOS) devices [16], with few designs establishing optimum buried layer doping versus filament motion [17]. A new design for obtaining moving current filament in lateral DeNMOS was also presented for the first time in [18]. However, a detailed approach for combining both the static and dynamic current filaments engineering, particularly in lateral LDMOS designs, is still unexplored. Using 3-D TCAD simulations, this work tries to provide insights into the critical design knobs to engineer the static and dynamic filament formation in the LDMOS. The static filament engineering pushes the onset of filamentation, while dynamic filament pushes the failure limit beyond static filament failure limits. This work, an extension of [19], attempts to fill this gap to develop LDMOS design guidelines using a 3-D TCAD-based approach to achieve moving filaments.

II. 3-D Simulation Approach and Devices Under Test

A. TCAD Simulation Strategy

High-voltage LDMOS device is simulated using the Sentarus 3-D Technology Computer-Aided Design (TCAD) tool, with 100-ns pulse stress condition. A well-calibrated, 3-D TCAD simulations approach established in [4] and [18] is borrowed in this work to explore the high current behavior of LDMOS. Electrothermal 3-D device simulation solves drift-diffusion transport along with temperature equations. Various physical models to capture the avalanche process and electric field-dependent electron and hole mobility degradation along with different carrier recombination processes (Shockley–Read–Hall (SRH) and auger) are included. Proper electrical and thermal boundary conditions are defined. Device voltage response for the constant current pulse is averaged between 60% and 90% of the pulse duration to obtain a single data point of the transmission line pulse (TLP) I–V characteristics.

B. Different LDMOS Designs Under Test

LDMOS device cross section used for different filament studies is shown in Fig. 1(a). Various design parameters are changed to tweak the LDMOS device behavior under ESD by keeping the basic construct same. Such a device design aims to engineer the static and dynamic current filaments and understand various physical knobs associated with them.

The current filament in the LDMOS device refers to nonuniform current conduction at one of the device edges along its width [4]. Localized current conduction increases the lattice temperature inside the filament region. If the maximum temperature exceeds the critical temperature and the current filament is standing still at one edge until it causes device failure, such filaments are called static filament. When filament starts moving along device width, before lattice temperature reaches a critical value, filament behavior is characterized by the dynamic current filament. Please note that detailed physics behind the static and dynamic filaments is given later in this article (Section IV).

This article uses drain engineering to engineer static filament behavior, whereas dynamic filaments are obtained by tweaking the inherent bipolar (n-p-n) action present in LDMOS. Table I summarizes different design parameters changed/tweaked to engineer the LDMOS in each device type. Type-I is a reference component. Type-II is designed to target stronger inherent n-p-n turn-on. The p-well (base of lateral bipolar) is made more resistive, and substrate potential is raised only during ESD events. Type-III is designed to enhance n-p-n turn-on further by making p-well more resistive, and drain engineering is also employed with DL increment. The higher resistive p-well doping profiles used in Type-II and Type-III designs are shown in Fig. 1(b). It is to mention that the practical implementation of substrate biasing during ESD strike in LDMOS/DeMOS devices was discussed and implemented in [5].

Fig. 1(c) shows the typical LDMOS device failure at the onset of voltage snapback in the measured TLP I–V characteristics. An abrupt jump in leakage current, measured after every pulse, illustrates the device failure. It is worth mentioning that, though the experimental data represents an LDMOS device

TABLE I
SUMMARY OF DIFFERENT DEVICES TYPES USED IN THIS WORK TO STUDY THE FILAMENT MOTION

Simulated Device	P-well Dop.	Sub. Biasing	DL
Type-I	Profile-A	0 V	Minimum
Type-II	Profile-B	0.4 V	Minimum
Type-III	Profile-C	0.4 V	5*Minimum

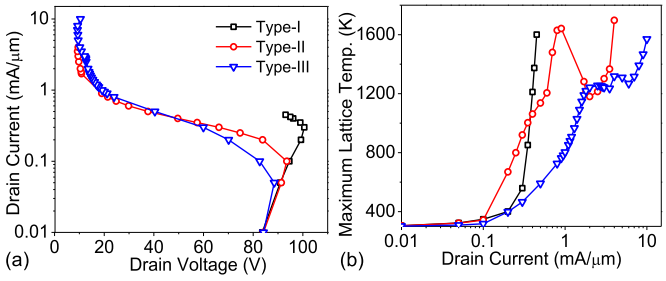

Fig. 2. (a) 3-D TCAD simulated TLP I–V characteristics of different LDMOS devices under investigations. (b) Maximum lattice temperature plotted as a function of TLP current.

of different voltage class, failure is LDMOS at the onset of voltage snapback, which is universally reported in most studies [6] unless any engineering is done to mitigate the static filament [13].

III. ESD BEHAVIOR OF DIFFERENT LDMOS DESIGNS

ESD behavior and analysis of device characteristics for three different designs, particularly designed to engineer the static and dynamic filaments, are presented. Table I shows the difference in each design, i.e., differences in p-well profiles and substrate biasing and drain length.

Fig. 2 shows the TLP I–V characteristics of three different LDMOS device designs. Type-I design is LDMOS with p-well Profile-A, without any filament engineering techniques. Type-I is the reference design (baseline component) for all the ESD investigations further. It is observed that, from TLP characteristics in Fig. 2, voltage and current increase beyond the onset of device breakdown, and the device experiences a voltage snapback. Lattice temperature found increases abruptly at the onset of voltage snapback, as shown in Fig. 2(b). This induces device failure at very low current levels in the Type-I device, hence poor ESD robustness. It is worth mentioning that the observed failure at onset of voltage snapback is in accordance with the literature and measurement data shown in Fig. 1.

In Type-II design, Profile-B is used for p-well and substrate biasing (V_{sub}) of 0.4 V is applied. The simulated (3-D) TLP characteristics of Type-II LDMOS design, as shown in Fig. 2(a), shows a unique behavior. The following observations are made from the TLP I–V: 1) the breakdown voltage of Type-II engineered LDMOS design remains the same as Type-I; 2) device snaps back at lower current (It1); and 3) lattice temperature increases until a critical value at first. However, if stressed further with higher current, lattice temperature decreased above a certain injected current, as shown in Fig. 2(b). The maximum temperature in this device during voltage snapback can be as high as silicon melting temperature, making this device vulnerable to failure near snapback. This critical temperature level exists in the device for a window of current levels near snapback, while it gets reduced beyond this window. In summary, designed Type-II LDMOS is vulnerable for ESD failures for a window of currents near the snapback; however, it survives higher current levels during TLP. Such unique device behavior observed in Type-II design using the 3-D TCAD analysis has practical significance and was never explored in the past. The similar vulnerability of device failure for current near snapback was experimentally demonstrated in [20]. It was also demonstrated that by skipping the vulnerable failure current window near the snapback (using a different load line TLP systems), the device can survive high currents. However, it is worth mentioning here that the physical mechanism for device survival at higher currents in the Type-II LDMOS device (in this work) is entirely different from what was observed in LDMOS-SCR in [20]. The physics of device survival at higher current levels in Type-II design is discussed later in this article. In addition, the weakness of device failure near the snapback observed for long-duration pulse discharges (beyond 100 ns) in LDMOS-SCR [20], and however, in Type-II LDMOS, such weakness is evident for sub-100-ns pulses.

In the Type-III device, drain engineering (5× increases in DL) is employed along with p-well profile-C, $V_{sub} = 0.4$ V applied during ESD stress. The following observations are made from the TLP I–V characteristics of Type-III design from Fig. 2: 1) drain voltage starts to snapback at lower current than Type-II; 2) maximum lattice temperature was found to be lower than Type-II and is below the critical failure temperature value; and 3) the final it2 also increases by shifting the thermal failure limits. The Type-III design depicts a 10× improvement in It2.

IV. STATIC VERSUS MOVING FILAMENT ENGINEERING

Drain engineering, reducing p-well doping, and pulling up p-well potential are done in Type-II and Type-III designs for engineering the failure limits associated with static and dynamic filaments. The physics of failure in each design is studied at different injected current levels.

A. Static Filaments

1) Filament-Induced Failures in Type-I Design: As shown in Fig. 2, Type-I design fails with an abrupt rise in lattice temperature, attributed to static filament formation [Fig. 3(b)]. ESD physics of LDMOS at different injection levels and physics of static filament formation are studied extensively in [6]. Various physical events present before the onset of snapback are summarized here for completeness. At the low injection current levels, junction breakdown dominates device conduction. Electron–hole pairs are generated during the avalanche multiplication process at the n-well junction. Generated electrons are collected at n-well contact, and holes

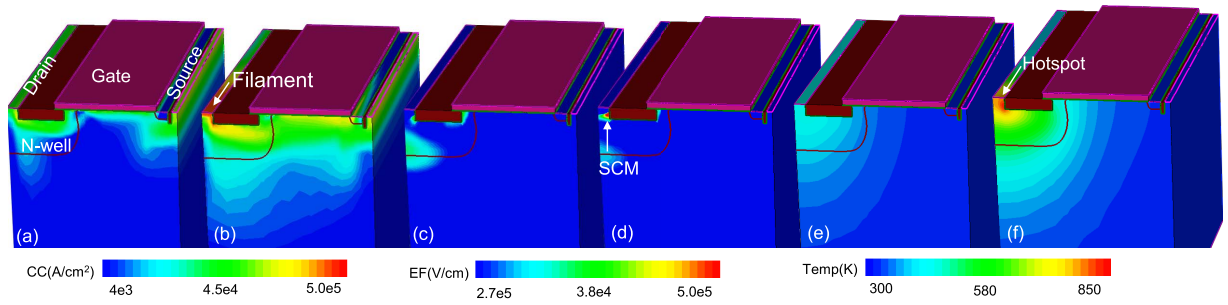

Fig. 3. (a) and (b) Conduction current density (A/cm^2), (c) and (d) electric field (V/cm), and (e) and (f) lattice temperature (K) in LDMOS before and at the onset of filament formation. Nonuniform SCM at the N+ drain contact causes filament formation and voltage snapback.

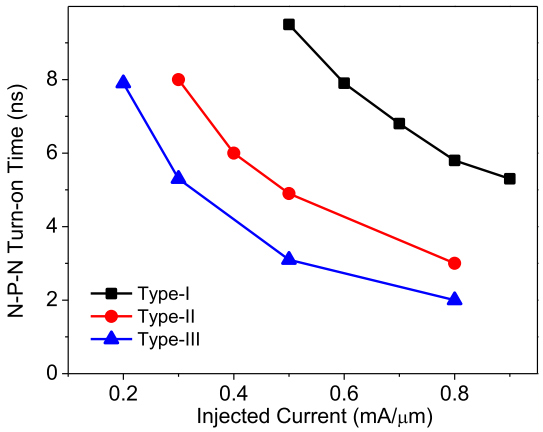

Fig. 4. N-p-n turn-on times for investigated devices. Faster n-p-n turn-on, with larger DL in Type-III device, yields larger failure current.

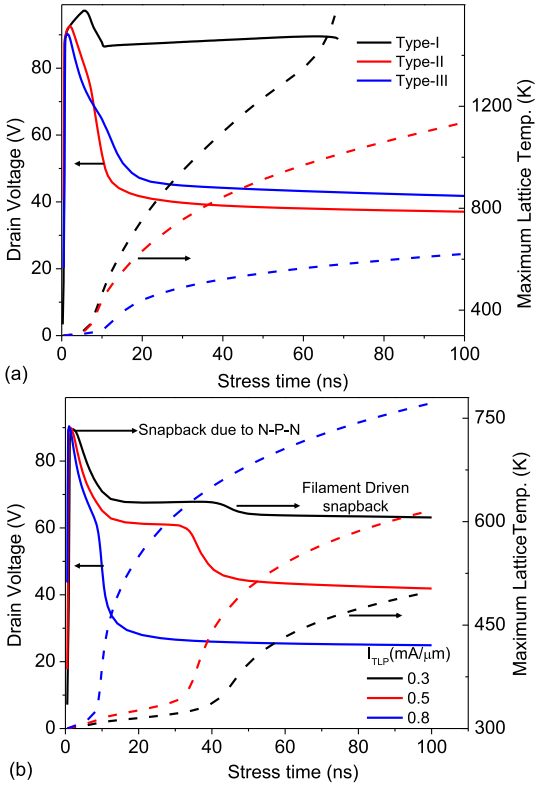

Fig. 5. (a) Drain voltage and maximum lattice temperature of different design types at a given inject current (0.6 mA/μm) near the snapback. (b) Drain voltage and lattice temperature of Type-III device at different current levels.

would travel through the lightly doped substrate region and collected at P+ pickup via p-well. This raises localized p-well potential near N+ source to forward bias the source and p-well diode and, hence, n-p-n turn-on. When the excess electron population in the n-well (injected due to n-p-n turn-on) exceeds the background doping concentration, the SCM condition is reached. Peak electric field will now be shifted from n-well junction toward N+ contact. The 3-D static current filament formation in the LDMOS device is attributed to nonuniform SCM, which shifts the peak electric field under N+ drain region as shown in Fig. 3(d), eventual filament formation, and hotspot formation [Fig. 3(f)] to cause device failure.

2) Static Filaments in Type-II and Type-III: Engineered designs show early voltage snapback in TLP characteristics, as shown in Fig. 2, attributed to improved lateral bipolar turn-on efficiency. Reduction in p-well doping in Type-II and III designs increases p-well resistance. Larger p-well resistance requires lower avalanche-induced current to forward bias source diode. In addition to increased p-well resistance, positive substrate biasing causes early turn-on of the source diode and deeper current conduction. The n-p-n turn-on time plotted as a function of injected current for different designs is shown in Fig. 4. The improved n-p-n turn-on time as a function of the injected current is seen from Type-I to Type-III. Transient data in Fig. 5(a) at the same current (close to snapback region) show a deeper snapback, and lower lattice temperature in engineered designs is compared to the reference structure. It is also worth highlighting that the snapback in engineered devices results from both n-p-n and nonuniform SCM-induced static filament formation. In Fig. 5(b), drain voltage and lattice temperature are plotted for different current levels in the Type-III design. Two-stage snapback can be seen at low current levels (0.3 and 0.5 mA). First, snapback is attributed to n-p-n turn-on and second snapback is due to filament formation. The second snapback is found to coincide with the rise in lattice temperature due to filament formation. These data further highlight that filament formation in LDMOS is not due to bipolar turn-on.

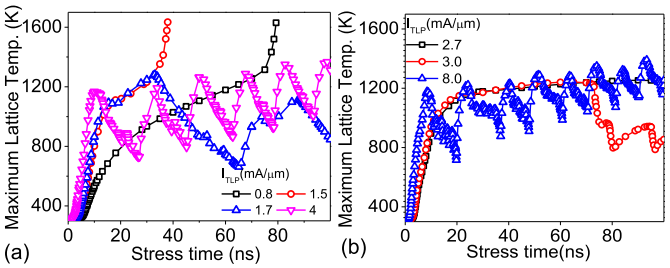

Fig. 6. Transient temperature for different injected currents. (a) Type-II and (b) Type-III devices. The oscillations in lattice temperature at higher injected current cause the device to survive higher currents.

Fig. 6(a) shows the maximum temperature inside the silicon volume as a function of time for the current level beyond snapback and holding state in Type-II. At an injection current of 0.8 mA/μm, device temperature increases abruptly until the device failure. Such a temperature rise is attributed to hotspot formation due to static filament formation. With the further rise in injected current (1.5 mA/μm), time for the filament to form reduces. Accelerated static filament-induced failure can be seen in a window of currents in the Type-II device. Fig. 7(a) and (d) shows the conduction current and lattice temperature in the Type-II device near Point A in the temperature versus current characteristics. The static filament-induced hotspot and temperature reaching the critical levels can be seen in Type-II.

Due to reduced current density in the n-well attributed to larger DL, the Type-III design pushes the onset of SCM to higher injected currents [6]. Lattice temperature response for an injection current of 2.7 mA/μm in Fig. 6(b) does not peak to critical value despite the static filament. Fig. 8(a) and (d) shows the conduction current and lattice temperature in the Type-III device near Point A in the temperature versus current characteristics. Despite SCM-induced filament formation, the Type-III device shows a relaxed temperature [Fig. 8(d)] as the current density inside the hotspot underneath N+ is lowered.

B. Dynamic Filaments

1) Type-II: When the lattice is observed at high current levels above the holding state, Type-II and Type-III show oscillations, as shown in Fig. 6. These damped oscillations ensure that lattice temperature does not cause device failure. At high current levels, the device survives after a window of currents in the Type-II design. The zigzag temperature changes in Fig. 6(a) are attributed to moving current filaments at higher injected currents. Current filament motion in the engineered Type-II device is seen from Fig. 7. Fig. 7 shows the current density and lattice temperature of Type-II design captured at three points (A, B, and C) in the current versus maximum temperature plot. Points A, B, and C are highlighted. At Point A, static filament-induced failure can be seen in the Type-II design (the previous section). At Point B, filament motion can be observed, as shown in Fig. 7(b). Filament motion from one edge of the device to another edge causes reduced hotspot strength Fig. 7(e). It is also observed that peaks in temperature versus time curve, in Fig. 6(a), correspond to hotspot location at one of the edges. The crux is when the filament reached almost in the center of the device, and the hotspot gets relaxed. The current filament motion is due to the negative temperature sensitivity of the impact ionization rate [8]. The higher localized temperature inside the filament reduces the impact ionization rate. Stronger bipolar action because of the adapted engineering techniques in Type-II and higher impact ionization rate turn-on the parasitic n-p-n next to filament location. This leads to the filament motion. When the filament starts moving from one edge to another edge, the device's average temperature increases with time. Finally, Point C lattice temperature in the moving filament reaches the thermal failure limit and eventual failure.

2) Type-III: The Type-III device was also found to show filament motion, as depicted with oscillations in device temperature in Fig. 6(b). However, filament motion is found to start at higher injected current levels than the Type-II device. Conduction current and lattice temperature are probed in Type-III design at different current levels (A, B, and C), as shown in Fig. 8. The static filament does not cause device failure in Type-III design, as the hotspot is weaker attributed to reduced current density in the filament with increased DL [Fig. 8(a) and (d)]. Moving filaments take over the current conduction at higher current values [Fig. 8(b) and (e)]. Despite moving filaments, the average temperature continues to increase for all higher current levels and eventually causes thermal failure in the device at Point C [Fig. 8(c) and (f)].

In summary, the Type-I device (reference device) fails since static filaments at the onset of voltage snapback provide small failure currents. Though the engineered Type-II fails due to the static filament formation in a window of current near the snapback, the p-well engineering and substrate biasing effects cause the device in Type-II to survive higher current levels by enhancing the n-p-n action and filament motion. The Type-III device mitigates this device failure window due to the static filament with increasing DL and reducing the hotspot strength during static filament formation. It is worth highlighting that the ramp rate for substrate biasing is critical to achieving the first current filament motion. The circuit design for the substrate pull-up circuit should ensure that the ramp rate is not too slow. There should be enough substrate potential (0.4 V in this design) during the first 10–15 ns of ESD pulse ramp.

V. New Insights on Filament Motion

Though different works in the past have experimentally demonstrated the filament motion and explained filament motion in high-voltage devices, few open questions still exist regarding current filament movement and its origin. There is a great deal of confidence established on 3-D TCAD in understanding high-voltage LDMOS physics under high current conditions in recent years. Explorations and observations in the previous section related to n-p-n engineering and drain engineering bring us to the fundamental question pertaining to filament motion.

A. What Triggers the Filament Motion in LDMOS?

Fig. 9(a) shows the transient lattice maximum temperature plotted for two different injected currents in the Type-II design.

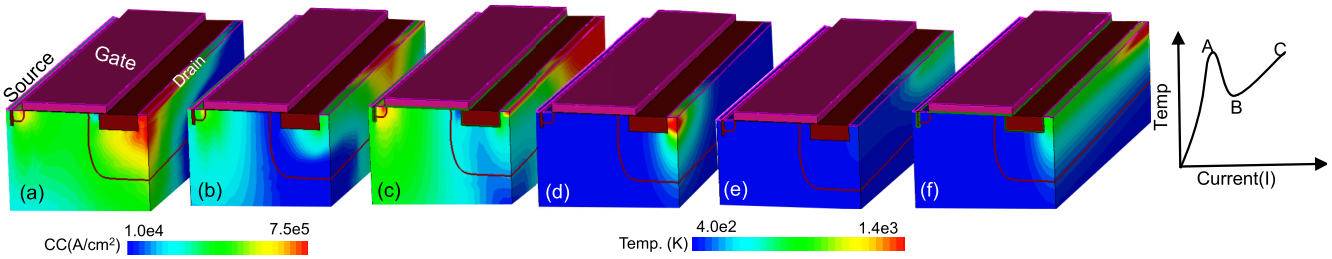

Fig. 7. (a)–(c) Conduction current density (A/cm^2) and (d)–(f) lattice temperature (K) at A, B, and C shown in the inset for Type-II device. At A, the static filament causes device failure. If stressed further at B, the filament motion mitigates the heating. The device conducts safely until C, where it fails because of excess heating.

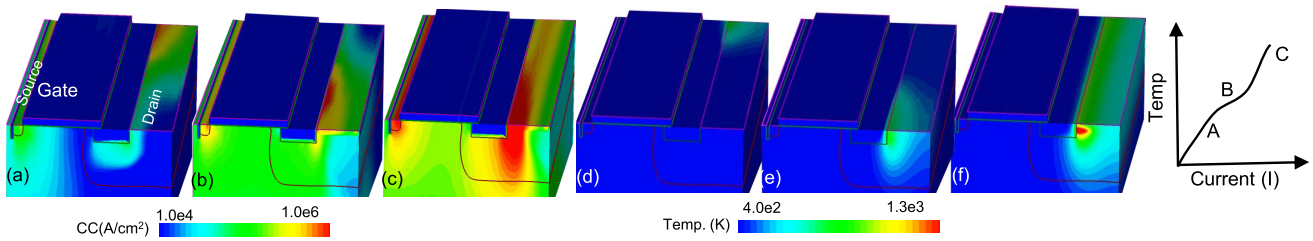

Fig. 8. (a)–(c) Conduction current density (A/cm^2) and (d)–(f) lattice temperature (K) at A, B, and C shown in the inset for Type-III device. A larger DL reduces the current density in the hot spot region at A, and the device survives failure. At B, filament starts moving, and the device survives until very high currents.

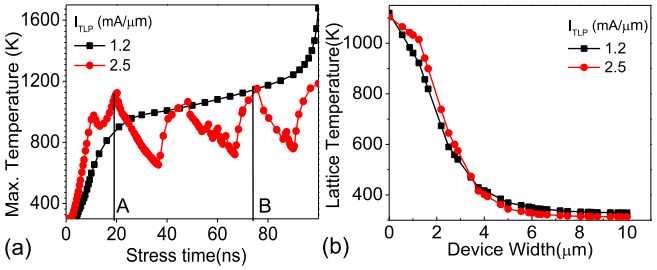

Fig. 9. (a) Transient temperature in Type-II device at a given injected current levels. (b) Temperature plotted at two different instances of times A and B shown in (a). A larger temperature gradient causes filament motion at higher current.

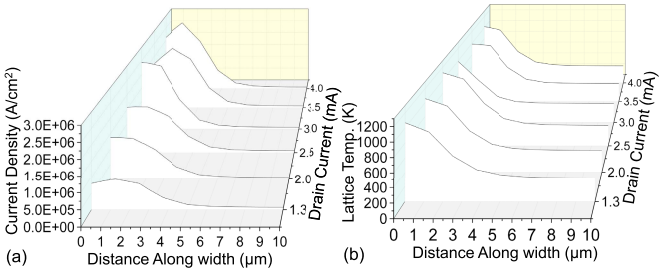

Fig. 10. (a) Conduction current density (A/cm^2) and (b) lattice temperature (K) along device width for different injected currents, extracted at the onset of filament motion.

For I_{TLP} of 1.2 mA/μm, filament motion is not seen. Static filament causes device failure. However, for I_{TLP} of 2.5 mA/μm, filament motion causes oscillations in lattice temperature and ensures safe device operation. Lattice temperature profiles are plotted along device width in Fig. 9(b) at two different time instances noted as A and B in Fig. 9(a) at different current levels. Point A denotes the onset of filament motion at higher current ($I_{\mathrm{TLP}} = 2.5$ mA/μm), and Point B is where the same peak temperature is observed but for a lower current ($I_{\mathrm{TLP}} = 1.2$ mA/μm). It is observed that in both cases, though the peak temperature is the same, filament motion is only seen at a higher current, where the temperature gradient is more elevated. A larger temperature gradient observed at the onset of filament motion indicates temperature gradient as the driving factor for the filament to move, not the peak temperature in the filament.

Furthermore, conduction current density and lattice temperature along device width at the onset of current filament motion (at different time instances for each current) are plotted for different injected currents in Fig. 10. It can be observed that, though the current density inside the filament is different, a similar temperature gradient can be seen at the onset of filament motion for various current levels. This confirms that filament starts to move when a certain temperature gradient is reached but not when a certain current density inside the filament. It is worth mentioning that the extracted temperature profiles and current densities in Fig. 10 correspond to the first instant of filament motion for a given stress level. It is also observed that with an increase in injected current, early onset of first filament motion is seen. The gradient in the lattice temperature reaches the critical value at a lower time scale, with a higher injection rate (larger dI/dt). As shown in Fig. 6(a) for Type-II, the first filament motion occurred around 30 ns for I_{TLP} of 1.7 mA/μm, whereas for I_{TLP} of 4 mA/μm, filament motion occurred in the sub-10-ns range.

B. Temperature Gradient Required for Filament Motion a Constant Value?

Another question to address is that if the temperature gradient is required for the filament to move, are there constant values? If not, what factors make it a variable?

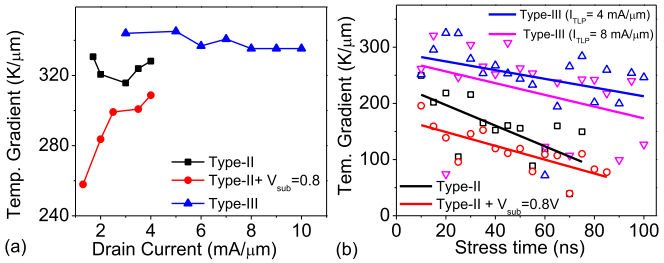

Fig. 11. (a) Temperature gradient required for filament motion as a function of injected current for different LDMOS designs under investigation (n-p-n strength). (b) Temperature gradient required for filament motion as a function of time at the same injected current but different n-p-n strengths.

1) Bipolar Action and Heat Dissipation: From the investigations on Type-II and III designs, it is observed that the temperature gradient required for first filament motion is not constant. It is a function of n-p-n strength and thermal heat dissipation inside the device. Fig. 11 shows the temperature gradient extracted as a function of injected current but for different device designs. Type-II designs with various substrate biasing are compared. This is done to compare different bipolar actions keeping the LDMOS geometry the same. The Type-III device has different heat dissipation inside the device (difference in geometry with larger DL). It is observed that stronger n-p-n (higher V_{sub}) requires a lower temperature gradient for filament motion, as shown in Fig. 11. However, with similar n-p-n strength, the Type-III design needs a larger gradient than the Type-II design. However, the temperature gradient required remains constant for different injected currents for different designs.

2) Stress Time?: The other fundamental question regarding the filament motion is, does the temperature gradient required for motion increase or decrease once the filament starts moving during the same pulse? It is observed that, once filament starts moving at a given injected current, the gradient required for filament motion also reduces, as shown in Fig. 11(b). As the heat accumulation occurs inside the silicon volume, each time filament moves through a point of cross section, the gradient required for motion gets reduced with time for a given pulse. The same trend is verified at different n-p-n strengths in the Type-II and Type-III designs, where the heat dissipation is different. It is found that the temperature gradient required for consecutive filament motion is smaller once the filament starts moving across different designs.

In summary, filament motion is triggered by the temperature gradient inside the filament along device width. However, it does not depend on peak temperature/current density inside the filament. The gradient required for first filament motion is also a function of n-p-n strength and heat dissipation (geometry of the device). Stronger n-p-n requires a lower gradient, whereas relaxed heating inside the device requires more temperature gradient. The gradient reduces as a function of time once the filament starts moving from one edge to other another edge.

Though a temperature gradient triggers filament motion, the process of filament motion is explained through the negative

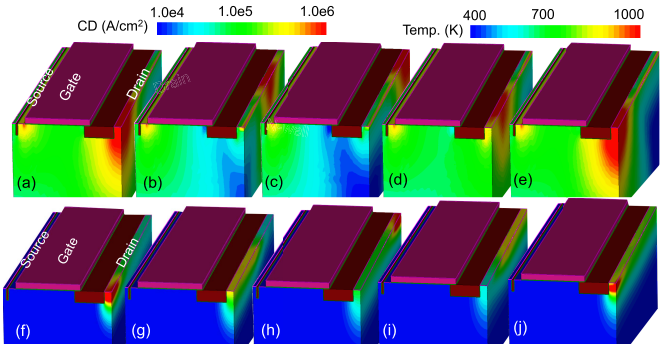

Fig. 12. (a)–(e) Current density (A/cm^2) and (f)–(j) lattice temperature (K) for an injected current of (3 mA/μm). For currents beyond the observed failure window in Type-II device, moving current filaments is observed from one edge to another.

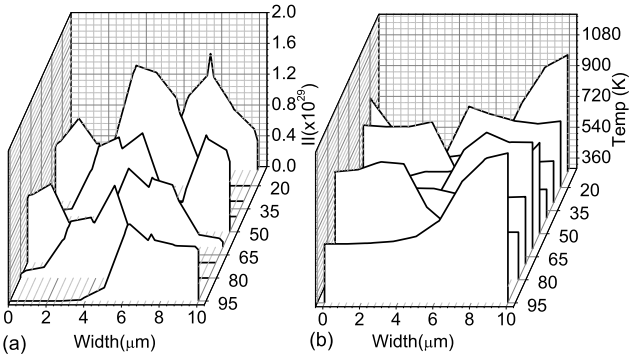

Fig. 13. (a) Impact ionization (II) and (b) lattice temperature at an injected current of 3 mA/μm as a function of stress time.

coefficient of impact ionization (II) with temperature [15], [16]. When the temperature gradient reaches a critical value (this value is found to change as a function of n-p-n strength, heat dissipation inside the device as mentioned in the previous section), reduction in impact ionization inside filament is high. Impact ionization at the edge of filament becomes more than II inside the filament. If the lateral bipolar is strong, it will start to turn on and conduct the current in the nonfilament region. Filament moves from one edge to the other edge. Fig. 12 shows the current density and lattice temperature of Type-II design when filament starts moving from one corner to corner [see Fig. 12(a)–(c)]. The maximum temperature inside the device reaches, lowest when the filament is at the center. Temperature peaks again when filament gets manifested at the other edge. The process continues and makes the filament move from one edge to another edge, as shown in Fig. 12(c)–(e). The sensitivity of impact ionization with the lattice temperature is shown in Fig. 13.

VI. Power Scalability and On-State Performance

A. Power Scalability

When a high-voltage LDMOS device is used in the self-protection concept for automotive ICs, the scalability of failure current for more extended pulsewidths is a crucial design concern [21]. System-level IEC discharge events can

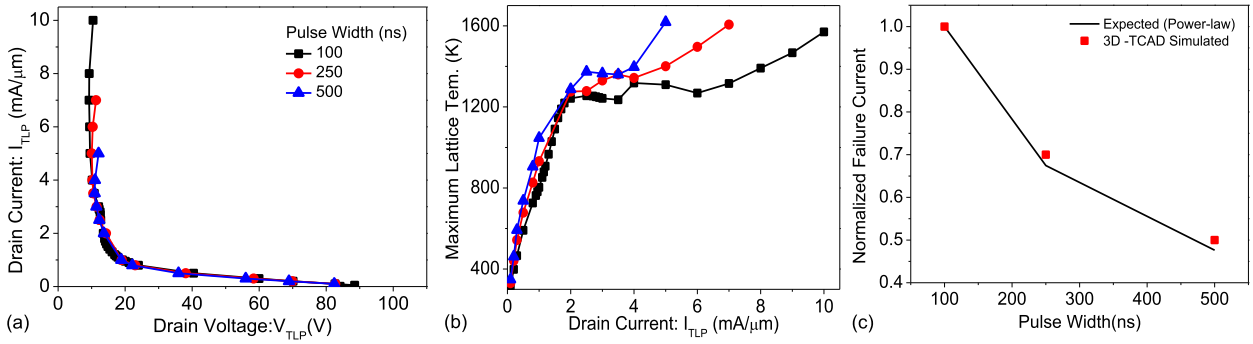

Fig. 14. (a) Simulated (3-D) TLP I–V characteristics and (b) maximum temperature at different current levels for a Type-III engineered LDMOS, stressed with different pulsewidths. (c) Normalized failure current as a function of pulsewidth, showing good scalability of the failure current for longer pulse discharges.

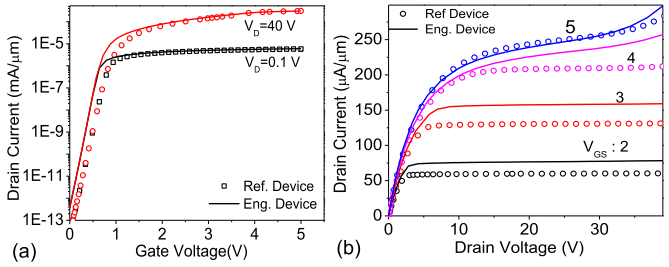

Fig. 15. (a) Input ID–VG characteristics and (b) output ID–VD characteristics of reference design (Type-I) and engineered (Type-III) device. The filament engineering yields 10× higher ESD robustness without much loss of ON-state performance.

exceed typical 100-ns HBM events. Hence, the HV ESD protection device should also be tested for scalability to longer pulsewidths [21], [22]. The Type-III LDMOS device shows that a 10× higher failure current should also be tested for its failure current scalability.

Fig. 14 shows the TLP I–V characteristics, and lattice temperature plotted as a function of stress current for different pulse durations. Failure current is found to scale for long pulse durations and follow the expected power law [Fig. 14(c)]. Lattice temperature rise near snapback, in the static filament zone, found to be limited. This will ensure that static filaments do not cause failure at snapback, even for more extended pulsewidths.

B. ON-State Performance

The design modifications (in Type-II and Type-III devices) mainly focus on improving ESD robustness by tweaking parasitic bipolar n-p-n action. These design changes found to cause only a small drift in ON-state dc I–V characteristics, as shown in Fig. 15. Of the three design modifications, p-well surface doping will only influence device threshold voltage and, hence, dc output characteristics. The substrate biasing is only applied during the ESD event, which does not affect the functional region. As reported in [11], the DL variation does not show any influence of functional characteristics.

VII. Conclusion

A novel approach to engineer current filaments is studied in detail. Positive substrate biasing and reduction in p-well doping, which improved the intrinsic n-p-n turn-on, resulted in moving current filament at higher injected current. However, such LDMOS devices could not survive failure from static current filaments at the onset of voltage snapback. This was addressed by reducing the critical temperature during initial filament formation after voltage snapback by using drain engineering. Drain engineering by relaxing the SCM strength lowered the current density inside the filament formed at the verge of voltage snapback. Faster n-p-n turn-on due to p-well and substrate bias engineering and static filament width adjustment by drain engineering provided 10× improvements in the ESD robustness. The engineered designs are useful in answering some of the fundamental questions related to filament motion. The temperature gradient inside the current filament is found to be the trigger point for filament motion. The gradient required for filament motion depends on n-p-n strength and heat dissipation inside the device via device geometry. Stronger n-p-n needs a smaller gradient for filament motion. Once the filament starts moving, it requires a lower temperature gradient to continue to move back and forth across device width. Finally, the engineered design shows good power scalability for long-duration discharges, a negligible effect on the transistor performance.

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