Part II: On the Three-Dimensional Filamentation and Failure Modeling of STI Type DeNMOS Device Under Various ESD Conditions

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***Abstract*—Time evolution of self-heating and current filamentation are discussed in this paper for shallow-trench-isolation (STI)-type drained-enhanced n-channel metal–oxide–semiconductor (DeNMOS) devices. A deeper insight toward regenerative n-p-n action and its impact over various phases of filamentation and the final thermal runaway is presented. A modified STI-type DeNMOS device is proposed in order to achieve an improvement ($\sim$2$\times$) in the failure threshold (I_{T2}) and electrostatic discharge (ESD) window (V_{T2}). The performance and filament behavior of the standard device under charge-device-model-like ESD conditions is also presented, which is further compared with the proposed modified device.**

***Index Terms*—Base push-out, charge device model (CDM), current filamentation, drain-enhanced metal–oxide–semiconductor (DeMOS), electrostatic discharge (ESD), human body model (HBM), input–output (I/O), kirk effect, laterally diffused metal–oxide–semiconductor (LDMOS), space charge build-up, thermal runaway, transient interferometric mapping (TIM).**

I. Introduction

TWO-DIMENSIONAL technology computer-aided design (TCAD) simulations are used by various groups [1]–[5] in the past in order to model the electrostatic discharge (ESD) behavior of various input–output (I/O) or ESD protection devices. Since grounded gate n-channel MOS (NMOS, with drain ballasting) and silicon-controlled-rectifierlike structures fail purely due to excess temperature rise (at drain/anode) and thermal runaway at very high transmission line pulse (TLP) currents, their failure current can easily be predicted using 2-D device simulation. However, we found that devices such as drain-extended MOS (DeMOS, as discussed in Part I) or, in general, devices that suffer from heavy charge modulation at early currents cannot be modeled using 2-D device simulations. As discussed in Part I, since the modeling for the ESD behavior of drain-enhanced n-channel MOS (DeNMOS) device [6]–[8] is normally based on 2-D simulations, it lacks the physical insight required to predict the 3-D filamentation and failure. Transient interferometric mapping (TIM) is another useful tool for understanding the device behavior under the ESD stress [9]. The TIM method monitors the temperature and free-carrier concentration-induced changes through a change in the silicon refractive index.

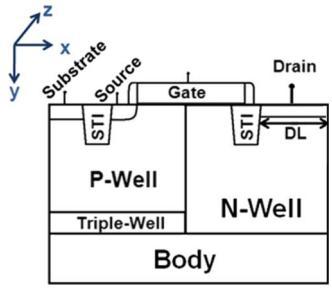

Fig. 1. DeNMOS device under study. Also shown is the one-sided structure (simulated). The actual structure on silicon has folded geometry where the drain (n-well) region is shared between two fingers.

In this paper, we present a better understanding of various phases of filamentation with a clear and correlated understanding of device failure during the ESD event. A clear and correlated picture on the impact of base push-out, space charge build-up, and regenerative n-p-n action over various phases of filamentation and thermal runaway is presented. Furthermore, we presented a modification in the device layout in order to achieve an improvement ($\sim$2.5$\times$) in the failure threshold (I_{T2}). The CDM performance of various devices is also discussed.

This part of this paper is arranged as follows: failure mechanism and 3-D device modeling of the device is presented in Section II, whereas Section III discusses the proposed (modified) device with $\sim$2$\times$ improvement in failure threshold and ESD window. Section IV compares the CDM performance of standard and modified DeNMOS devices, whereas Section V provides a summary.

II. Failure Mechanism and 3-D Device Modeling

Before we start discussing 3-D device behavior, it is worth pointing out the 3-D simulation approach. Fig. 1 shows a cross-sectional view of a single-finger DeNMOS device. In order to capture current filamentation, physical nonuniformity was created across the device width. In the past, it was reported that nonuniformity in the meshing (i.e., numerical nonuniformity) along the width can easily capture current filamentation.

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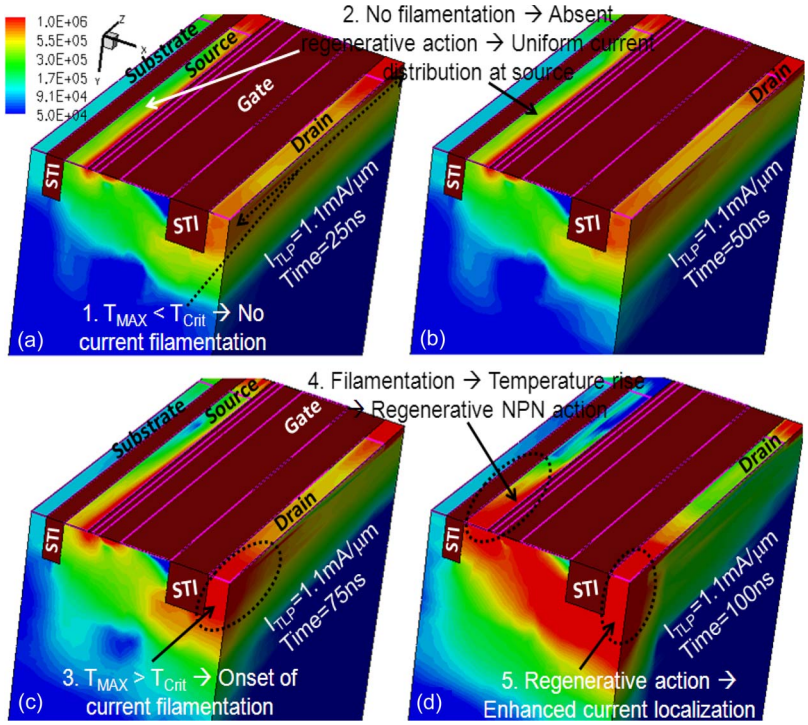

Fig. 2. Current density (in amperes per square centimeter) at different times extracted from 3-D simulations (DL = 0.2 μm). The first filament starts shrinking at the drain side because of temperature rise, which leads to a regenerative n-p-n action (due to the high fields after base push-out) that further causes a filament shrink at source side.

However, this may lead to artifacts in the generated results; hence, a "physical" nonuniformity along the width was created for 3-D simulations in this work. The following are the different ways for achieving a physical nonuniformity: 1) use source, drain, and substrate contact strips with different lengths (in the Z direction), i.e., nonuniform contact strips; 2) use multiple drain contacts with unequal spacing between them; and 3) terminate only one side of the device at STI. Furthermore, in order to achieve proper thermal boundary conditions, we extended the device boundaries by 5 μm and defined 300 K of thermal boundary condition at the surroundings of the device. The extension was done in such a way that it does not affect the electrical behavior of the device. We chose 5 μm since the thermal diffusion (in Si) length for 100 ns (HBM) is 3.3 μm. Fig. 2 shows the 3-D distribution of current density inside the device (i.e., along the device width at source and drain separately), which shows a unique filament behavior for different times. For shorter times, [Fig. 2(a), i.e., 25 ns], the device has almost uniform current conduction across the device width. However, for moderate times [Fig. 2(b), i.e., 50 ns], the current starts confining at the drain side, which is the onset of filamentation. Furthermore, at longer times [Fig. 2(c), i.e., 75 ns], the filament is greatly confined at the drain side, and there is also an onset of current localization at the source side. Finally, at 100 ns [Fig. 2(d)], a very narrow filament was formed, at both the source and the drain sides. It is worth mentioning at this point that the current confinement (i.e., filamentation) at the drain and source sides are indeed different events. First, the current filamentation forms at the drain side due to the base push-out and causes very high current densities and electric fields at the front side of the device. (This can also be the back side of the device, depending on the location of the current filament.) High electric fields and temperature underneath the N^+ drain diffusion, near the front (or back) side of the device, lead to excess carrier generation (due to impact ionization and thermal generation), which takes place nonuniformly across the device width. These generated carriers (holes for a parasitic n-p-n device) then flow through the substrate. The nonuniform nature of hole distribution (across the device width) in the substrate causes a nonuniform (i.e., local) triggering of the distributed parasitic bipolar devices along the width of the device. Since the number of holes greatly exceeds in the front (or back) side of the device, the distributed bipolar in the front (or back) side triggers strongly, which gives a better conductive path through the front (or back) side of the device. This eventually turns off the distributed parasitic bipolar across the rest of the device width and leads to the onset of nonuniform current distribution at the source side, which shows up as a filament shrink at the source side. A strong turn-on of the distributed bipolar at the front (or back) side or the turning off of the distributed bipolar across the rest of the device width further confines the current in a narrow region at the drain side, i.e., further filamentation. These two processes eventually get coupled to each other (i.e., act like a positive feedback to each other) and lead to a very fast filamentation and failure. We call this coupled mechanism a *regenerative n-p-n triggering or action*. It is also worth pointing out that 1) the depth of snapback is strongly connected with the strength of regenerative n-p-n action, which essentially depends on the width of the device, and a device with higher width will result in higher current density inside the filament, which will eventually cause a stronger regenerative n-p-n action, i.e., producing a deeper snapback, and 2) the rate at which these two

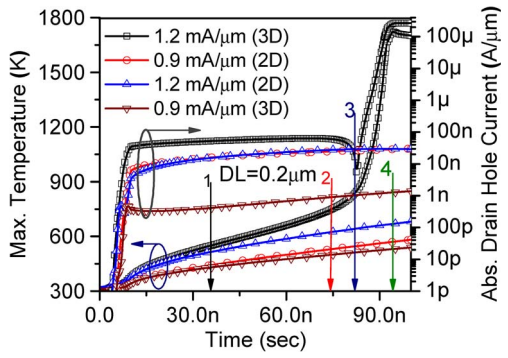

Fig. 3. Hole current and maximum temperature at different current levels, extracted from 2-D and 3-D simulations. Three-dimensional simulations for lower currents and 2-D simulations show the absence of regenerative n-p-n action, whereas the regenerative n-p-n action is clear for higher currents (beyond the onset of base push-out 3-D) because of an exponential rise in the hole current. The various phases of filament formation are also described (1: onset of base push-out and space charge build-up, 2: onset of filamentation because of high temperature, 3: filamentation causing temperature rise, which starts a regenerative n-p-n action, 4: device failure because of thermal and regenerative-n-p-n-based filamentation).

processes becomes coupled is a current (i.e., I_{TLP})-dependent phenomenon. In other words, the higher the stress current, the earlier (with respect to time) the onset of regenerative n-p-n action and device failure.

Fig. 3 shows an exponential increase in the drain hole current (extracted from TCAD simulations, at $I_{\mathrm{TLP}} \sim I_{T2}$) at higher times, which gives an indication of the presence of regenerative n-p-n action.[1] The generated large hole current leads to a stronger local turn-on of the n-p-n, as previously discussed. This regenerative n-p-n behavior was not observed in 2-D simulations and was also not observed before the base push-out in 3-D simulations, which further validates the previous discussion on the current confinement at the drain and source ends. We find that regenerative n-p-n action starts at a lattice temperature higher than 1000 K, which itself is a sufficient temperature for the formation of a current filament at the drain.

In summary, we find six unique filament behaviors at the drain and source sides during 20–100 ns, considering a current that is sufficient to cause base push-out, which finally leads to a device failure.

1) Onset of the base push-out, which leads to a high space charge buildup.
2) High energy storage in the space charge region and its dissipation into silicon.
3) Heating, because of high fields after the base push-out, leading to an onset of filamentation at the drain side.
4) Filamentation leading to further temperature rise.
5) Onset of regenerative carrier generation due to high electrical fields and high current density in the filament.
6) Further enhancement of heating at drain diffusion because of filament shrink at the drain side that causes a regenerative n-p-n action. The regenerative n-p-n action shrinks the filament at the source side. These two mechanisms work together and act like a positive feedback to each other. This leads to a fast temperature rise within a short time (Fig. 3).
7) Device failure because filamentation based on thermal and regenerative n-p-n.

Even though the regenerative n-p-n action was observed, the dominant mechanism for device failure is exceeding the melting temperature. The regenerative n-p-n action only acts as an extra positive feedback after the onset of filamentation, which causes shrinking of current filament at the source side, leading to a rapid confinement of the current filament during short time scales.

Fig. 4 shows the lattice temperature at different times extracted from 3-D simulations, which validates the location of hot spot and failure due to excessive temperature, as observed in the scanning-electron-microscope image (shown in Fig 3 of Part I). Fig. 4 shows that the hot spot always sits underneath the N+ drain diffusion, which is due to a very high electrical field underneath the drain diffusion after the onset of base push-out. Initially, temperature rises uniformly across the 3-D plane, whereas, after the onset of filamentation at the drain side, it rises even faster [compared to 2-D simulation results, Fig. 3]. STI in the vicinity of the hot spot further degrades the heat flux, leading to a faster temperature rise, causing a sufficient temperature at the drain side for strong filamentation. Finally, regenerative n-p-n action causes an exponential rise in temperature, which leads to a device failure.

III. Further Improvement in Failure Threshold

In Part I [10], we have also seen (Fig. 5) improvement in failure threshold by extending n^+ drain diffusion ($\mathrm{DL} = 2.2\ \mu\mathrm{m}$) and drain contact (no change in ballast resistance) all over the drain diffusion. Increasing the diffusion area (increasing DL) leads to a lower carrier density in the n-well region underneath the drain diffusion (Fig. 5). Reduction of carrier density in n-well shifts the onset of base push-out to higher currents. Since there is no base push-out before device failure, the high field is located at the well junction, which is much lower than the peak electrical field under the drain contact (n^+) of a device showing base push-out (for $\mathrm{DL} = 0.2\ \mu\mathrm{m}$). This behavior is discussed in more detail in the next section.

Fig. 5 shows the (a) current density, (b) electric field, and (c) impact ionization contours for a modified device ($\mathrm{DL} = 2.2\ \mu\mathrm{m}$) at a higher TLP current (i.e., $2\ \mathrm{mA}/\mu\mathrm{m}$). The modified device fails at $2.5\ \mathrm{mA}/\mu\mathrm{m}$ [10], whereas, from Fig. 5, an efficient bipolar triggering is evident, without any device failure. Furthermore, Fig. 5(a) shows relaxed current density (or carrier density) underneath the drain diffusion, compared to the standard device (Fig. 7(b) for Part I and Fig. 2 for Part II). The relaxation in carrier density is attributed to an increased volume of the n-well region. The relaxed carrier density pushes the onset of base push-out to a higher TLP current, which is

[1] In the past, it was reported that the carrier heating in the high field region influences the saturation drift velocity and enhances the impact ionization. This causes higher impact-ionization-generated carriers, which flow (holes for parasitic n-p-n) through the substrate. Excess holes in the substrate trigger the parasitic n-p-n device faster, causing a deeper snapback. This type of regenerative carrier generation and bipolar triggering was named *regenerative NPN action*. Furthermore, the deep snapback leads to a short circuit power dissipation, which was reported as the dominant cause of second breakdown [6], [7].

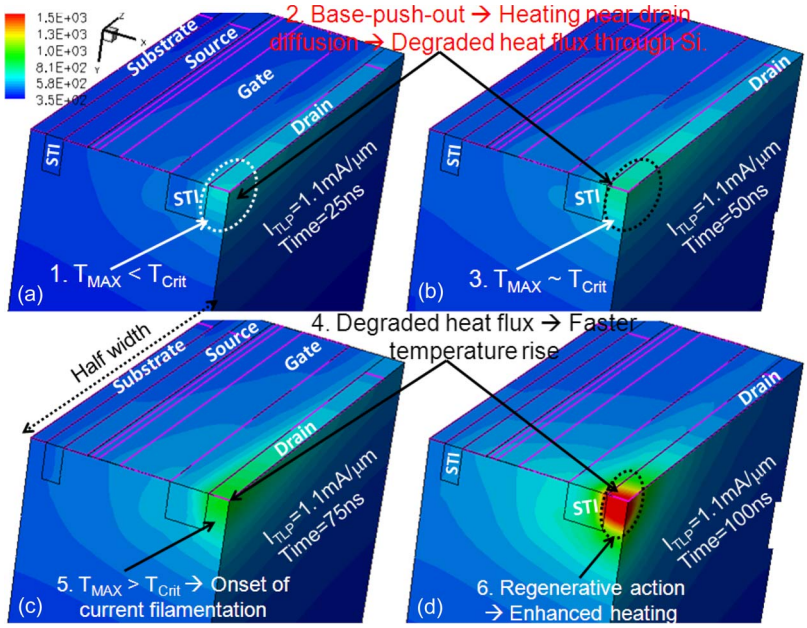

Fig. 4. Lattice temperature (in Kelvin) at different times extracted from 3-D simulations (DL = 0.2 μm).

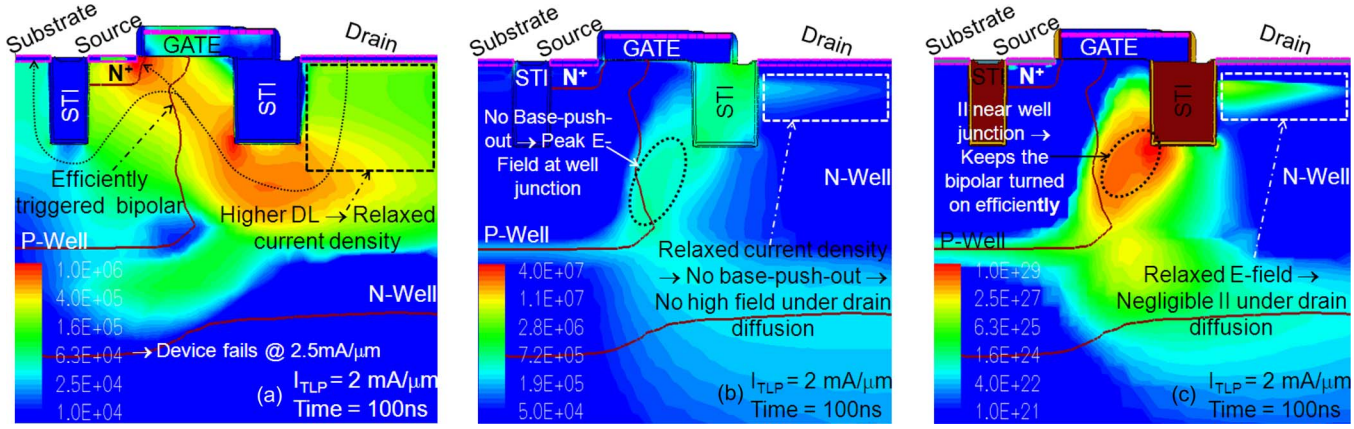

Fig. 5. (a) Current density (in amperes per square centimeter). (b) Electric field (in volts per centimeter). (c) Impact ionization ($\mathrm{cm}^{-3}\ \mathrm{s}^{-1}$) contours for modified device (DL = 2.2 μm) at $I_{\mathrm{TLP}} = 2\ \mathrm{mA}/\mu\mathrm{m}$.

evident from the absence of base push-out [Fig. 5(b)]. Since the base push-out is not present in the modified device, the device experiences a significantly relaxed electric field underneath the drain diffusion, whereas the peak electric field was observed at the n-well/p-well junction. This helps the device in two ways: 1) *relaxed heating*: the peak electric field and, eventually, the hot spot exists at the n-well/p-well junction, which leads to a relaxed heating (J.E) due to lower current density (J) and E-Field (E) at n-well/p-well, compared to J and E underneath the drain diffusion for a device with DL = 0.2 μm. Furthermore, the hot spot at the well junction has a higher Si volume for heat diffusion, which enhances the heat flux and eventually improves the device cooling during the ESD stress. 2) *efficiently triggered bipolar*: peak E-Field and, eventually, the peak impact ionization occurs at the well junction [Fig. 5(c)], and therefore, the effective base length does not degrade at higher currents, unlike the standard device. This further keeps the bipolar triggered efficiently, which eventually improves the turn-on capability of the device, i.e., reduces the ON-resistance, which is evident from the TLP characteristics of the modified device (Fig. 4, Part-I).

Fig. 6 depicts the filament behavior of a device having a larger DL. Fig. 7 shows that, initially, the heating takes place at the well junction, which was quite relaxed, compared to the case of DL = 0.2 μm (i.e., the device having base push-out) because of less electric fields and less current density. Fig. 8 compares the maximum temperature and hole current in both the devices at failure current. Because of the absence of base push-out and regenerative n-p-n action, the device with larger DL exhibits a smoother increase in temperature until failure. At high temperatures, only an extended filament is formed at the drain side (Fig. 6) because of lack of regenerative n-p-n action. At the source, a uniform current distribution is found for the simulated device. Due to a reduced current confinement in the filament, a higher I_{T2} was achieved.

The device intrinsic performance, i.e., R_{ON} (ON-resistance), V_{BD} (breakdown voltage), C_{GG} (gate capacitance), and C_{DD} (drain capacitance), was found unchanged for the DL = 2.2 μm

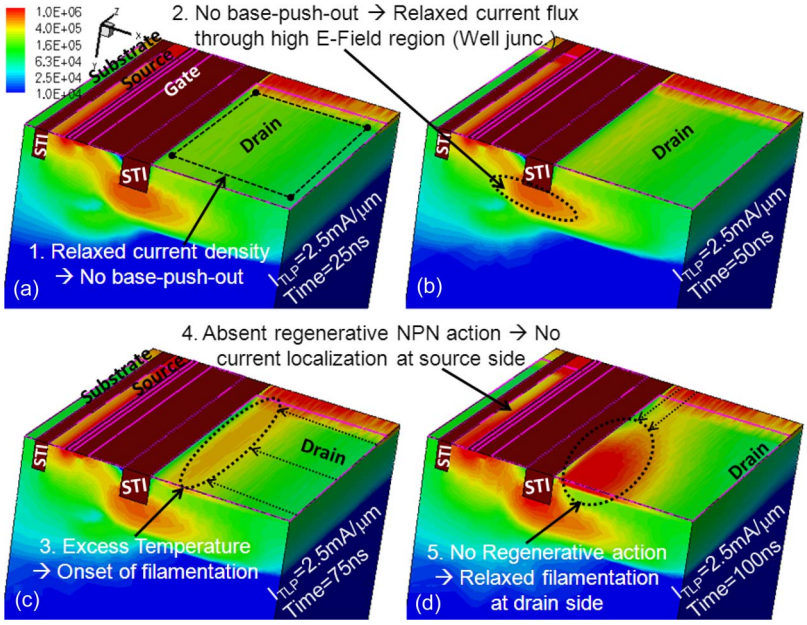

Fig. 6. Current density (A/cm^{-2}) at different times extracted from 3-D simulations (DL $= 2.2$ μm). The filament shrink at the drain side is because of the temperature rise, whereas the absence of regenerative n-p-n action (due to the lower fields in the absence of base push-out) causes a uniform current density at the source side.

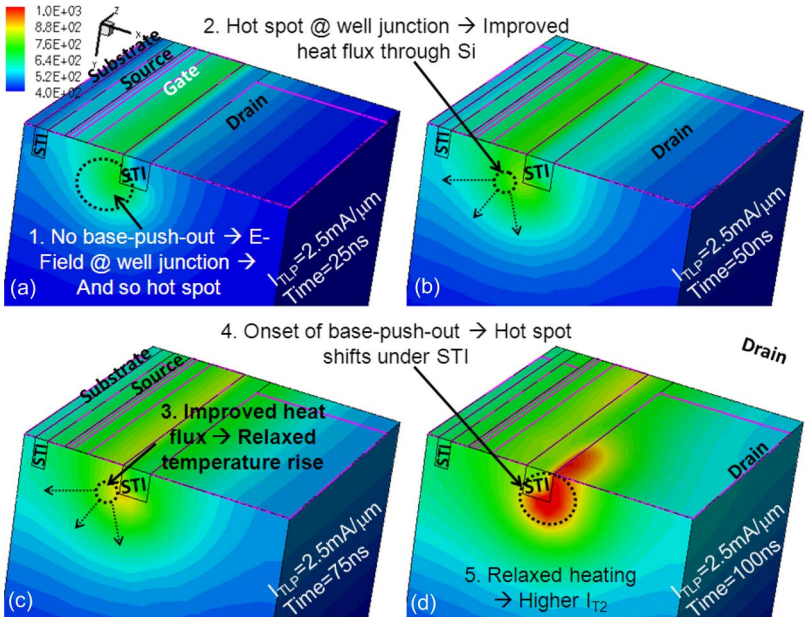

Fig. 7. Lattice temperature (in Kelvin) at different times extracted from 3-D simulations (DL $= 2.2$ μm).

case, so no loss of mixed signal/RF performance of the device is observed when used in I/O circuits. Furthermore, we found that DL $= 0.6$ μm is sufficient enough to shift the onset of base push-out to higher currents in order to achieve high I_{T2} values.

IV. CDM Performance

Fig. 9 shows the pulsed I–V (or quasi-static TLP) characteristics of the standard and modified STI DeNMOS devices (i.e., DL $= 0.2$ μm and DL $= 2.2$ μm). The rise time and pulsewidth used for very fast TLP simulations were 250 ps and 5 ns, respectively, whereas the extraction of I–V data for TLP characteristic is done by averaging the transient voltage and temperature data (w.r.t. time) between 3 and 5 ns. The following points can be concluded from Fig. 9: 1) The modified device has better bipolar-driven snapback, even under the fast transients. This behavior is similar to the HBM case. This also validates that the parasitic bipolar triggering is a faster event, compared to "current filamentation" or "thermal failure." 2) The modified device shows lower ON-resistance at lower current densities similar to the HBM case, whereas, at higher current densities, the $R_{\rm on}$ of the standard device is much smaller. 3) Both the devices survive much higher currents, compared to HBM. This behavior is attributed to a lower self heating due to smaller time

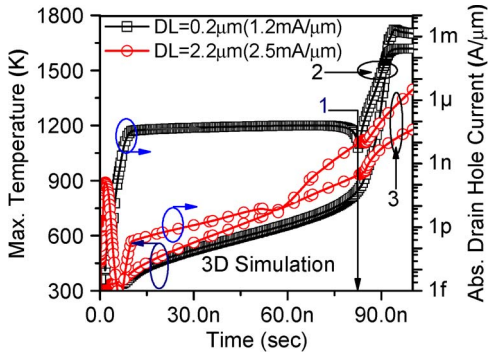

Fig. 8. Hole current and maximum temperature at the failure current level of the device having base push-out (DL $= 0.2$ μm) and no base push-out (DL $=$ 2.2 μm) before filamentation (1: time at which the maximum temperature and hole current are the same for both devices, 2: regenerative n-p-n action leading to fast formation of filament, 3: absence of base push-out causing lower electric fields, which leads to lower impact-ionization-generated holes). Since hole current is negligible, there is no regenerative n-p-n action.

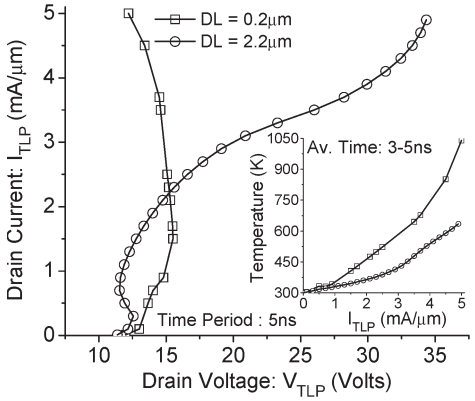

Fig. 9. Simulated (3-D) very fast TLP (CDM) characteristics of DeNMOS device having different drain diffusion lengths (DLs).

scales, which also validates that the parasitic bipolar triggering or regenerative n-p-n action is not the dominant cause of failure. The STI DeNMOS fails because of excess heating at the drain side. 4) The standard STI DeNMOS device shows a soft base push-out in contrast to the hard base push-out observed in the HBM case. As discussed earlier, the base push-out is a current (or carrier density)- and time-dependent phenomenon. The space charge build-up underneath the drain diffusion due to carrier modulation is limited due to the very short (i.e., CDM) pulse duration, and therefore, a much higher current density (i.e., $I_{\rm TLP} = 4{-}5$ mA/μm) is required for the base-push out. 5) The modified device shows a relaxed self heating due to the absence of base push-out, as discussed earlier. 6) The modified device provides a higher ESD window similar to the HBM case.

Fig. 10 shows the transient TLP characteristics for both the structures at a TLP current of 5 mA/μm. It can be seen from this figure that 1) voltage overshoot is 30% higher in the standard device (DL $= 0.2$ μm), which may lead to an early failure due to gate oxide breakdown. 2) Both the devices show a faster bipolar triggering, i.e., within 100 ps. 3) Standard device shows a soft base-push-out-driven snapback. The onset of this base push-out occurs at $\sim$300 ps. 4) The modified device shows a linear temperature rise during the 5-ns CDM stress, whereas the standard device shows an exponential temperature

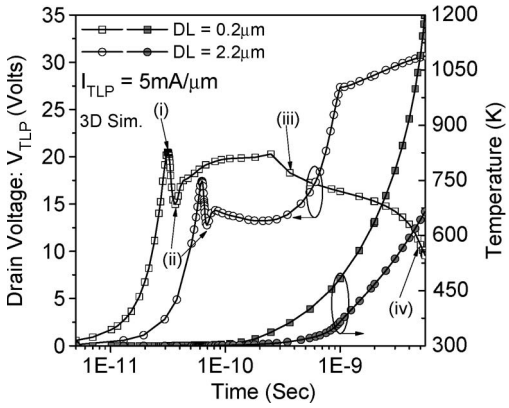

Fig. 10. Transient characteristics of DENMOS devices having different drain DLs under CDM condition, extracted from 3-D simulations.

rise in temperature after 3 ns. This is attributed to an excess heating in the standard device, even at shorter time scales, leading to a temperature higher than the critical temperature (for thermal runaway, i.e., the onset of NDR), causing a current filamentation and thermal failure.

Fig. 11 shows the 3-D contours of lattice temperature (K) and current density (in amperes per square centimeter) for both the devices at a TLP current of 5 mA/μm. The figure validates the conclusions drawn from Figs. 9 and 10. Furthermore, it also shows that the hot spot location and filament behavior for both the devices occur at a significantly higher current, which is almost similar to the HBM case, except the current confinement at the source side for the device with smaller DL. As discussed earlier (for the HBM case), regenerative n-p-n triggering leads to a filament shrink at the source side and causes a very fast filamentation and failure. On the other hand, it is evident from Fig. 11 that regenerative triggering is absent for the CDM case. This is due to the fact that the coupling of filamentation at the drain and source sides and a strong turn-on of a few distributed bipolars are considered to be time-dependent phenomena. Since the CDM time domain (5 ns) does not allow the processes to both start and become coupled, the current shrink at the source side is absent. This also causes a soft snapback for devices with a smaller DL, whereas it was harder for the HBM case.

V. Conclusion

We have found that the onset of filamentation is caused by the onset of space charge modulation under the HBM condition, which is electrical in nature. After the onset of filamentation, devices fail due to excess heating at the drain side, i.e., electrothermal failure. On the other hand, the onset of current filamentation under CDM conditions is purely due to elevated temperatures at the drain side, i.e., a thermal failure. The degree of confinement of the filament is strongly dependent on the existence of a regenerative n-p-n action, i.e., excess carrier generation under high E-fields at high temperatures. In a DeMOS with smaller DL, a strong regenerative n-p-n triggering is found to occur along with a base push-out or space charge modulation, which results in a low It2 under HBM condition. On the other hand, the significant space charge build-up and regenerative triggering were absent during the CDM stress, which

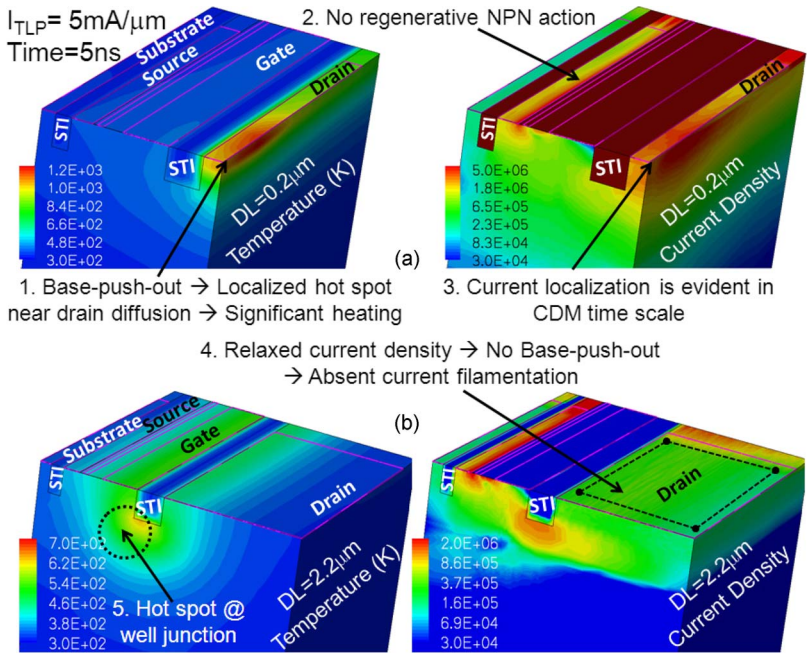

Fig. 11. Three-dimensional contours of temperature (in Kelvin) and current density (in amperes per square centimeter) for (a) a standard DENMOS device and (b) a modified DENMOS device. Comparison of the filamentation and self-heating in two devices with different DL values under CDM-like conditions is also shown.

shows the time dependence of these new phenomena. Avoiding the base push-out by decreasing the current density under the drain diffusion increases the failure current significantly. This can be achieved by choosing a sufficient length of the drain diffusion area. Devices with a higher DL show improved It2 values and have been found to have a pure thermal failure due to the absence of base push-out or conductivity modulation.

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