An Insight Into the ESD Behavior of the Nanometer-Scale Drain-Extended NMOS Device—Part I: Turn-On Behavior of the Parasitic Bipolar

Amitabh Chatterjee, Mayank Shrivastava, *Member, IEEE*, Harald Gossner, *Member, IEEE*, Sameer Pendharkar, *Senior Member, IEEE*, Forrest Brewer, *Member, IEEE*, and Charvaka Duvvury, *Fellow, IEEE*

***Abstract*—A second-breakdown phenomenon (It2) in a drain-extended n-type metal–oxide–semiconductor (DENMOS) is associated with complex triggering of a parasitic bipolar transistor. Full comprehension of the problem requires 3-D modeling; however, there is even deficiency in the understanding of the phenomenon occurring in the 2-D cross-sectional plane. We present experiments and models to understand the physics of bipolar turn-on and its impact on the onset of space-charge modulation in a DENMOS device. We present a detailed analysis of the current paths involved during the bipolar turn-on. We show that a strong snapback is triggered due to coupling of the parasitic bipolar turn-on in a deeper region of the p-body and avalanche injection at the drain junction. Furthermore, we show that the ballast resistor formed in the drain region due to current crowding of electrons under high-current conditions can be modeled through a simplified 1-D analysis of the n^+/n^- resistive structure.**

***Index Terms*—Avalanche injection, current crowding, electron ballasting, filamentation, hole ballasting, stages of Bipolar turn-on.**

I. Introduction

AGGRESSIVE scaling of devices, in adherence to Moore's law, has resulted in a fall in the core voltage level down to an operative level of 0.9 V at the 90-nm node. However, mainstream input–output (I/O) voltages continue to be higher than 1.8 V, which requires high-voltage (HV) drivers that can be easily integrated into low-cost complementary metal–oxide–semiconductor (CMOS) technologies. A nanometer-scale drain-extended n-type metal–oxide–semiconductor (DENMOS) (see Fig. 1)—an HV device compared with low-voltage core CMOS devices—is suitable for I/O drivers as they can satisfy higher voltage requirements and stringent requirements such as low leakage at high temperature and lower capacitive loading, which is essential for signaling application.

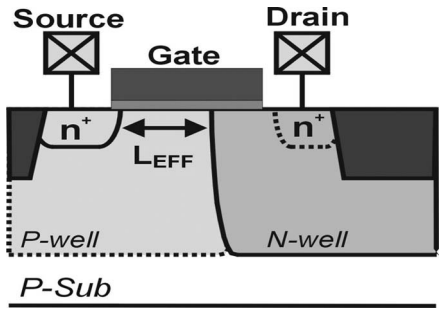

Fig. 1. Schematic of a 90-nm DENMOS.

HV technologies resort to local oxidation of silicon for HV isolation, which allows poly to terminate on the thick field oxide.

However, the technique is not applicable for nanometer-scale technologies. In the deep-submicrometer process, analog and power integrated circuit technologies have incorporated methods that are used in mainstream nanometer-scale CMOS technologies. Shallow trench isolation (STI) is one such critical low-voltage technology that allows increased logic density. Drain extension, which has so far been used only in mature HV analog processes, can now be integrated in standard CMOS processes without the requirement for a field oxide. A very thin gate oxide in the DENMOS can withstand high breakdown voltages, and extra costs for the thicker gate oxides of the HV devices can be avoided [1].

In spite of the ease of process flow, which allows cost-effective integration with the CMOS technology, the reliability of the HV drivers against electrostatic discharge (ESD) strikes has remained a big concern [3]. Protection circuitry for the HV I/O can be based on devices such as diodes, low-voltage NMOS, and silicon-controlled rectifiers (SCRs). However, using low-voltage devices requires stacking in order to support 5-V applications, which is not a feasible solution due to reliability issues such as hot-carrier effects and gate-oxide reliability

Manuscript received January 12, 2010; revised September 24, 2010; accepted October 20, 2010. Date of current version January 21, 2011. The review of this paper was arranged by Editor J. Woo.

A. Chatterjee and F. Brewer are with the Department of Electrical Engineering, University of California, Santa Barbara, CA 93106 USA (e-mail: amitabh@ece.ucsb.edu; forrest@ece.ucsb.edu).

M. Shrivastava and H. Gossner are with Infineon Technologies AG, 81726 Munich, Germany (e-mail: shrivastva.mayank@gmail.com; harald.gossner@infineon.com).

S. Pendharkar and C. Duvvury are with Silicon Technology Development, Texas Instruments, Dallas, TX 75265 USA (e-mail: s-pendharkar1@ti.com; c-duvvury@ti.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2010.2093010

[3]. Similarly, using a diode is also a highly inefficient protection strategy. A larger voltage drop across the diode makes it unsuitable for HV applications. An alternative approach can be based on the SCR, which has an efficient current-handling structure [3]–[4]. However, it is normally not suitable for protecting such HV pins due to the extremely low sustaining voltage, which makes the SCR susceptible to latch-up either during transients or during power-on ESD strikes. An effective and simple solution may be is to use a gate-grounded (GG) DENMOS as the protection element itself having a variable rise time. However, these HV devices are susceptible to ESD events, and their failure mechanism has remained enigmatic. The weak behavior of the DENMOS is explained through inhomogeneous triggering of bipolars along the width as it leads to current filamentation due to localized heating and permanent damage of the device [2], [5]–[6]. However, in order to understand this behavior in the 3-D structure and deconvolute the processes involved, one needs to understand the 2-D behavior of the parasitic bipolar turn-on in DENMOS devices first. This requires a detailed study of turn mechanisms and an accurately established model for the current-crowding mechanisms involved. A better understanding of the 2-D electrostatics of the breakdown field and the physics of avalanche injection around the drain region allows improving the design of these devices for improved robustness [4]–[9].

In the current–voltage (I–V) characteristics of DENMOS devices, strong snapback behavior can be found, which often coincides with the failure of the devices under ESD conditions. This monotonic fall in the device voltage is triggered by the onset of current filamentation or localization in the DENMOS due to modulation of space charge, which is simultaneously accompanied by excess heating and device damage [10]–[13]. The dynamics of the bipolar turn-on and the sequential events has been systematically investigated in this paper. Finally, experiments and analysis have been presented to corroborate the model. Generalized models established in this paper are useful in building high-current models for field-effect transistor (FET) structures having an n-p-n-n$^+$ structure, wherein compact models can be extracted for building I/O circuits. Simulation of turn-on behavior, and hence space-charge-limited (SCL) transport, is established.

II. Experimental Analysis of DENMOS Failure Under Human Body Model Stress

GG DENMOS devices exhibit failure due to filament formation (see Fig. 2) from the drain to the source under transmission line pulsing (TLP) stress conditions at very low failure current densities It2 $= 0.1$ mA/μm. Fig. 3 shows the failure point on the I–V curve. The nature and location of the damage points shows the critical role of the localized turn-on of a parasitic bipolar junction transistor, which is formed by the drain n$^+$, the substrate p$^-$, and the source n$^+$ [10]–[13].

The goal of this paper is to analyze the localized turn-on of the parasitic bipolar and space-charge modulation (or base push-out) conditions in a non-STI-type DENMOS device [15]. In this section, we first present a technology computer-aided design-based (TCAD) study of the dynamical bipolar turn-on under a current ramp having a variable rise time.

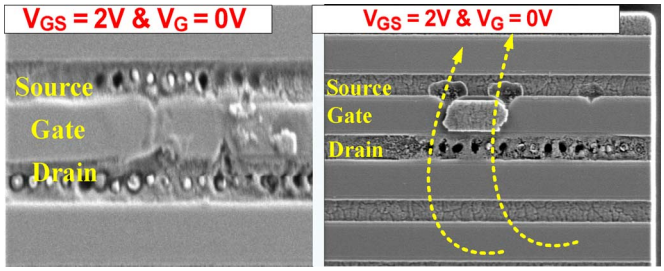

Fig. 2. Scanning electron microscopic image showing a filament that extends from drain-to-source points to the critical role of the parasitic bipolar turn-on.

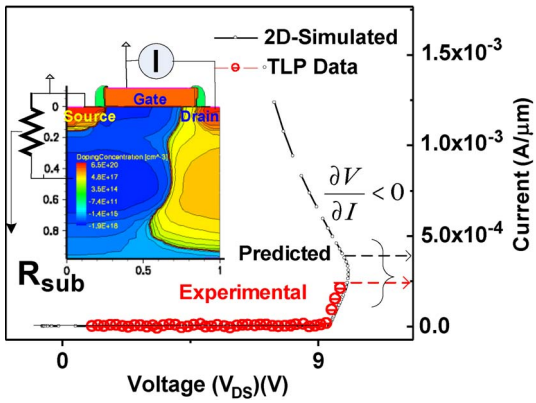

Fig. 3. Extremely low failure current in the DENMOS under TLP stressing compared with a predicted It2 value at the knee of the I–V curve.

III. Understanding the Dynamical Turn-On of the Parasitic Bipolar in the DENMOS: TCAD-Based Analysis

A. Analysis of a Strong Snapback in the DENMOS

In this section, a strong snapback has been investigated using calibrated 2-D transient device simulations on a test structure realized using a well-calibrated process simulation deck. A current ramp is applied. Substrate contacts are added at the left boundary of the simulation structure, which approximates the flow of holes through the substrate in the experimental test structure. The variables $I(t)$ and $V(t)$, which are explicit functions of time, are together plotted to generate an I–V relationship. In the simulations, the current ramp can be adjusted to study the dependence of a snapback on the rise time of the pulse.

The quasi-steady behavior can be simulated by slowing the current ramp. Under these conditions, a recombination current across the drain–substrate diode becomes comparable with the magnitude of the input current as it minimizes the dv/dt effect (see Appendix A.1). As the breakdown current increases, the device exhibits a prolonged negative resistance region or a strong snapback beyond the knee (see Fig. 3), which is marked as the onset of catastrophic failure due to filamentation.

The impact of an avalanche-generated hole current on the bipolar turn-on was analyzed through simulations by adding the resistance $R_{\rm sub}$ (per device width) to the substrate contact

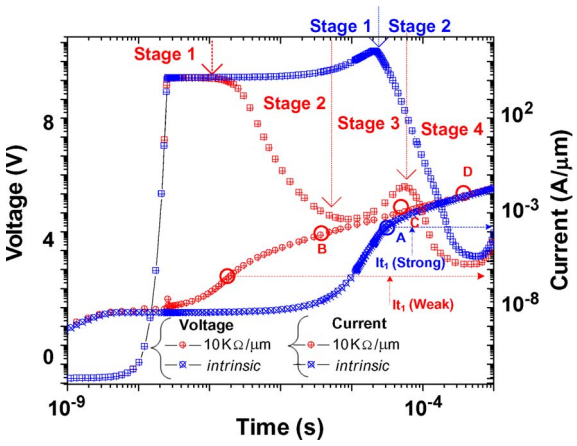

Fig. 4. Dependence of snapback features on the ramp rate: The monotonic fall in voltage when $R_{\rm sub}$ = intrinsic is very prominent and less predominant when $R_{\rm sub} = 10\ {\rm K}/\mu{\rm m}$. The substrate resistance $R_{\rm sub}$ is given as resistance per device width (to be consistent, stage 2 in blue must be stage).

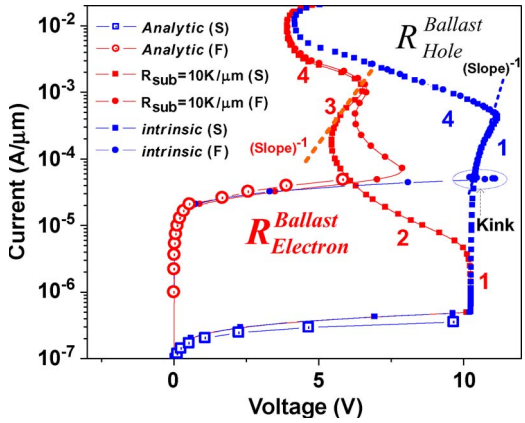

Fig. 5. Ramp rate dependence of the snapback on the I–V curve slow (S) and fast (F). The strong snapback observed is due to the intrinsic substrate resistance, whereas the double snapback (hence the weak first snapback) can be observed for higher $R_{\rm sub}$. The different stages of snapback for $R_{\rm sub} = 10\ {\rm k}\Omega/\mu{\rm m}$ are the following: stage 0, prebreakdown; stage 1, hole ballast; stage 2, bipolar turn-on; stage 3, electron ballast; stage 4, current-controlled snapback. Slow (S) 1 A/μm/ms, fast (F) 1 A/μm/ns.

(i.e., $R_{\rm sub}$; see Fig. 4) in the calibrated structure (see Fig. 3). Irrespective of the ramp rate, the device with the intrinsic substrate resistance $R_{\rm sub} = 0$ always exhibits a strong snapback in Figs. 4 and 5 (i.e., the device goes from stage 1 to stage 4).

For higher $R_{\rm sub} = 10\ {\rm K}/\mu{\rm m}$, an additional positive resistive branch is observed (stage 3) in between two negative resistance regions for slower ramps. This disappears at faster current ramps.

This behavior can be explained as follows.

Stage 1: Breakdown in the Depletion Region and Formation of the Current Path Controlled by the Hole Current (Hole Ballast Region): During an ESD event, the voltage buildup establishes twin pockets of the electric field (E-field), namely, PX and PA, in the structure: The first of these appears deep in the bulk at well junctions, and the second appears around the region of the drain sidewall junction, i.e., the gate-to-drain edge (see Fig. 6). Both peaks lead to a current in the bulk by avalanche-generated holes. For a GG configuration DENMOS, the E-field shows a reversal around the region,

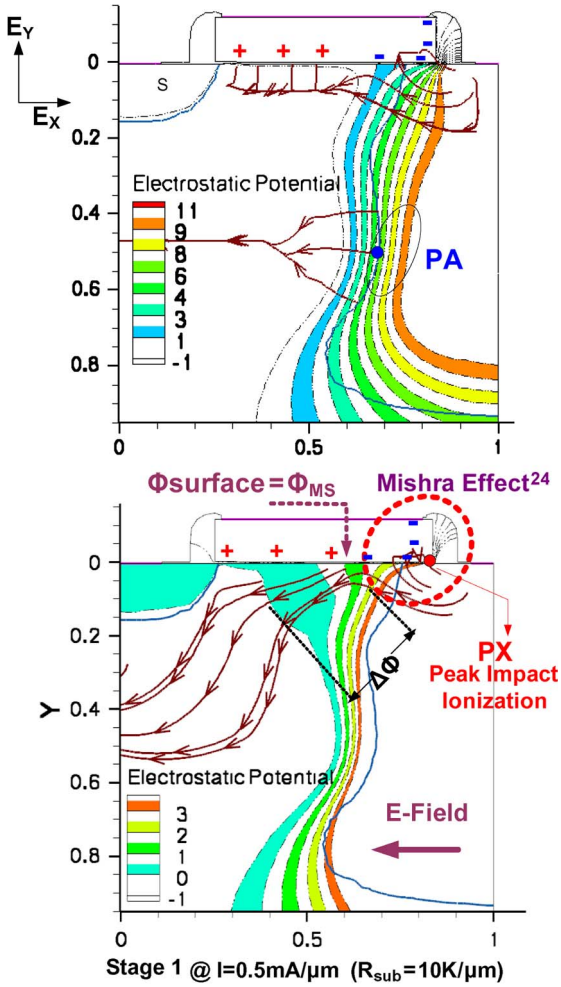

Fig. 6. Contours showing the electrostatic potential and E-field distribution. Twin pockets of the E-field, i.e., PX and PA, where the impact-ionized-generated holes lower the barrier around the source end. Holes are attracted by the gate, and their crowding leads to the buildup of the potential $\boldsymbol{\Delta\Phi}$

where the surface potential Φ_S in the channel is equal to the metal–semiconductor work function $\Phi_{\rm MS}$, i.e., $\Phi_S = \Phi_{\rm MS}$, and thus, avalanche-generated holes in the region PX are pulled toward the gate [24].

Thus, the drain region, which is under the influence of SCL transport of accumulated holes, behaves as a current-controlled 2-D SCL resistor in the process and exhibits a ballast action due to the hole current, whereby the potential $\Delta\Phi$ builds up across this region (see Appendix A.2). Interestingly, the ballast action due to the hole current shows a linear characteristic. The flow of holes also influences the barrier height at the source end, both within the bulk (SB) and around the gate region (SG). Around the drain region, electrons diffusing below the oxide are initially pushed toward the substrate (pinchoff region in a depleted channel), where they get eventually collected at the drain contact [see Fig. 7(a)].

Stage 2: First Snapback (Presnapback) Due to n-p-n Turn-On: Thus, initially, most of the electron current is through the depleted channel below the gate and the extremely low injection inside the bulk. However, the increased flow of holes into the substrate can substantially lower Φ_{SB} (SB) and causes electron injection into the depleted channel (see Fig. 8).

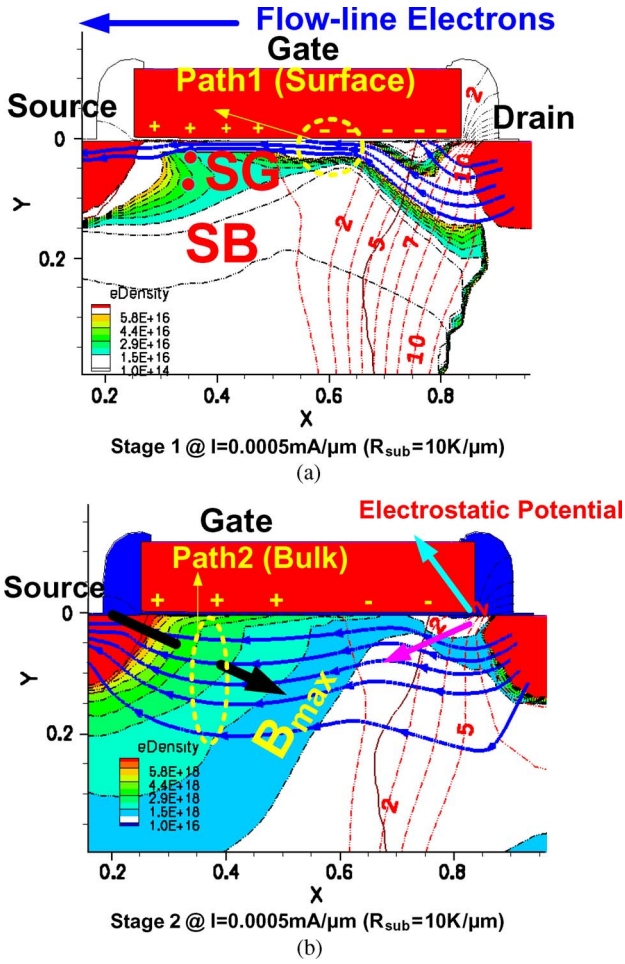

Fig. 7. Turn-on of the parasitic bipolar where the electrons are initially injected across path 1 and subsequently initiate higher injection across path 2 (the lower barrier around SG compared with SB makes the initial injection easier).

At a certain stage, when the source injection becomes very prominent, avalanche-generated carriers begin to modulate the depleted drain region. Subsequently, a snapback is triggered (shown by the change in $\Delta\Psi_1$ for the potential contour Ψ_1 and in $\Delta\Psi_2$ for the potential contour Ψ_2), which leads to more electron–hole pair generation (see Fig. 8). Electrons that diffuse along path 2 now help sustain an avalanche-generated phenomenon, which was initially triggered due to increased electron injection through the channel (path 1; see Fig. 7).

Stage 3: Postsnapback and Ballast Action Due to the Electron Current: This is marked by a positive slope, which exhibits the inability of the device to maintain the regenerative process. Now, in order to sustain avalanche injection in this region, a sufficient potential drop needs to be established across the space-charge region for a given current density. The current density below a threshold value can lead to a positive slope in the I–V curve [see Fig. 9(a)]. Thus, during this dynamical turn-on process, the space-charge region behaves as an SCL resistor under avalanche injection, whereby it exhibits a positive slope (for structure 2). The dynamical ballast action on the I–V curve during the bipolar turn-on can be efficiently utilized to limit the current, which can prevent filamentation during the bipolar turn-on [19].

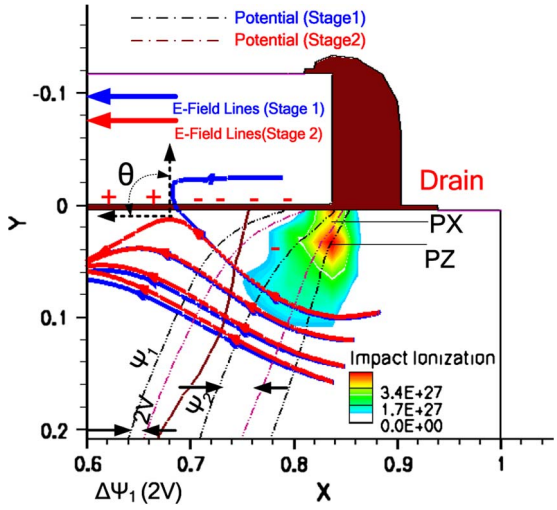

Fig. 8. Avalanche injection phenomenon across the drain region as the initial impact ionization peak shifts from the region PX to the region PZ.

Faster ramps (under ESD-like conditions) lead to a larger displacement current, making the positive resistive trend less prominent.

Stage 4: Strong Avalanche Injection: This is due to triggering of a regenerative avalanche injection phenomenon at the drain contact. As the current increases beyond region 3, the E-field continues to peak around the junction of the N-well (n^- region) and the drain contact (n^+ region) [see Fig. 9(b)]. Finally, at a critical current density, space-charge modulation in the lowly doped drain leading to a shift of the peak E-field to the highly doped drain junction (similar to the Kirk effect) triggers a further snapback. This, again, can be seen as a monotonic fall in the drain voltage (see Appendix A.3) Often, this gives rise to filament formation along the device width and failure of the device [15]. Electrothermal and self-heating in the ballast region can have a strong impact on the localization phenomenon due to nonuniform triggering of bipolar, as well as in the final stages of thermal runaway.

B. Twin Path on Injection Across the Surface and the Bulk

In summary, the process is principally governed by coupling of electron injection across two paths (see Fig. 10).

Path 1: This is critical for the initial turn-on of the parasitic bipolar formed below the thin oxide.

Path 2: This is critical for establishing a current path in the bulk, which is essential to sustain a strong snapback.

Thus, the bipolar snapback is initially triggered due to higher electron injection across path 1, which is eventually maintained through diffusive electron injection across path 2. The flow of electron injection across path 1 is established primarily due to the 2-D coupled electrostatics of the source and gate regions. However, electron injection into the bulk is relatively less impacted by the electrostatics of the gate region once the barrier is sufficiently lowered and triggers the onset of space-charge modulation (see Fig. 11).

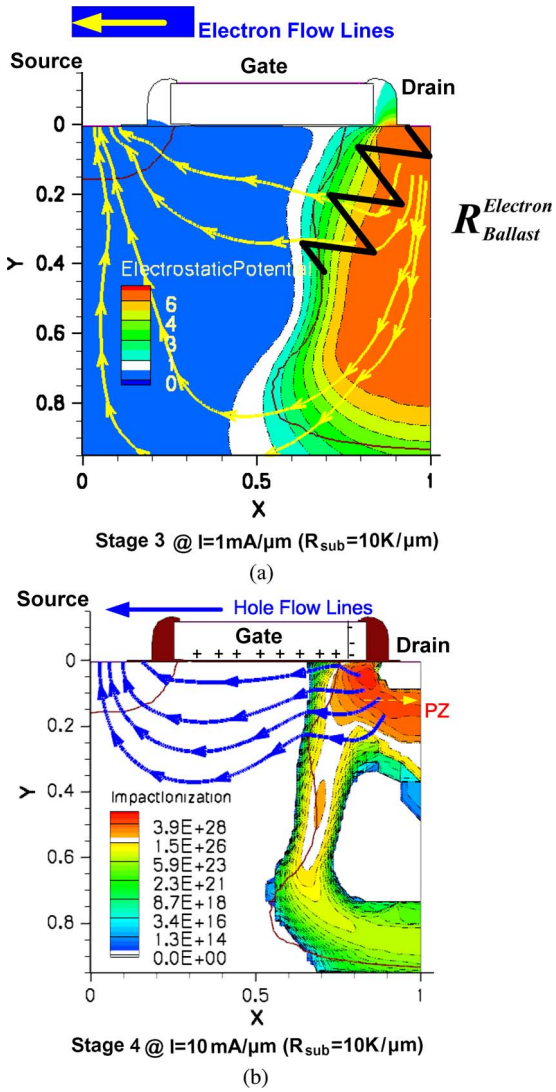

Fig. 9. Positive slope due to the ballast action of the space-charge region (stage 3).

C. Comparing a Single Snapback in a DENMOS With a Double Snapback in an NMOS

Thus, when $R_{\rm sub} = 0$ (i.e., no external substrate resistance is added), a strong snapback (i.e., the device goes to stage 1–stage 2–stage 4) is triggered at a higher current and a higher voltage when compared with the weaker snapback, which involves an additional stage 3. If the role of path 2 is ignored, the snapback mechanisms become identical to a regular n-p-n turn-on in a low-voltage NMOS [21]–[22]. Conventionally, the snapback in a low-voltage NMOS is characterized by a continuous decline in the E-field across the depleted junction, whereas at a higher current density, it leads to a voltage buildup ΔV across the space-charge region until extremely high current densities trigger the second snapback due to the onset of an avalanche injection phenomenon across the SCL nonlinear resistor R_2. In the process, the electrical instability-driven current filamentation or the "strong snapback" in the DENMOS is characterized by the simultaneity of the collapse of electron flow from the surface to the bulk, i.e., the switching of path 1→path 2, as it triggers strong avalanche injection across path 2, which is the critical phase in a current localization process (the comparison is summarized in Table I).

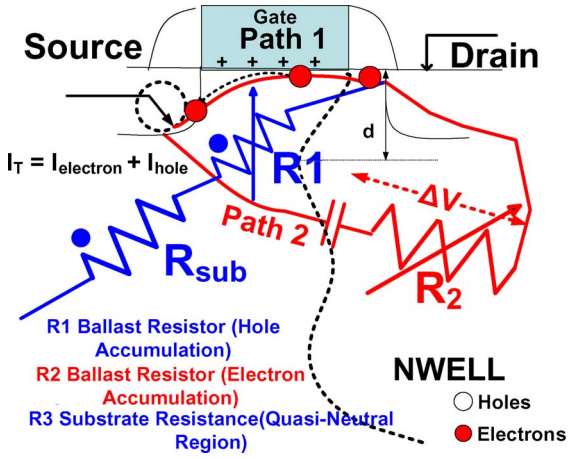

Fig. 10. Twin paths of electron injection. Path 1 is constituted due to channel injection, whereas path 2 is constituted due to bulk injection. The shift of electron injection modulates the ballast resistor R_1.

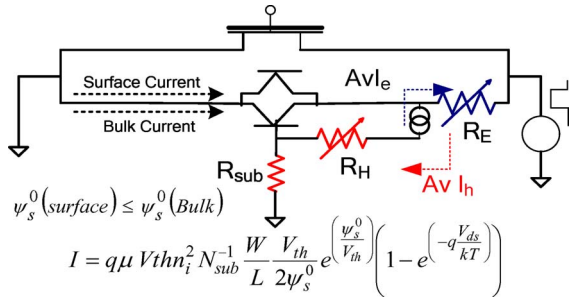

Fig. 11. Circuit model to represent thermal effects as the surface and bulk currents are impacted differently.

TABLE I
COMPARISON OF THE 2-D BIPOLAR PROPERTIES OF NMOS VERSUS DENMOS

		NMOS	DeNMOS
1	Switching Behavior Path 1-2	Higher I_e	Lower I_e
2	2D-Localization (PZ)	Lower	Higher
3	Flow of holes	$R_{substrate}$	P-Well Implants
4	FunnelAngle (θ)	Large	Small
5	$R_{EBallast}$ (Stage 3) (2D Effect)	Prominent	Either Missing/ Temperature Dependent
6	Snapback	Double	Merged

IV. Analysis of Experiments: Corroborating the Model

Thus, filamentation causing failure can be attributed to current localization during space-charge modulation as the drain region behaves as a ballast resistor due to SCL transport of avalanche-generated carriers at a critical low current density.

The model is next corroborated through a detailed analysis of the following experiments.

1) *Independence of a strong snapback on the pulse rise time* dv/dt: The device shows a lack of dv/dt dependence when tested under a TLP setup. The simulated I–V curve shows that the preballast region (i.e., stage 0) is determined by the magnitude of the displacement current under the transient simulation.

   As the displacement current subsides and the device goes into the presnapback region, a jump (or a kink) is observed (see Fig. 5). However, in the hole ballast (presnapback region stage 1), there is a marginal impact on the speed of the ramp, whereas the slope is determined by the ballast action due to localization of the hole current in the drain region. This also confirms our experimental observation that the current-controlled phenomenon is marginally impacted by the ramp speed.
2) *Avoiding filamentation through the abutment of the source and the substrate:* The turn-on path of the parasitic bipolar in the DENMOS can be changed by abutting the source and the substrate contact in the device. The lack of electron injection across path 1 (see Fig. 10) can restrict current localization and alleviate the onset of space-charge modulation or avalanche injection in the process, which can prevent the onset of isothermal filament formation.

V. Conclusion

We have presented the failure analysis of a nanometer-scale DENMOS under an ESD event. Through detailed TCAD-based transient simulations, we have investigated the 2-D electrostatics of the drain region and analyzed the high-current ballast action under SCL conditions. We have demonstrated the bipolar-driven snapback action at different stages under excessive current localization in the drain region, which eventually leads to different bipolar paths after bipolar triggering. This paper demonstrates the possible role of avalanche injection through various parasitic paths (i.e., flipping in the dominant bipolar conduction path) causing electrical instability, which may eventually lead toward current filamentation. An analytical model that is established for the critical stages will help develop a compact model for understanding the dynamical bipolar turn-on.

Appendix

A. Ramp Rate Dependence

The ramp rate dependence is given as

$$I_{\mathrm{Ramp}} = I_{\mathrm{Displacement}} + I_{\mathrm{Recombination}} + I_{\mathrm{Breakdown}}.$$

In the prebreakdown region, $I_{\mathrm{Displacement}} \gg I_{\mathrm{Breakdown}}$, whereas in the hole ballast region, $I_{\mathrm{Displacement}} \ll I_{\mathrm{Breakdown}}$.

The device voltage in the preballast region for a faster ramp speed is given by (2), whereas recombination-limited slower ones obey (3) in the prebreakdown region (as shown in Fig. 5),

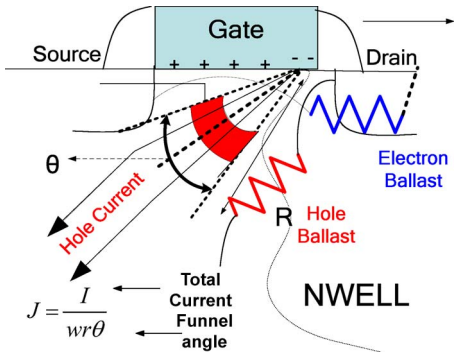

Fig. 12. Potential distribution due to the flow of holes, which shows a linear rise in the device voltage.

where W is the depletion width, and τ is the average carrier lifetime of holes and electrons. Thus

For faster ramps :

$$\underset{\text{Displacement}}{\frac{d(\varepsilon_0 E)}{dt}} = I_{\mathrm{ramp}}t + I_{\mathrm{rev}} - \underset{\text{Recombination}}{N_i \frac{W}{\tau}} \tag{1}$$

$$V \approx \left(\frac{qN_a}{2\varepsilon_0}\right)\left(\frac{I_{\mathrm{rmp}}t^2}{2qN_a}\right)^2 \approx \left(\frac{I^2}{2qN_a I_{\mathrm{rmp}}}\right)^2 \tag{2}$$

For slower ramps :

$$V \approx \left(\frac{qN_a}{2\varepsilon_0}\right)W^2 = \left(\frac{qN_a}{2\varepsilon_0}\right)\left(\frac{I\tau}{A}\right)^2 \quad I = I_{\mathrm{ramp}}t = A\frac{W}{\tau}. \tag{3}$$

B. Modeling a Ballast Resistor Due to the Flow of Holes

In the hole ballast regime, the current is primarily dominated by the avalanche-generated holes and electrons. The flow of avalanche-generated holes establishes a space-charge region near the n^+ drain diffusion region, which defines the buildup of drain voltage and can be modeled as a nonlinear resistor. In Fig. 12, I_{hole} is the hole current injected into the substrate, and r is the depth where the electron concentration due to the SCL current is equal to the background concentration N_B. Thus, the ballast resistor $R_{\mathrm{H\text{-}Ballast}}$ due to hole accumulation exhibits a fall in the drain voltage (see Fig. 3).

C. Modeling an Avalanche Injection Phenomenon in a Ballast Resistor Due to the Flow of Electrons

The physics of a snapback in the DENMOS is intricately related to avalanche injection across the 2-D nonlinear resistor in the drain region (see Section III, stage 4 of the bipolar turn-on). As the electron current density increases, the parasitic bipolar turns on completely, the impact of hole flow into the substrate can be neglected, and a strong snapback in the n-p-n structure can be approximated through a quasi-steady simulation of an n^-/n^+ resistive slab.

The drain region initially shows a nonlinear resistive behavior (i.e., a ballast action due to electron flow). However, at a higher current at a critical density, i.e., J_{critical}, it exhibits space-charge modulation. In this section, we analyze the

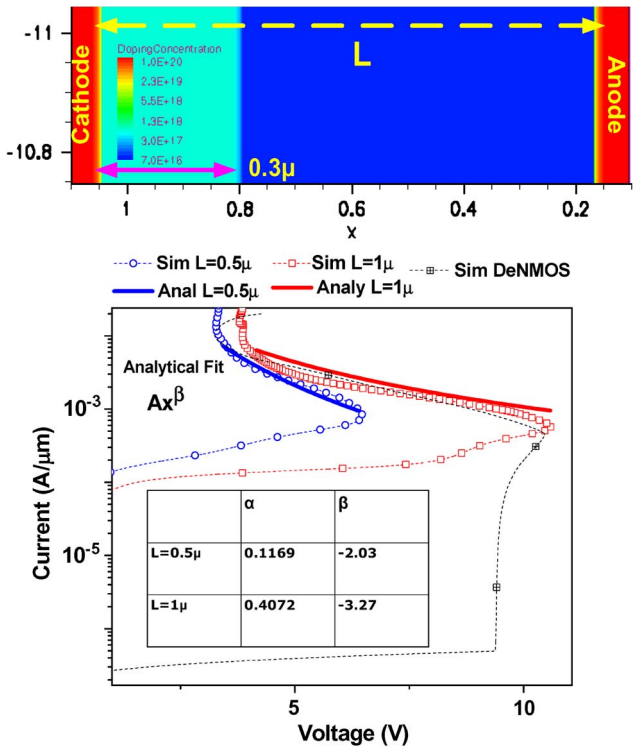

Fig. 13. The quasi-steadily simulated I–V curve shows a nonlinear resistive behavior, which triggers a snapback at a critical value of the current density J_{critical}.

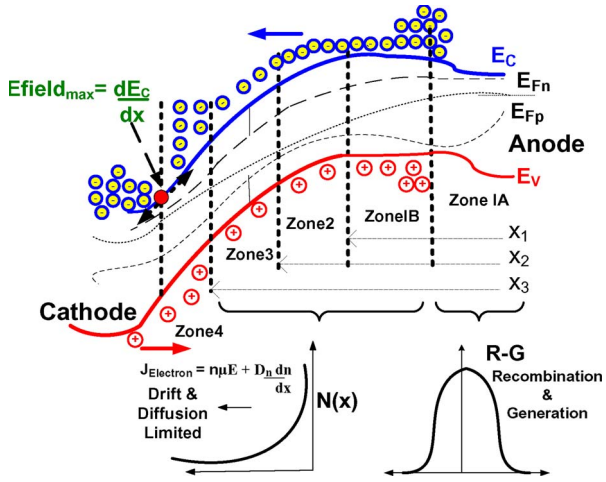

Fig. 14. Band diagram showing the contribution of the net current due to both electron and hole flows. The maximum multiplication factor is achieved when $J_{\text{Electron}} = J_{\text{Hole}}$ across zone 3 (region of saturated drift velocity).

snapback of a 1-D resistive slab (a low-doped n^-/n^+) during heavy charge modulation as follows:

$$\nabla \cdot \vec{E} = \frac{\rho}{\varepsilon_{\text{si}}} = \frac{J}{\varepsilon_{\text{si}} V_S} \tag{4}$$

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \Phi}{\partial r}\right) = \frac{I}{\varepsilon_{\text{si}} r \theta V_S} \tag{5}$$

$$R_{\text{H-Ballast}} = \frac{\Phi}{I} = \frac{1}{\varepsilon_{\text{si}} \theta V_S}. \tag{6}$$

1) Avalanche Injection Across an SCL 1-D Resistor: Now, as the current density increases, the I–V curve (see Fig. 13) makes a transition from an ohmic regime into a regime of

TABLE II
SUMMARY OF THE TRANSPORT MECHANISM OF CARRIERS ACROSS DIFFERENT ZONES OF AN n^-/n^+ RESISTIVE SLAB

	Electrons	Holes
Zone1A Zone1B (x1)	Diffusion	Recombination
	Diffusion	Drift
Zone2 (x2)	Drift	Drift
Zone3 (x3)	V_{sat}	V_{sat}
Zone4 (x4)	V_{sat}	V_{sat}

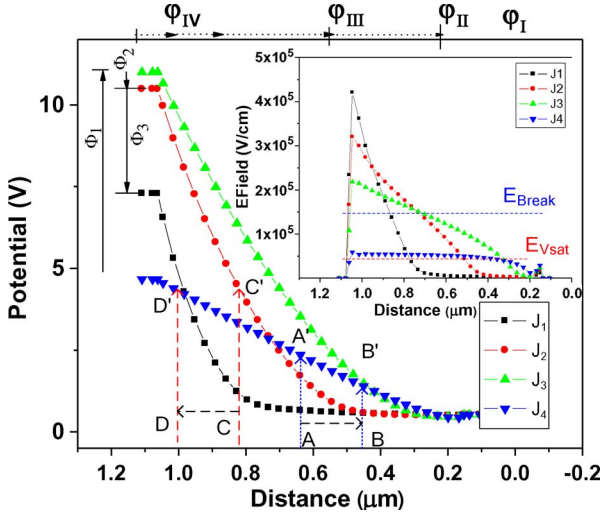

Fig. 15. Potential Distribution showing non-linear resistive behavior in the 1D showing an expansion in zone 4 (avalanche) AA→BB (when $J_1 \rightarrow J_{\text{critical}}$) and a shrinking of zone 2 (drift) CC→DD (when $J_2 \rightarrow J_{\text{critical}}$). (Inset) Showing E-Field distribution. Snapback is observed when an increase in potential across zone 4 is less than drop in potential other zones (10).

SCL transport [13], [26], [27]. The energy band diagram (see Fig. 14) shows that avalanche-generated holes drift under the field established due to injected electrons. The transport mechanisms of carriers are summarized in Table II. As the space charge of avalanche-multiplied electrons increases, the voltage across the slab increases first, which works as a ballast resistor. However, beyond the positive nonlinear slope, a snapback is triggered in the n^-/n^+ resistor [23]–[30]. An analytical model, which has been established, has been compared with simulation of the structure.

2) Understanding the Snapback Voltage in an n^-/n^+ Resistive Slab: Avalanche injection plays a critical role in a strong snapback in the DENMOS, where the SCL resistor first exhibits a buildup of voltage and then a snapback as the potential across the device falls. Thus

$$\frac{d^2E}{dx^2} = \frac{q}{\varepsilon_{\text{si}}}\left(\frac{dp}{dx} - \frac{dn}{dx}\right) = \frac{1}{\varepsilon_{\text{si}}}\frac{d\rho}{dx} \tag{7}$$

$$\varepsilon_{\text{si}}\frac{d^2E}{dx^2} = \rho\frac{d\rho}{dx} = \frac{2\varepsilon}{V_s} J\alpha \begin{bmatrix} J = J_n + J_p \\ p = \frac{J_p}{V_s}, n = \frac{J_n}{V_s} \\ \alpha(E) = aE^n [\text{EmpiricalModel}] \end{bmatrix}. \tag{8}$$

The structure (see Fig. 13) first exhibits an SCL positive slope (ballast action) until, at a critical current density, a snapback is

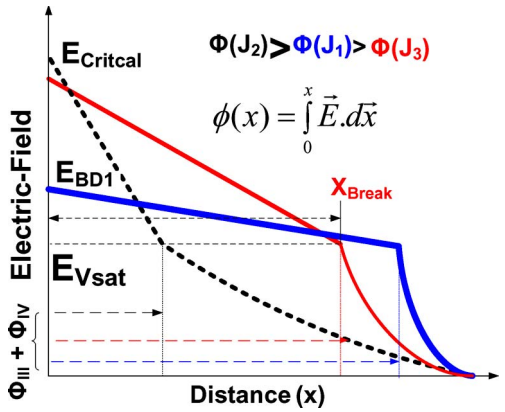

Fig. 16. E-field distribution under high-current conditions, where the peak E-field continues to increase at contact and the injection of holes modulates the E-field in the bulk.

triggered. Thus, under strong avalanche injection, accumulated holes efficiently modulate the E-field due to injected electrons, which enhances the length over which electrons can diffuse and increases the transit time of average electron–hole pair or ambipolar transit time. At any voltage, the injected plasma concentration builds up to the point where, approximately, the pair transit time is equal to the pair lifetime, i.e.,

$$\frac{dE}{dx} = \left[\frac{4J}{V_S \varepsilon_{\rm si}} \frac{a}{n+1}\left(E^{n+1} - E_m^{n+1}\right)\right]^{\frac{1}{2}} \tag{9}$$

$$\left.\frac{\partial \Phi}{\partial I}\right|_{I+\rm II} + \left.\frac{\partial \Phi}{\partial I}\right|_{\rm III+IV} = 0. \tag{10}$$

Moreover, the second term in (9) can be neglected under strong injection, and at a certain stage, the potential across the structure begins to fall when the condition in (10) is met. Once the snapback is triggered, we make an approximation that the peak E-field is pinned at E_c, whereas $x_{\rm break}$ decreases. Now, under modulation of space charge by the reverse-injected holes, the distance $x_{\rm break}$ over which the critical breakdown field E_c is established reduces (see Fig. 16). Thus

$$E_c = \left[\frac{4J}{V_S \varepsilon_{\rm si}} \frac{a}{n+1}\right]^{\frac{1}{2}} x_{\rm break}^{\frac{2}{1-n}} \tag{11}$$

Therefore, the $x_{\rm break}$ distance for the critical E-field E_c can be defined from

$$x_{\rm break} = \frac{V_s}{J}\left[\varepsilon_{\rm si}\frac{(n+1)}{4a}\right] E_c^{\frac{1-n}{2}}. \tag{12}$$

Therefore, the potential V across the slab can be estimated by integrating the following:

$$V = \int_0^{\rm xbreak} E \cdot dx \tag{13}$$

$$V = K^{\frac{2-n}{n}} \frac{\Gamma\left[\frac{n-2}{n-1}\right]}{\Gamma\left[2 - \frac{2}{n-1}\right]}. \tag{14}$$

Therefore, the expression can be reduced to allometric form using the gamma function Γ, i.e.,

$$V = \text{const} \cdot I^{\frac{2-n}{2}} = \text{const} \cdot I^{\beta}. \tag{15}$$

ACKNOWLEDGMENT

The authors would like to thank Dr. P. Hower from Texas Instruments for technical discussions and S. Krishnamurthy from Synopsys for help with the simulations.

REFERENCES

[1] J. Mitros, C. Y. Tsai, H. Shichijo, K. Kunz, A. Morton, D. Goodpaster, D. Mosher, and T. Efland, "High voltage drain-extended devices for 0.18 mm digital CMOS process," in *Proc. ESSDERC*, 2000, pp. 376–379.

[2] R. M. Steinhoff, J. B. Huang, P. L. Hower, and J. S. Brodsky, "Current filament movement and silicon melting in an ESD-robust DENMOS transistor," in *Proc. ESD/EOS Symp.*, 2003, pp. 1–10.

[3] G. Boselli, V. Vassilev, and C. Duvvury, "Drain extended NMOS high current behavior and ESD protection strategy for HV Applications in sub-100 nm CMOS technologies," in *Proc. IRPS*, 2007, pp. 342–347.

[4] S. Pendharkar, T. Reggatz, J. Devore, J. Carpenter, and T. Efland, "SCR-LDMOS. A novel LDMOS device with ESD robustness," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2000, pp. 341–344.

[5] M. P. J. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker, and W. Fichtner, "Analysis of lateral DMOS power devices under ESD stress conditions," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2128–2137, Nov. 2000.

[6] M. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker, and W. Fichtner, "Analysis and compact modeling of lateral DMOS power devices under ESD stress conditions," in *Proc. ESD/EOS. Symp.*, 1999, pp. 1–10.

[7] H. Gossner, T. Muller-Lynch, K. Esmark, and M. Stecher, "Wide range control of the sustaining voltage of ESD protection elements realized in a smart power technology," in *Proc. ESD/EOS Symp.*, 1999, pp. 19–27.

[8] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, A. Bose, and R. Ida, "A double RESURF LDMOS with drain profile engineering for improved ESD robustness," *IEEE Trans. Electron Devices*, vol. 23, no. 4, pp. 212–214, Apr. 2002.

[9] A. J. Walker, H. Puchner, and S. P. Dhanraj, "High-voltage CMOS ESD and the safe operating area," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1753–1760, Aug. 2009.

[10] A. Chatterjee, S. Pendharkar, Y.-Y. Lin, C. Duvvury, and K. Banerjee, "An insight into the high current ESD behavior of drain extended NMOS (DENMOS) devices in nanometer scale CMOS technologies," in *Proc. IRPS*, 2007, pp. 608–609.

[11] A. Chatterjee, S. Pendharkar, Y.-Y. Lin, C. Duvvury, and K. Banerjee, "A microscopic understanding of DENMOS device failure mechanism under ESD conditions," in *IEDM Tech. Dig.*, 2007, pp. 608–609.

[12] A. Chatterjee, H. Gossner, S. Pendharkar, C. Duvvury, and F. Brewer, "Robust high current ESD performance of nano-meter scale DeNMOS by source ballasting," in *Proc. IRPS*, 2010, pp. 853–856.

[13] A. Chatterjee, R. D. Schrimpf, S. Pendharkar, and K. Banerjee, "Mechanisms leading to erratic snapback behavior in bipolar junction transistors with base emitter shorted," *J. Appl. Phys.*, vol. 97, no. 8, pp. 084504-1–084504-8, Apr. 2005.

[14] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, and V. R. Rao, "On the failure mechanism and current instabilities in RESURF type DeNMOS device under ESD conditions," in *Proc. IRPS*, 2010, pp. 841–845.

[15] M. Shrivastava, H. Gossner, M. S. Baghini, and V. R. Rao, "Part II: On the 3D filamentation and failure modeling of STI type DENMOS Device under ESD Conditions," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2243–2250, Sep. 2010.

[16] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part I: Mixed-signal performance of various high-voltage drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[17] V. A. Vashchenko and V. F. Sinkevitch, *Physical Limitations of Semiconductor Devices Defects, Reliability and ESD Protection*. New York: Springer-Verlag, 2008.

[18] M. Denison, M. Blaho, P. Rodin, V. Dubec, D. Pogany, D. Silber, E. Gornik, and M. Stecher, "Moving current filaments in integrated DMOS transistors under short duration current stress," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1695–1703, Oct. 2004.

[19] E. R. Worley, "New ballasting method for MOS output drivers and power bus clamps," in *Procs. IRPS*, 2005, pp. 458–461.

[20] M. Ker and K. Lin, "Double snapback characteristics in high-voltage nMOSFETs and the impact to on-chip ESD protection design," *IEEE Electon Device Lett.*, vol. 25, no. 9, pp. 640–642, Sep. 2004.

[21] V. Vassilev, M. Lorenzini, and G. Groeseneken, "MOSFET ESD breakdown modeling and parameter extraction in advanced CMOS technologies," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2108–2117, Sep. 2006.
[22] J. B. Gunn, "Avalanche injection in semiconductors," *Proc. Phys. Soc. B*, vol. 69, no. 8, pp. 781–790, Aug. 1956.
[23] Prof Umesh Mishra, Private Discussion.
[24] M. Domeij, B. Breitholtz, J. Linnros, and M. Ostling, "Avalanche injection in high voltage Si PiN diodes measurements and simulation," in *Proc. ISPSD Conf.*, 1997, pp. 125–128.
[25] P. L. Hower and V. G. Krishna Reddi, "Avalanche injection and second breakdown in transistors," *IEEE Trans. Electron Devices*, vol. ED-17, no. 4, pp. 320–335, Apr. 1970.
[26] M. A. Lampart and P. Mark, *Current Injection in Solids*. New York: Academic, 1970, p. 285.
[27] P. Hower, C.-Y. Tsai, S. Merchant, T. Efland, S. Pendharkar, R. Steinhoff, and J. Brodsky, "Avalanche-induced thermal instability in LDMOS transistors power semiconductor devices and ICs," in *Proc. ISPSD Conf.*, 2000, pp. 153–156.
[28] P. Hower, S. Pendharkar, R. Steinhoff, J. Brodsky, J. Devore, and W. Grose, "Using two-dimensional structures to model filamentation in semiconductor devices," in *Proc. ISPSD Conf.*, 2001, pp. 385–388.
[29] V. A. Vashchenko, Y. B. Martynov, and V. F. Sinkevitch, "Simulation of avalanche injection filamentation in MOSFETs and IGBTs," in *Proc. ESSDERC*, 1997, pp. 316–319.
[30] G. Boselli, "On high injection mechanisms in semiconductor devices under ESD condition," Ph.D. dissertation, Twente Univ., Enschede, The Netherlands, 1999.

Amitabh Chatterjee, photograph and biography not available at the time of publication.

Mayank Shrivastava (S'09–M'10), photograph and biography not available at the time of publication.

Harald Gossner (M'06), photograph and biography not available at the time of publication.

Sameer Pendharkar (SM'06), photograph and biography not available at the time of publication.

Forrest Brewer (M'87), photograph and biography not available at the time of publication.

Charvaka Duvvury (F'07), photograph and biography not available at the time of publication.