An Insight Into ESD Behavior of Nanometer-Scale Drain Extended NMOS (DeNMOS) Devices: Part II (Two-Dimensional Study-Biasing & Comparison With NMOS)

Amitabh Chatterjee, Mayank Shrivastava, *Member, IEEE*, Harald Gossner, *Member, IEEE*, Sameer Pendharkar, *Senior Member, IEEE*, Forrest Brewer, *Member, IEEE*, and Charvaka Duvvury, *Fellow, IEEE*

***Abstract*—In this paper, we present an analysis of drain extended n-channel metal–oxide–semiconductor (DeNMOS) and study the impact of both substrate and gate biasing on the regenerative avalanche injection phenomenon at the edge of drain contact. We will demonstrate that the flow and distribution of avalanche-generated holes and electrons are significantly impacted by biasing the gate and pumping current through the substrate. Finally, we show that gate bias or drain bias, when individually applied, can only lead to marginal improvement in It_2; however, when both the biases are applied simultaneously, it can then optimally improve the failure performance. Subsequently, we compare high current performance of DeNMOS with NMOS or swapped DeNMOS configuration through a simplified 1-D macroscopic model.**

***Index Terms*—Ballast, electrothermal runaway, filamentation, regenerative turn-on, transmission line pulsing.**

I. Introduction

HIGH-VOLTAGE interface and other mixed-signal applications require integration of high-voltage transistors in a low-voltage complementary metal–oxide–semiconductor (CMOS) technology. The drain-extended n-channel metal–oxide–semiconductor (DENMOS) (Fig. 1, Part I) is a high-voltage device that can be easily integrated with standard nanometer-scale CMOS process flow by adding an n-well extension at the drain side of a regular NMOS. However, the addition of an n-well process on standard CMOS process makes it particularly susceptible to electrostatic discharge (ESD) events [1]–[6]. In a DENMOS, the drain extension improves the device reliability by lowering the peak electric field below the gate in the drain region. Recently, a microscopic model for destructive snapback in different DENMOSs has been linked to both the Kirk phenomenon and thermal effects [1]–[5], [7]–[9]. In the past, this poor It_2 was believed to be due to low parasitic n-p-n gain [6]. However, the role of the macroscopic parameter in triggering parasitic bipolar, which can affect the permanent damage of the device, is still not very well understood. On the other hand, biasing techniques (i.e., gate or substrate) are often used in the protection devices in order to improve the level of the individual device, as well as the overall protection concept. However, basic physics of n-p-n turn-on under *second snapback* or *filamentation* regime in these biased structures is not well understood.

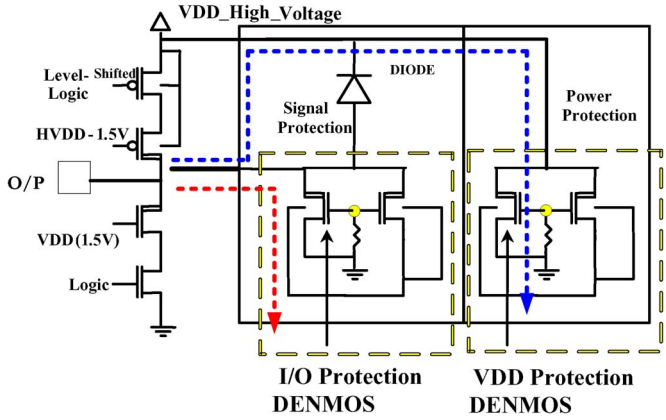

Fig. 1. Biased I/O circuit showing the discharge path for positive and negative ESD strike as it gets clamped to the power or ground rail so the current flows.

So far, phenomenological understanding indicates a general lack in the interpretation of the phenomenon in terms of macroscopic parameters defining the failure of drain-extended metal–oxide–semiconductor (MOS) devices.

Damage in DeNMOS is defined through current inhomogeneity due to nonuniform conduction in an array of 2-D bipolar, which leads to current localization or filamentation in the 3-D [3]–[5]. This transition from uniform turn-on to the process of localization requires an in-depth study of the 3-D electrothermal behavior. Moreover, the 3-D modeling comes with large overhead in terms of both numerical consistency and computational requirement. Therefore, it is useful to first do exhaustive understanding of the 2-D electrothermal behavior and then look at the ensemble behavior of an array of 2-D bipolar as one investigates the problem in 3-D.

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A. Chatterjee and F. Brewer are with the Department of Electrical Engineering, University of California, Santa Barbara, CA 93106 USA (e-mail: amitabh@ece.ucsb.edu; forrest@ece.ucsb.edu).

M. Shrivastava and H. Gossner are with the Infineon Technologies AG, 81726 Munich, Germany (e-mail: shrivastva.mayank@gmail.com; Mayank.Shrivastava@infineon.com; harald.gossner@infineon.com).

S. Pendharkar and C. Duvvury are with Silicon Technology Development, Texas Instruments, Dallas, TX 75243 USA (e-mail: s-pendharkar1@ti.com; c-duvvury@ti.com).

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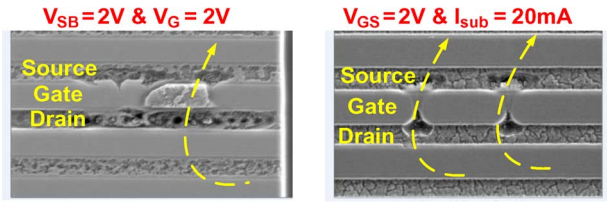

Fig. 2. SEM micrograph showing damage in different biasing schemes of DENMOS with (a) the gate and substrate grounded and (b) $V_{gs} = 2$ V and $I_{\rm sub} = 30$ mA.

The purpose of this paper is to present a critical understanding and to analyze the impact of applying gate bias and pumping substrate current on the failure current of drain-extended MOS devices. The role of gate biasing and/or substrate pumping with its impact on alleviating the onset of space charge modulation has been discussed. The detailed microscopic understanding of alleviation of current crowding or space charge modulation mechanisms presented in this paper will help to improve the ESD robustness of the input/output (I/O) circuits comprising DENMOS devices (Fig. 1). Generic models established in this paper will be extremely critical for building compact models for designing I/O circuits in future nanometer-scale technologies using both NMOS and DeNMOS devices. Moreover, generalized understanding of the 2-D behavior of such devices will be extremely helpful in building circuit models, for both NMOS and DeNMOS devices, which can define their ESD behavior.

II. Modeling the Impact of Gate and Substrate Biasing

Biasing the gate and substrate of a DeNMOS slightly improves the failure performance. Failure analysis of failed devices under ESD event (Fig. 2) shows that a drain–source filament is formed, contrary to the expected failure along the drain–substrate junction if the n-p-n had not been turned on. Similarity of the failure mechanism under gate-grounded condition with that under biased condition points toward the role of bipolar turn-on in defining the path of current conduction after the bipolar turns on.

Under an ESD event, the device, which is in a gate-grounded configuration, turn-on is limited by subthreshold injection (leakage under gate-grounded condition) across path 1 (i.e., source injection). The device subsequently fails as the bipolar turns on and triggers current localization due to holes near the surface and eventually causes space charge modulation. In this dynamic two-stage process, in the first stage, subthreshold source (path 1) (Fig. 3) injection leads to an increased voltage buildup across the ballast region as the holes accumulate under the gate. In the process, the ballast action prevents base pushout effect in the parasitic bipolar. Subsequently, increased electron injection (at higher TLP current) modulates the e-field, which helps to lower the hole current density and leads to regenerative base pushout-driven current filamentation, as the device fails. However, under biasing (substrate and gate), the emitter of the parasitic BJT can be turned on prior to an ESD event, which alleviates the current localization during the critical turn-on phase. Under the biased condition, injection of minority carriers, which is evenly distributed (i.e., electrons), prevents

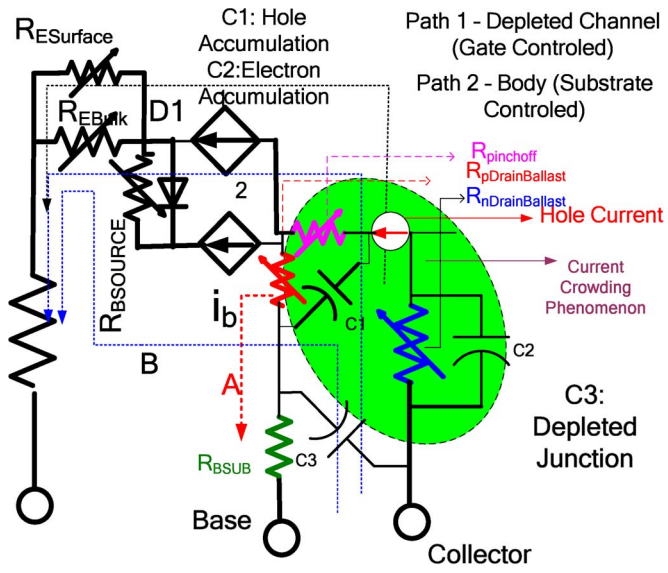

Fig. 3. Equivalent configuration of strong snapback and biasing eliminates path 1 while the role ballast resistor R is mitigated.

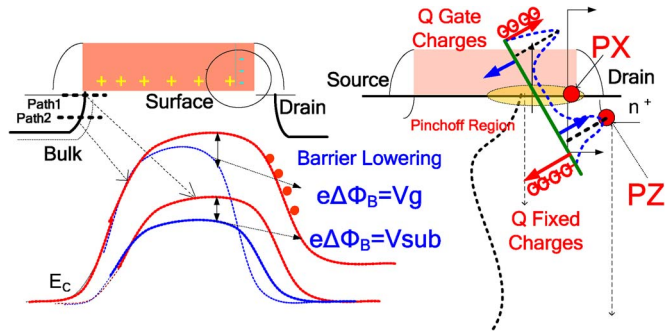

Fig. 4. (i) Energy barrier at the source end inside the bulk. (ii) Pockets of peak electric field.

excess buildup of voltage and also keeps the device away from unsafe space charge modulation regime. Moreover, under the biased conditions, modulation of the depletion field in the bulk (under breakdown condition) is less prominently observed when compared to the gate-grounded structure. The space charge modulation is triggered mainly due to the avalanche injection phenomenon at higher TLP current in the region across PZ, where the electric field peaks due to increased electron current. Eventually, at a critical current density, it leads to a phenomenon, i.e., base-out effect in 1-D, which triggers *isothermal filamentation* (Fig. 2) [10]–[12]. The role of individual gate and substrate bias influences the current distribution, and how their combined biasing strategy can be impacted by dual application of gate and substrate bias has been discussed in this section.

A. Gate Biasing Alleviates Current Crowding Due to Holes Near Surface (Drain Region)

Biasing the gate profoundly impacts the DeNMOS, whereas the gate biasing is known to have relatively less impact on the low-voltage NMOS [13]. Primarily, the gate bias impacts the barrier to the flow of electron near the surface at the source end. As the surface barrier is lowered at the source end, the minority carriers are injected into the channel (Fig. 5). However, this

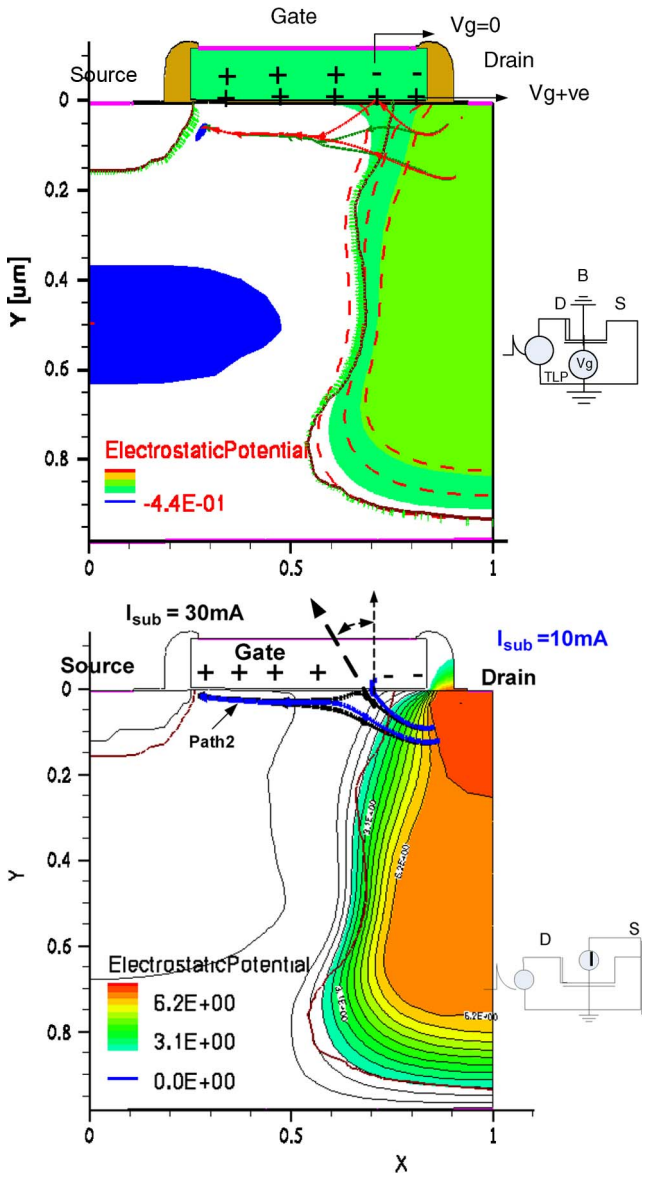

Fig. 5. (a) Electrostatic potential (field lines) under gate biasing shifts the pinchoff region to the left and is pushed below. (b) Under substrate biasing, the e-field lines near the pinchoff region are almost pinned to the surface.

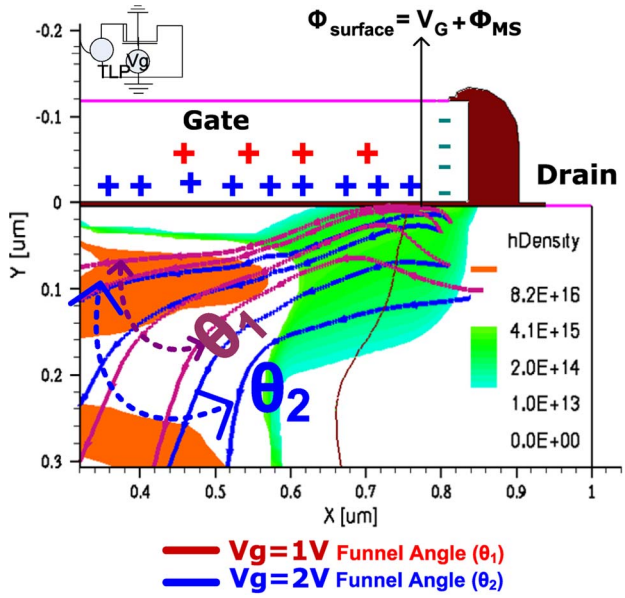

Fig. 6. Improved hole current density (*hence large funnel angle*) under gate biasing alleviates the current-crowding phenomenon, which helps prevent filamentation.

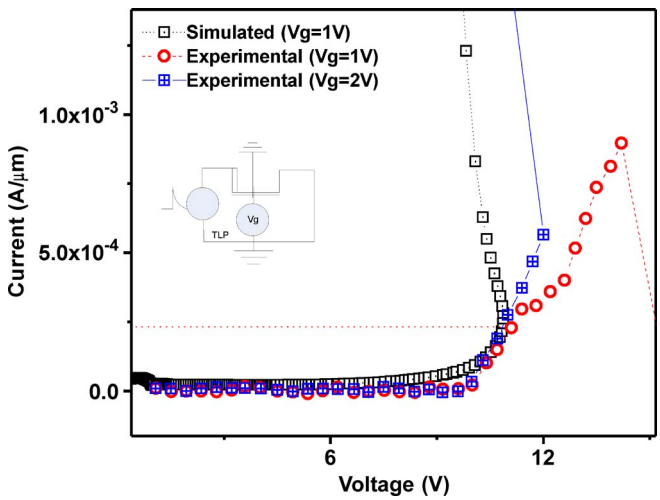

Fig. 7. TLP data compared to 2-D simulated I–V curve, which shows the impact of gate biasing and improvement in the failure current; however, lateral localization can result in a kink in the I–V curve.

results in excessive localization of hole current across the ballast region in the drain area (pinchoff region), which can be significantly improved by gate biasing. However, in the drain region, not only does positive gate bias push the hole toward the bulk but, in the process, electrons are also attracted toward the gate (Fig. 6). Thus, while the hole current density is alleviated below the drain region, electron current density is comparatively higher around region PZ, where the avalanche injection phenomenon is triggered after charge modulation.

Injection of nonlocalized or distributed holes deep in the bulk due to gate bias helps in triggering a greater number of 2-D parasitic bipolar in the array across the 3-D. This delays the onset of base pushout or charge modulation at a critical current density when compared to the gate-grounded structure (Fig. 7). However, as the gate voltage increases, failure current It_2 degrades, which can be attributed to the deleterious impact of gate biasing, i.e., higher electron current density around region PZ and also due to poor thermal performance as the hot spot activity shifts toward the gate (hence the reduced thermal capacitance). Excessive localization triggers thermal generation of carriers in the drain region, which, triggers device failure at critical current density due to regenerative processes under space charge modulation, principally involves thermal mechanisms.

B. Source Biasing Alleviates Current Crowding Due to Electron Flow in the Bulk (Drain Region)

Thus, a gate bias impacts the source–substrate barrier near the surface and efficiently turns on the injection across path 1 (Fig. 3). However, biasing the substrate lowers the barrier more prominently within the bulk, i.e., path 2 (Fig. 5). This leads to uniform and highly distributed (in the 2-D plane) injection of minority carriers into the bulk [Fig. 8 (inset)]. This helps in surviving the onset of current localization or the space charge

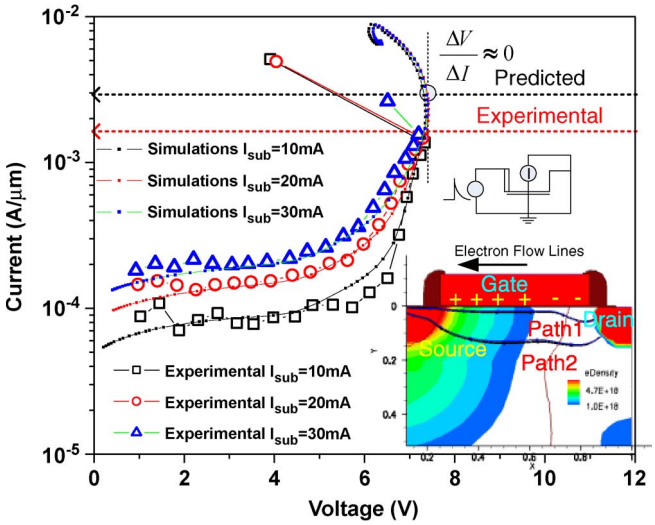

Fig. 8. I–V curve showing improvement in It_2 and e-density profile showing an improvement of electron flow into the bulk while it degrades the hole flow at the surface.

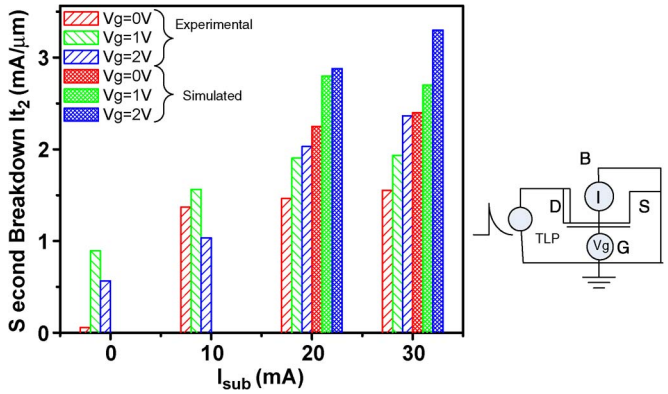

Fig. 9. I–V curve showing improvement in failure current under dual application of gate and substrate bias and impact of biasing experiments and simulation showing improvement in failure under dual application of gate and substrate biasing.

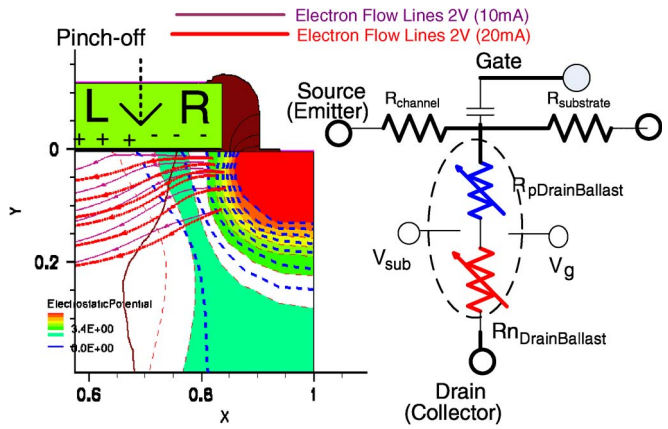

Fig. 10. Better flow lines under dual application of gate and substrate bias alleviate the avalanche injection phenomenon.

modulation around the drain contact, which is the region around PZ (Fig. 4).

Thus, just like gate biasing, under substrate biasing, avalanche-generated carriers due to the source injection, which initially provides a *ballast action* across the drain region, can be attributed to both the accumulated electrons across the drain contact and the holes, which get accumulated under the gate (Fig. 4). However, at a critical electron current density (still higher compared to that in gate-grounded condition), snapback is triggered, which is the onset of current filamentation and failure in 3-D [4], [5]. Under these conditions, the source injects an electron into the substrate for each hole, which is generated around the drain region and marks the onset of the negative resistance regime on the device I–V curve (Fig. 8); thus, the current value at which $dV/dI(\text{slope}) = 0$ becomes the predicted It_2 value.

The unstable negative resistance region is similar to the second snapback observed in grounded-gate n-channel MOS (ggNMOS). However, since the first snapback (due to parasitic bipolar triggering) is less prominent in DeNMOS device (missing under substrate biasing), we also call it *strong snapback*.

To summarize, a higher electron current density causes the peak electric field across the edge of drain contact PZ to increase. At a critical current density, back-injected holes cause the potential across the device to fall. Thus, substrate biasing can play a critical role by alleviating the critical electron current density (for the onset of space charge modulation) around the drain contact, i.e., *region PZ*.

C. Design Consideration Biasing of Gate and Source Alleviates the Avalanche Injection Phenomenon

In a DENMOS, both the gate and substrate biasing can independently improve the It_2 (Fig. 9) by alleviating the critical current density for the onset of base pushout or space charge modulation. The gate bias primarily improves the flow of holes by distributing them deep into the bulk (Fig. 7); substrate bias alleviates the electron current density by reducing the overall potential buildup across the device. Thus, each biasing technique has an independent role to play in improving the current density, whereas, individually, they only have a limited impact on the performance. In fact, under gate bias, degradation in the It_2 performance is observed for higher gate bias. Moreover, the flow of carriers is coupled as the drift of electron is also determined by the electric field established due to the space charge of holes. Thus, electrons, which are first attracted by the gate [(left) region L], are also pulled up by the space charge due to hole accumulation, which are then forced toward the substrate [(right) region R] toward the contact (Fig. 10).

Their impact can be improved by a combined technique, which is also confirmed by the simulations, showing that an *improvement* in the ESD performance can be obtained by a combination of gate and substrate bias (Fig. 9). Thus, an optimal combination was achieved at a gate bias of 2 V and a substrate current of 20 mA. The optimal biasing technique thus minimizes the required gate bias and substrate current levels while it restricts the DeNMOS in the safe operating area.

III. 2-D Summary: Failure Performance NMOS Versus Strong Localization in DENMOS

Experiments were performed under gate-grounded condition in the DeNMOS in a configuration where the source–drain was swapped, and in the process, we apply a TLP pulse across the device, without the drain extension. In this configuration,

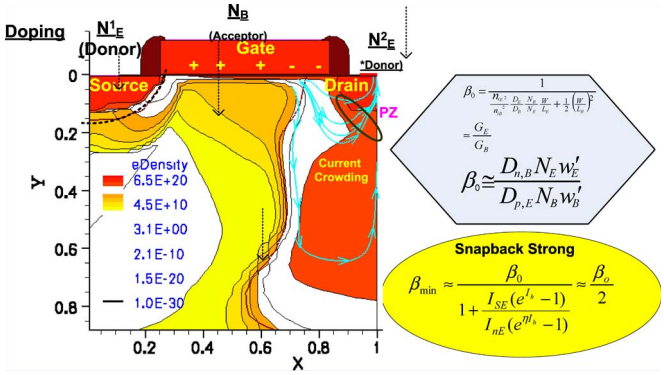

Fig. 11. Gain β of the parasitic bipolar, depending on gummel number, reaches a minimum value when the hole current is equal to the electron current.

the device showed similarities with a low-voltage NMOS, as the device survived thermal runaway due to lower current localization. Improved performance can be attributed to a simplified 1-D picture, primarily due to the absence of lowly doped n-well (subsided avalanche injection and less localization, Fig. 11). Due to this fact, it survives the space charge modulation or 1-D base pushout, which eventually helps in achieving higher It_2 similar to the ggNMOS. After the onset of charge modulation in the 2-D plane, the device fails due to filament formation in the 3-D [14]–[22]. Hence, the 2-D properties of the bipolars play a critical role in determining the ensemble conduction mechanism of the array of bipolar under high current stressing. The 2-D simulations show that, in a low-voltage NMOS, hole path is maintained across *path A*, even after n-p-n triggering. However, in the DeNMOS, once the bipolar turns on fully, the hole path shifts abruptly from drift-dominated path A to recombination-dominated path 2, and in the process, under strong snapback, the collapse is faster.

The 2-D bipolar in the DeNMOS shows high gate bias dependence when compared with a regular NMOS structure due to lower background n-well doping, which leads to stronger coupling between the gate and the n-well. Thus, it often shows an improvement when compared with regular low-voltage NMOS. Similarly, substrate biasing is known to have a stronger influence in a DeNMOS when compared with NMOS due to its higher influence on the electrostatics of the drain region (also determined by lower background doping concentration N_D).

Macroscopically, the bipolar physics is defined by gain β, which determines the fraction of drain current due to injected electrons (see Appendix). It plays a critical role, as the contribution of electron current, which determines the extent of localization in the 2-D plane. Therefore, the localization across PZ (Fig. 4) is strongly dependent on gain β (due to higher electron current density) of the 2-D bipolar (Fig. 11). Beyond It1 in the 2-D plane, the shift from PX $\rightarrow$ PZ for incremental increase in bipolar conduction in NMOS is gradual as the current begins to localize across PZ. As the bipolar turns on fully, the electron and hole path critically influence the process of localization in both DeNMOS and regular NMOS first in the 2-D plane [14]–[20]. In the event of strong localization, which leads to localized heating across, the device can have different distributions, depending on the current density $\vec{J}$ and electric field $\vec{E}$, i.e., $\vec{J}$ and $\vec{E}$ heating.

TABLE I
COMPARISONS OF NMOS VERSUS DeNMOS

		NMOS	DeNMOS
1	*Hole Path (Pre-snapback)*	PathA (fig. 3)	**PathA (fig. 3)**
2	*Hole Path (Post-snapback)*	PathA (fig. 3)	**Path2 (fig. 3)**
3	*Electron path (Pre-snapback)*	Path1 (fig. 3)	**Path1 (fig. 3)**
4	*Electron path(Post-snapback)*	Path1 (fig. 3)	**Path2 (fig. 3)**
5	*Snapback (shift PX-PZ)*	Gradual	**Abrupt**
6	*It1(Background Doping Dependent)*	Less	**High**
7	*Impact (Gate Bias)*	Low	**High**
8	*β (localization factor in 2D)*	Deteriotes/Improves (depending on heat distribution)	**Deteriotes**
9	*Temperature dependence on Holding Voltage*	Low	**High**

Therefore, in reverse configuration, the localization is much less in the 2-D plane and involves less self-heating. Moreover, it is often observed in low-voltage NMOS that increased current gain β improves the peak heat dissipation in the device as the total heat dissipation is alleviated, even though there is greater localization across PZ as the bipolar triggers.

To summarize (also summarized in Table I) the phenomenon, the addition of an n-well in a DENMOS exacerbates the 3-D localization phenomenon, which is due to early charge modulation in the 2-D plane. Now, for a low-voltage NMOS, under lesser localization or absence of charge modulation, the device can settle down to a steady-state value up to a much larger value of external current supply beyond its first snapback (onset of bipolar triggering), and subsequently, it triggers thermal runaway in the 3-D plane.

IV. CONCLUSION

In this paper, we have also shown a limited impact of biasing the gate and the substrate, where they can only marginally improve It_2. However, the current crowding behavior can be optimized under dual application of gate and substrate bias. Within limitations of the 2-D modeling, we have compared bipolar conduction mechanisms in DeNMOS with regular NMOS. We have compared the 2-D behavior, wherein the weak DeNMOS behavior can be interpreted.

APPENDIX

A. Modeling Macroscopic Parameters Under High Current Avalanche Injection

The avalanche multiplication factor M and bipolar gain β are two critical macroscopic parameters that give computer-aided-design designers a very useful design methodology for fitting spice models while designing an efficient ESD I/O protection circuits.

1) Miller Formulation for 1-D Current-Controlled Phenomenon: Role of the 2-D bipolar conduction mechanisms under avalanche injection can be reduced to a simplified 1-D process, which can be approximated under the assumption that, near the pinchoff region, for $x < x_{\text{pinchoff}}$ (region I), the hole current

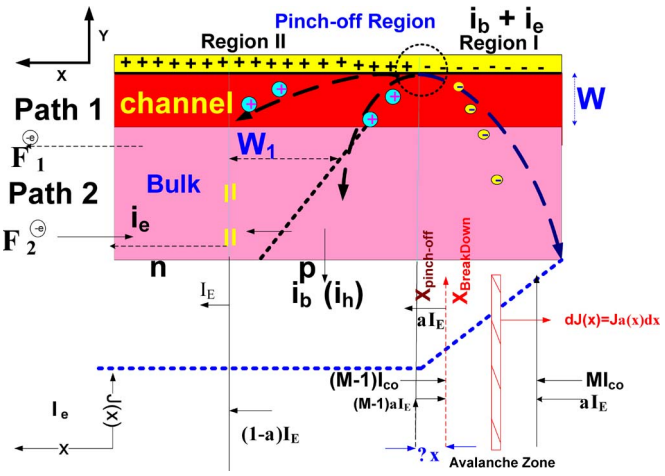

Fig. 12. Simplified 1-D model of the 2-D bipolar conduction phenomenon to build the circuit model. Width W of the channel and width W_1, which is the width of the source and substrate junctions, determine the recombination process due to hole injection.

J_h becomes dominant, whereas, for $x > x_{\text{pinchoff}}$ (region II), the electron current J_e becomes the dominant current Fig. 12.

In the process, a new formulation is desired similar to the Miller formulation, where we can model the current-controlled phenomenon that can be expressed in terms of current established in the circuit, through 1-D-empirical solution.

Miller formulation can be expressed as

$$1 - \frac{1}{M} = \int_0^W \alpha_i \exp\left[-\int_o^x (\alpha_i - \beta_i) dE'\right] dE \tag{1}$$

$$\alpha_i(E_M) = \frac{2}{W_1^2} \frac{d\left(1 - \frac{1}{M}\right)}{dE_M} \exp\left[\frac{1}{2} W_1^2 \int_0^{E_M} (\alpha_i - \beta_i) dx'\right] \tag{2}$$

$$\alpha = \frac{2n}{W_B} \left(\frac{E_B}{E_{\text{MB}}}\right)^n \exp\left(\frac{1}{2} W \int_0^E (\alpha - \beta) dx\right) \tag{3}$$

where α and β are the coefficient of impact ionization for holes and electrons, the electric field E_B is the maximum electric field distribution, and E_{MB} is the normalizing constant. Under this current-controlled avalanche injection model, the electric field peaks across the drain contact. Hence, as the bipolar conduction increases, the edge of avalanche breakdown shifts toward the n^-/n^+ junction in 1-D. Moreover, we assume that the distance between x_{pinchoff} and x_{br} is small, as the 2-D electric field increases and causes it to increase across the n^-/n^+ junction.

Now, localization in the 2-D bipolar physics can be reduced to a simplified 1-D model through the introduction of the current-dependent coupling factor α^*.

The current density $J(x)$ is defined as

$$J(x) = Ja\left[\frac{4J}{V_{\text{si}}\varepsilon_{\text{si}}} \frac{a}{n+1}\right]^{\frac{n}{2}} \int_0^x x^{\frac{2n}{n-1}} .dx = J^{\frac{n}{2}+1} \times \text{const} \times \int_0^x x^{\frac{2n}{n-1}} \times dx \approx J^{\frac{n}{2}+1} \times \text{const} \times x^3 \qquad (\text{n} \gg 1). \tag{4}$$

TABLE II
CURRENT DENSITY, ELECTRIC FIELD, AND POTENTIAL DISTRIBUTION AS A FUNCTION OF DISTANCE x

	Current-Density J(x)	*Electric Field $\vec{E}$ (x)*	*Potential ϕ (x)*
Region I	$\left[\frac{J_e}{\varepsilon_{si} V_s} x\right]^{\frac{2n}{n-1}}$	$\left[\frac{4J}{V_S \varepsilon_{si}} \frac{a}{n+1}\right]^{\frac{1}{2}} x^{\frac{2}{1-n}}$	$\left[\frac{4J}{V_s \varepsilon_{si}} \frac{a}{n+1}\right]^{\frac{1}{2}} \times (3-n) \times \frac{x^{\frac{3-n}{1-n}}}{1-n}$
Region II	$(n+p)V_s$	$\frac{(n-p)LV_s}{\varepsilon_{si}}$	$\frac{(n-p)L^2 V_s}{\varepsilon_{si}}$

Now, the voltage across the 1-D structure is given by

$$V = \underbrace{V_{\text{Br}}(1 - J_h \alpha^* \beta)}_{\text{Region II}} + \underbrace{K \beta^{1/2} J_h^{1/2}}_{\text{Region I}}. \tag{5}$$

A constant K can be obtained by solving (5) as

$$0 = \underbrace{V_{\text{Br}}(1 - J_{1h} \alpha^* \beta)}_{\text{Region II}} + \underbrace{K \beta^{1/2} J_{1h}^{1/2}}_{\text{Region I}}$$

$$K = V_{\text{Br}} \frac{(1 - J_{1h} \alpha^* \beta)}{\beta^{1/2} \sqrt{J_{1h}}}$$

where J_{1h} is the hole current at snapback Vt1

$$\text{The Bipolar Gain}(\beta) = \frac{i_e}{i_h}. \tag{6}$$

From the table, we obtain a relationship between the peak electric field and the peak potential, i.e.,

$$E_B = J_e^m (V_B)^{\frac{n-1}{n}} \tag{7}$$

$$M = \frac{1}{1 - \left(\frac{J_e}{J_{\text{Be}}}\right)^k \left(\frac{V_B}{V_{\text{BE}}}\right)^n}. \tag{8}$$

Therefore, the classical Miller formulation [23] is modified by a term comprising electron current density under the current-controlled model (Table II).

2) Relationship Between Gain β and Multiplication Factor M Under Current-Controlled Avalanche Injection Phenomenon: Physics of bipolar-driven snapback, due to the current-controlled avalanche injection process, leads to the 2-D-bipolar conduction mechanism. Thus, it can be analyzed in a method similar to describing the empirical process of avalanche breakdown in 1-D bipolar devices [24] by assuming that the base current I_B is maximum just at the onset of snapback, i.e., there is no incremental increase in the base current for added avalanche-generated holes into the substrate I_{sub}. Therefore, beyond this point, incremental increases in base current (due to the flow of holes I_h) and multiplication factor M (as both the mechanisms hold simultaneously) are negligibly small, i.e.,

$$I_{\text{Drain}}(\text{collector}) = I_{\text{sub}}(\text{Base}) + I_{\text{Source}}(\text{Emitter}). \tag{9}$$

Therefore, voltage drop across the substrate $(\text{V}) = \text{R}_{sub}\text{I}_h \& \gamma_{1e}$ and γ_{1h} are coupling factors for electrons and holes across path 1, while γ_{2e} and γ_{2h} are coupling factors

for electrons and holes across path 2 (10)–(12b), shown at the bottom of the page. As the bipolar turns on, the dependence of the bipolar gain on the hole current increases, wherein the flow of holes [across path 1, which is below the channel (Fig. 12)] reduces the gain of the transistor. Moreover, while understanding 2-D bipolar behavior, the recombination process of the hole current can be neglected for the holes injected into the substrate (i.e., path A). Therefore, the current gain begins to decrease as the channel opens up (width W) and the holes are swept into the channel. In the process, the current gain becomes a function of the hole current, and the recombination mechanism becomes the dominant process needed to establish the hole current, as the gain begins to decrease.

In this self-adjusting coupled process, for a given voltage, only that fraction of electron can be injected into the drain region, which can generate the amount of holes needed to establish the flow of holes. However, more critical to understanding the mechanism is modeling the current-controlled behavior, where the product $\beta(M-1)$ approaches a value of 1 (15). Hence, I_h reaches a point wherein no more extra voltage is needed to drive holes across the ballast region; in the process, it triggers snapback (13)–(14a), shown at the bottom of the page. Now, when the current across path1 is dominant and under injection reaches a minimum value of $\beta_0/2$

$$\beta_{\min} = \frac{\beta_0}{1 + \frac{I_{SE1}\left(e^{\gamma_{1h} R_{sub} I_h}\right)}{I_{Bsat1}(e^{\gamma_{1e}{}^{\gamma} R_{sub} I_h})}} \approx \frac{\beta_0}{2}. \tag{14b}$$

Therefore, the equation can be reduced to classical interpretation of snapback [25]

$$\beta \bullet (M-1) \rightarrow 1. \tag{15}$$

$$I_B = \overbrace{I_{Bsat1}(e^{\gamma_1 R_{sub} I_h}-1) - \beta_0 \bullet (M-1) \bullet I_{Bsat1} \bullet (e^{\gamma_1 R_{sub} I_h}-1) + I_{SE1}(e^{\gamma_1 R_{sub} I_h}-1)}^{Path1}$$
$$+ \overbrace{I_{Bsat2}(e^{\gamma_2 R_{sub} I_h}-1) - \beta_0 \bullet (M-1) \bullet I_{Bsat2} \bullet (e^{\gamma_2 R_{sub} I_h}-1) + I_{SE2}(e^{\gamma_2 R_{sub} I_h}-1)}^{Path2} \tag{10}$$

$$\frac{dI_B}{dI_h} \approx 0 \;\&\; \frac{dM}{dI_h} \approx 0$$

$$\frac{dI_B}{dI_h} = \overbrace{\gamma_1 R_{sub} \bullet I_{Bsat1}(e^{\gamma_1 R_{sub} I_h}) - \beta_0 \bullet (M-1) \bullet I_{Bsat1} \bullet \gamma_1 R_{sub} \bullet (e^{\gamma_1 R_{sub} I_h}) + \gamma_1 R_{sub} I_{SE1}(e^{\gamma_1 R_{sub} I_h})}^{Path1}$$
$$+ \overbrace{\gamma_2 R_{sub} \bullet I_{Bsat2}(e^{\gamma_2 R_{sub} I_h}) - \beta_0 \bullet (M-1) \bullet I_{Bsat2} \bullet \gamma_2 R_{sub} \bullet (e^{\gamma_2 R_{sub} I_h}) + \gamma_2 R_{sub} I_{SE2}(e^{\gamma_2 R_{sub} I_h})}^{Path2} \tag{11}$$

$$0 = \overbrace{\gamma_{1e} \bullet R_{sub} \bullet I_{Bsat1}(e^{\gamma_{1e} R_{sub} I_h}) - \beta_0 \bullet (M-1) \bullet I_{Bsat1} \bullet \gamma_{1e} R_{sub} \bullet (e^{\gamma_{1e} R_{sub} I_h}) + \gamma_{1h} R_{sub} I_{SE1}(e^{\gamma_{1h} R_{sub} I_h})}^{Path1}$$
$$+ \overbrace{\gamma_{2e} \bullet R_{sub} \bullet I_{Bsat1}(e^{\gamma_{2e} R_{sub} I_h}) - \beta_0 \bullet (M-1) \bullet I_{Bsat2} \bullet \gamma_{2h} R_{sub} \bullet (e^{\gamma_{2h} R_{sub} I_h}) + \gamma_{2h} \bullet R_{sub} \bullet I_{SE2}(e^{\gamma_{2h} R_{sub} I_h})}^{Path2} \tag{12a}$$

$$\gamma_{1e} \bullet R_{sub} \bullet I_{Bsat1}(e^{\gamma_{1e} R_{sub} I_h}) + \gamma_{1h} \bullet R_{sub} \bullet I_{SE1}(e^{\gamma_{1h} R_{sub} I_h}) + \gamma_1 \bullet R_{sub} \bullet I_{Bsat2}(e^{\gamma_{2e} R_{sub} I_h}) + \gamma_{2h} R_{sub} I_{SE2}(e^{\gamma_{2h} R_{sub} I_h})$$
$$= \beta_0 \bullet (M-1) \bullet I_{Bsat1} \bullet \gamma_{1e} \bullet R \bullet e^{\gamma_{1e} R_{sub} I_h} + \beta_0 \bullet (M-1) \bullet I_{Bsat2} \bullet \gamma_{2e} \bullet R \bullet e^{\gamma_{2e} R_{sub} I_h} \tag{12b}$$

$$\beta_0 \bullet (M-1) = \frac{\gamma_{1e} \bullet R_{sub} \bullet I_{Bsat1}(e^{\gamma_{1e} R_{sub} I_h}) + \gamma_1 \bullet R_{sub} \bullet I_{SE1}(e^{\gamma_{1h} R_{sub} I_h}) + \gamma_{2e} \bullet R_{sub} \bullet I_{Bsat1}(e^{\gamma_{2e} R_{sub} I_h}) + \gamma_{2h} \bullet R_{sub} \bullet I_{SE1}(e^{\gamma_{2h} R_{sub} I_h})}{I_{Bsat1} \bullet \gamma_{1e} \bullet R \bullet e^{\gamma_{1e} R_{sub} I_h} + \bullet I_{Bsat2} \bullet \gamma_{2e} \bullet R \bullet e^{\gamma_{2e} R_{sub} I_h}} \tag{13}$$

$$\left[\overbrace{\frac{\beta_0}{\frac{\gamma_{1e} \bullet R_{sub} \bullet I_{Bsat1}\left(e^{\gamma_{1e} R_{sub} I_h}\right) + \gamma_{1h} \bullet R_{sub} \bullet I_{SE1}(e^{\gamma_{1h} R_{sub} I_h}) + \gamma_{2e} \bullet R_{sub} \bullet I_{Bsat2}\left(e^{\gamma_{2e} R_{sub} I_h}\right) + \gamma_{2h} \bullet R_{sub} \bullet I_{SE2}(e^{\gamma_{2h} R_{sub} I_h})}{I_{Bsat1} \bullet \gamma_{1e} \bullet R \bullet e^{\gamma_{1e} R_{sub} I_h} + \bullet I_{Bsat2} \bullet \gamma_{2e} \bullet R \bullet e^{\gamma_{2e} R_{sub} I_h}}}^{\beta} \right] \bullet (M-1) = 1 \tag{14a}$$

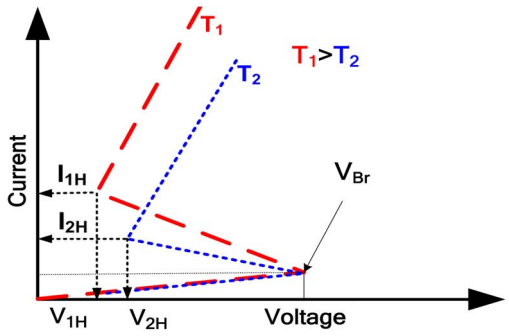

Fig. 13. Holding voltage and breakdown voltage of the device as it changes due to temperature dependence.

3) Determination of Holding Voltage V_h Relationship With β: The temperature-dependent holding voltage of the 2-D bipolars determines the state of conduction of individual 2-D bipolars in an array across the 3-D. Thus, during this critical localization phase (filamentation) after the bipolar turns on in 2-D, we can model the conduction mechanisms in the 3-D array from the temperature-dependent I–V curve (Fig. 13). Moreover, it is useful to model the holding voltage by relating it with the bipolar gain. The potential across the device can be estimated by adding the drop across the structure, and the holding voltage across the device can be derived by obtaining minimal solution for the given hole density J_h.

Solving for

$$\frac{dV}{dJ_h} = 0 \tag{16}$$

$$\frac{dV}{dJ_h} = -V_{\mathrm{Br}}\alpha^*\beta + \frac{1}{2}K\sqrt{\beta}J_h^{-\frac{1}{2}} = 0 \tag{17}$$

$$J_h = \left[\frac{K}{2V_{\mathrm{Br}}\alpha^*\sqrt{\beta}}\right]^2 \tag{18}$$

we make an approximation by ignoring the first term in (5), i.e.,

$$V_h \approx V_{\mathrm{Br}}\left(1 - \left[\frac{K}{2V_{\mathrm{Br}}\alpha^*\sqrt{\beta}}\right]^2 \alpha^*\beta\right) + K\beta^{1/2}\frac{K}{2V_{\mathrm{Br}}\alpha^*\beta}$$

$$= V_{\mathrm{Br}}\left(1 - \frac{K^2}{4V_{\mathrm{Br}}^2\alpha^*}\right) + K\frac{K}{2V_{\mathrm{Br}}\alpha^*\beta^{1/2}}. \tag{19}$$

Thus, the holding voltage across the device can be obtained by series approximation of

$$V_h \approx \frac{1}{\sqrt[k]{\eta+\beta}}V_B \approx \frac{V_B}{\sqrt[k]{\beta}}. \tag{20}$$

Therefore, the holding voltage can be expressed as a function of gain β. This consistently leads to very well established classical understanding of the phenomenon due to bipolar turn-on during avalanche breakdown.

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REFERENCES

[1] A. Chatterjee, S. Pendharkar, Y. Y Lin, C. Duwury, and K. Banerjee, "An insight into the high current ESD behavior of drain extended NMOS (DENMOS) devices in nanometer scale CMOS technologies," in *Proc. IRPS*, 2007, pp. 608–609.

[2] A. Chatterjee, S. Pendharkar, Y.-Y. Lin, C. Duvvury, and K. Banerjee, "A microscopic understanding of DENMOS device failure mechanism under ESD conditions," in *IEDM Tech. Dig.*, 2007, pp. 181–184.

[3] R. M. Steinhoff, J. B. Huang, P. L. Hower, and J. S. Brodsky, "Current filament movement and silicon melting in an ESD-robust DENMOS transistor," in *Proc. ESD/EOS Symp.*, 2003, pp. 98–107.

[4] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, and V. R. Rao, "On the failure mechanism and current instabilities in RESURF type DeNMOS device under ESD conditions," in *Proc. IRPS*, 2010, pp. 841–845.

[5] M. Shrivastava, H. Gossner, M. S. Baghini, and V. R. Rao, "Part II: On the 3D filamentation and failure modeling of STI type DENMOS device under ESD conditions," *IEEE Trans. Electron Devices*, to be published.

[6] G. Boselli, V. Vassilev, and C. Duvvury, "Drain extended NMOS high current behavior and ESD protection strategy for HV applications in sub-100 nm CMOS technologies," in *Proc. IRPS*, 2007, pp. 342–347.

[7] M. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker, and W. Fichtner, "Analysis and compact modeling of lateral DMOS power devices under ESD stress conditions," in *Proc. EOS/ESD Symp.*, 1999, pp. 1–10.

[8] M. Denison, M. Blaho, P. Rodin, V. Dubec, D. Pogany, D. Silber, E. Gornik, and M. Stecher, "Moving current filaments in integrated DMOS transistors under short-duration current stress," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1331–1339, Aug. 2004.

[9] K. Esmark, "Device simulation of ESD protection elements," Ph.D. dissertation, ETH, Zurich, Switzerland, 2001.

[10] A. Chatterjee, C. Duvvury, and K. Banerjee, "New physical insight and modeling of second breakdown phenomenon It_2 in advanced ESD protection devices," in *IEDM Tech. Dig.*, 2005, pp. 195–198.

[11] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd ed. Hoboken, NJ: Wiley, 2002.

[12] P. Hower and K. Reddi, "Avalanche injection and second breakdown in transistors," *IEEE Trans. Electron Devices*, vol. ED-17, no. 4, pp. 320–335, Apr. 1970.

[13] K. H. Oh, C. Duvvury, K. Banerjee, and R. W. Dutton, "Analysis of gate bias induced heating effects in deep submicron ESD protection designs," *IEEE Trans. Device Mater. Rel.*, vol. 2, no. 2, pp. 36–42, Jun. 2002.

[14] Y. S. Chung and B. Baird, "Electrical-thermal coupling mechanism on operating limit of LDMOS transistor," in *IEDM Tech. Dig.*, 2000, pp. 83–86.

[15] P. Hower, C.-Y. Tsai, S. Merchant, T. Efland, S. Pendharkar, R. Steinhoff, and J. Brodsky, "Avalanche-induced thermal instability in LDMOS transistors," in *Proc. ISPSD*, 2001, pp. 153–156.

[16] V. Khemka, V. Parthasarthy, R. Zhu, A. Bose, and T. Roggenbauer, "Experimental and theoretical analysis of energy capability of RESURF LDMOSFETs and its correlation with static electrical Safe Operating Area (SOA)," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1049–1058, Jun. 2002.

[17] V. M. Dwyer, A. J. Franklin, and D. S. Campbell, "Thermal failure in semiconductor devices," *Solid State Electron.*, vol. 33, no. 5, pp. 553–560, May 1990.

[18] D. C. Wunsch and R. R. Bell, "Determination of threshold failure levels of semiconductor diodes and transistors due to pulse voltages," *IEEE Trans. Nucl. Sci.*, vol. NS-15, no. 6, pp. 244–259, Dec. 1968.

[19] D. Pogany, S. Bychikhin, C. Furbock, and M. Litzenberger, "Quantitative internal thermal energy mapping of semiconductor devices under short current stress," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 2070–2079, Nov. 2002.

[20] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, A. Bose, and R. Ida, "A double RESURF LDMOS with drain profile engineering for improved ESD robustness," *IEEE Electron Device Lett.*, vol. 23, no. 4, pp. 212–214, Apr. 2002.

[21] K.-H. Oh, C. Duvvury, K. Banerjee, and R. W. Dutton, "Analysis of nonuniform ESD current distribution in deep submicron NMOS transistors," *IEEE Trans. Electron Devices*, vol. 49, no. 12, pp. 2171–2182, Dec. 2002.
[22] P. L. Hower and S. Merchant, "Snapback and safe operating area of LDMOS transistors," in *IEDM Tech. Dig.*, 1999, pp. 193–196.
[23] S. L. Miller, "Avalanche breakdown in germanium," *Phys. Rev.*, vol. 99, no. 4, pp. 1234–1241, Aug. 1955.
[24] J. D. Hayden, D. Burnett, and J. Nangle, "A comparison of base current reversal and bipolar snapback inadvanced npn bipolar transistors," *IEEE Electron Device Lett.*, vol. 12, no. 8, pp. 407–409, Aug. 1991.
[25] R. Dutton, "Bipolar transistor modeling of avalanche generation for computer circuit simulation," *IEEE Trans. Electron Devices*, vol. ED-22, no. 6, pp. 334–338, Jun. 1975.

Amitabh Chatterjee, photograph and biography not available at the time of publication.

Mayank Shrivastava (S'09–M'10), photograph and biography not available at the time of publication.

Harald Gossner, (M'06) photograph and biography not available at the time of publication.

Sameer Pendharkar, (SM'06) photograph and biography not available at the time of publication.

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