A Solution Toward the OFF-State Degradation in Drain-Extended MOS Device

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***Abstract*—We investigated the surface band-to-band tunnelling (BTBT) current under the OFF-state condition in drain-extended MOS (DeMOS) devices. We found significant gate-induced drain leakage current due to surface BTBT, which was also reported earlier as the dominant cause of early time-dependent dielectric breakdown and device failure. Furthermore, a layout solution for the existing DeMOS device is proposed in order to mitigate the surface BTBT current and the associated gate oxide reliability issues, without sacrificing the mixed-signal performance of the device.**

***Index Terms*—Band-to-band tunnelling (BTBT), drain extended, drain-extended MOS (DeMOS), input/output, time-dependent dielectric breakdown (TDDB).**

I. Introduction

As THE TECHNOLOGY is shrinking below 45-nm node, the core circuits are now operating at voltages below 1 V, whereas the input/output circuits are still operating at higher voltages, leading to severe gate oxide reliability issues. This can either be due to hot-carrier degradation or electrostatic discharge events. There are several high-voltage structures proposed for advanced CMOS technology, and among them, drain-extended MOS (DeMOS) device is one of the possible options due to its easy integration in the advanced CMOS process and its process compatibility. There are two possible DeMOS structures suitable for advanced CMOS technologies: 1) shallow trench isolation (STI) type, i.e., with an STI underneath a gate-to-drain overlap, and 2) non-STI type, i.e., without any STI underneath a gate-to-drain overlap (as shown in Fig. 1). Although the STI-type DeMOS has shown excellent gate oxide reliability, it is known for its degraded mixed-signal performance [1], [2]. The non-STI device shows excellent mixed-signal performance but suffers from significant gate oxide reliability concerns in the OFF state [3]. As reported earlier [3], [4], significant surface band-to-band tunnelling (BTBT) current leads to excess hot-hole generation in the OFF state and causes the early time-dependent dielectric breakdown (TDDB) failure of the non-STI device. In this brief, we have proposed a modification in the device's layout, which mitigates the surface BTBT current and eventually helps in improving the associated gate oxide reliability behavior significantly without sacrificing its mixed-signal performance.

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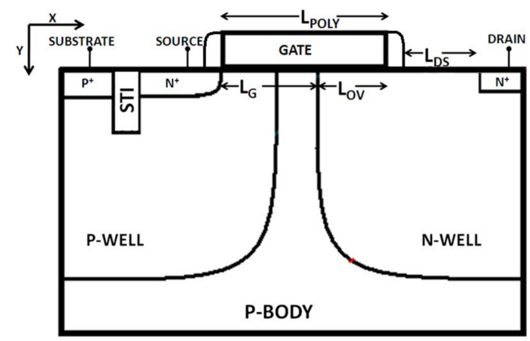

Fig. 1. Non-STI-type DeMOS device. Standard device, which is prone to TDDB failure in the OFF state, has $L_{\rm DS} = 0$ nm.

This brief is arranged as follows. Section II describes the experimental and simulation setup. The proposed modification and results are discussed in Section III, and Section IV summarizes the important contributions of this study.

II. Simulation and Experimental Setup

A thin-gate-oxide non-STI-type DeMOS device was fabricated using standard 65-nm CMOS process and characterized. For simulation studies, the device was realized using a well-calibrated process simulation deck. The device simulation setup with well-calibrated mobility models for hydrodynamic transport was used.

In order to accurately capture the surface BTBT current and carrier energy (or temperature), Hurkx BTBT model [5] was calibrated with the reference non-STI-type DeMOS device, and carrier (i.e., both electron and hole) temperatures were solved in the hydrodynamic simulations. Fig. 2(a) shows the calibration of our simulation setup with experiments. This simulation setup is used further in order to study the performance of the modified device.

III. Results and Discussions

Fig. 2 shows the experimental and simulated I_D–V_G characteristics of the non-STI DeMOS device (with $L_G = 450$ nm). The inset in Fig. 2 shows the hole temperature (T_h) profile

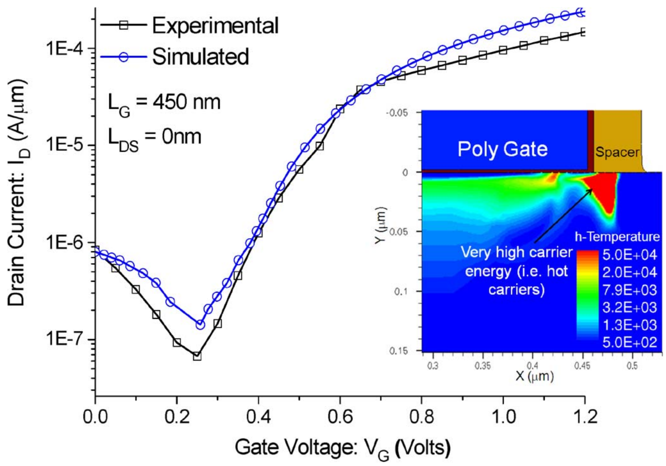

Fig. 2. Experimental and simulated I_D–V_G characteristics (@ $V_D = 5$ V) of standard DeMOS device (i.e., $L_{\mathrm{DS}} = 0$ nm). Inset shows the hole temperature (in kelvins) contour extracted from hydrodynamic simulations in the OFF state (i.e., $V_D = 5$ V and $V_G = 0$ V).

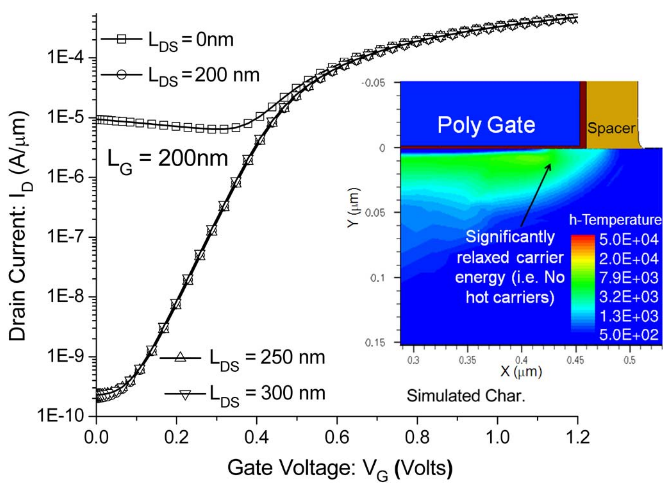

Fig. 3. Simulated I_D–V_G characteristics (@ $V_D = 5$ V) of the modified DeMOS device (i.e., $L_{\mathrm{DS}} \geq 200$ nm). Inset shows significantly relaxed hole temperature (in kelvins) in the OFF state (i.e., no hot holes) for the device with $L_{\mathrm{DS}} \geq 200$ nm.

extracted from hydrodynamic simulations, where the hole energy (E_h) is given by the relation

$$E_h = 3kT_h/2 \tag{1}$$

where k is the Boltzmann constant and T_h is the hole temperature. A significant BTBT current in the OFF state is evident from Fig. 2. The surface BTBT current causes hot-hole generation in the OFF state, which causes severe gate oxide reliability issues [3] and eventually leads to early TDDB and permanent failure of the DeMOS device.

Fig. 3 shows that, by increasing the L_{DS} (Fig. 1) from 0 (standard device layout) to 200 nm or more (proposed device layout), one can mitigate the surface BTBT. This behavior is attributed to the increased tunnelling width (valance band to conduction band, w.r.t. electrons) by shifting the N^+ drain diffusion away from the gate edge. This helps in reducqing the excess leakage current in the OFF state by orders of magnitude and eventually helps in improving the gate oxide reliability. This is evident from the inset in Fig. 3, as the hole temperature (i.e., energy) is relaxed significantly. Recently, we have reported

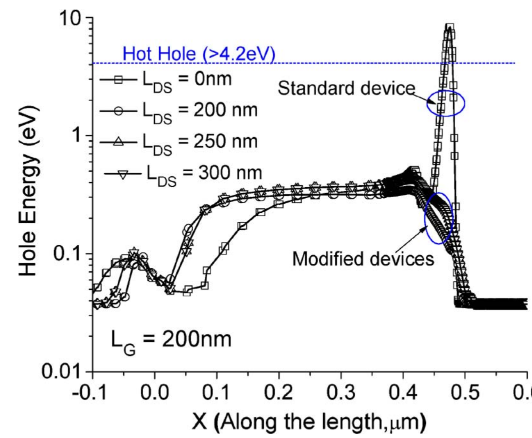

Fig. 4. Simulated (hydrodynamic simulations) hole energy profile along the length of the device, extracted 1 nm below the Si surface, in the OFF state (i.e., $V_D = 5$ V and $V_G = 0$ V).

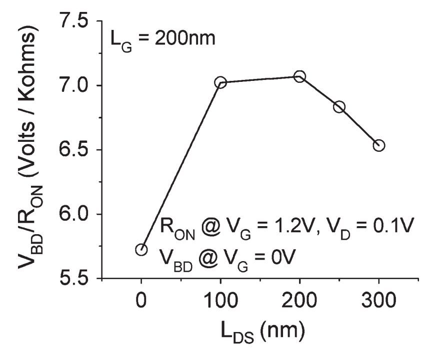

Fig. 5. Simulated $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ tradeoff characteristics. It shows an optimum point at $L_{\mathrm{DS}} = 200$ nm and 25% improvement in $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ tradeoff. V_{BD} was extracted at $V_G = 0$ and an I_D compliance of 1 μA/μm.

few other ways of reducing BTBT current [1], [2]. However, they lead to degraded R_{ON} or require an extra masking step.

Furthermore, Fig. 4 compares the hole energy profile (1 nm under the surface) for devices with different L_{DS}. It shows that increasing the L_{DS} to 200 nm or more relaxes the carrier (hole for DeNMOS) energy significantly. The proposed modification will greatly help in improving the device reliability. In order to incorporate the proposed modification, a silicide blocking mask is required, in order to block the silicidation in the drain extension region (between gate edge and N^+ drain diffusion), and the proposed modification does not need any other masking or process step. Since the silicide blocking mask already exists in the standard sub-100-nm-node CMOS process, the proposed modification does not require any extra mask or process step.

Furthermore, Fig. 5 shows a 25% improvement in the $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ tradeoff. It is also evident from the figure that devices give an optimum value of $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ tradeoff at $L_{\mathrm{DS}} = 200$ nm. For further discussions and comparison of the standard device with the modified device in this brief, we use $L_{\mathrm{DS}} = 200$ nm. Fig. 6 shows the change in the device's intrinsic performance (i.e., V_T, I_{OFF}, V_{BD}, and R_{ON}) by incorporating the proposed modification. For $L_{\mathrm{DS}} = 200$ nm, it shows that, while I_{OFF} was improved by five orders of magnitude (as discussed earlier), R_{ON} degrades by less than 20%, which is due to a slight increase in the resistance of extended drain region. Furthermore, it also shows a negligible change in threshold

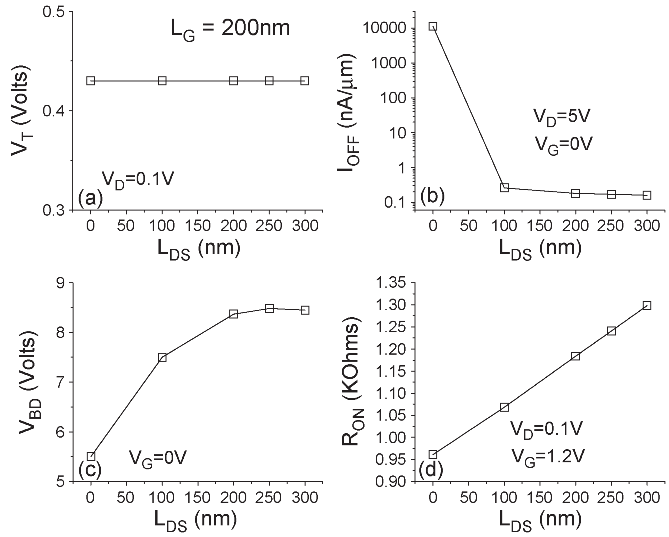

Fig. 6. Simulated intrinsic characteristics (i.e., V_T, I_{OFF}, V_{BD}, and R_{ON}) of the DeMOS device w.r.t. L_{DS}.

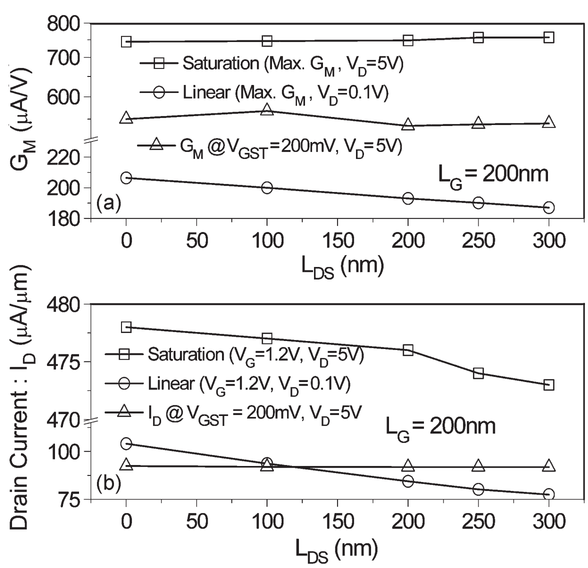

Fig. 7. Simulated impact of gate-to-drain spacing (L_{DS}) over drain current and transconductance (G_M) under various bias/circuit conditions.

voltage in the linear operating condition of the device and 60% improvement in the breakdown voltage. Improvement in breakdown voltage is explained as follows: Initially, for $L_{\mathrm{DS}} = 0$ nm, the device's breakdown was limited due to dominance of surface BTBT, which triggers at lower drain voltages (5.5 V). Whereas, by mitigating the surface BTBT effect, the device's breakdown dominantly depends on impact ionization at Nwell-to-Pwell junction, which occurs at a higher drain voltage. Eventually, this leads to improved V_{BD} values.

Fig. 7 shows the impact of increasing L_{DS} over drain current (I_D) and transconductance (G_M) of the device under various bias/circuit conditions. It is evident from Fig. 7 that, for $L_{\mathrm{DS}} = 200$ nm, there is a negligible degradation in I_D and G_M for the following: 1) $V_{\mathrm{GST}} = 200$ mV and $V_D = 5$ V and 2) under the device's operation in the saturation region (i.e., $V_D = 5$ V). On the other hand, I_D and G_M degrade by less than 20% and 6%, respectively, for devices' operating in the linear region (i.e., $V_D = 0.1$ V), due to a slight increase in the resistance of the drift region. It is worth mentioning that the observed degradation in the linear operating condition (under which R_{ON} versus V_{BD} is the dominant figure of merit) is in the acceptable range, considering 25% improvement in $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ tradeoff.

IV. Conclusion

The standard non-STI-type DeMOS device suffers from the surface BTBT current, which causes early TDDB failure. Increasing L_{DS} length is the key to improve the surface BTBT current in the device without sacrificing the analog performance of the device for a given value of $V_{\mathrm{DB}}/R_{\mathrm{ON}}$ tradeoff. The proposed modification also helps in improving $V_{\mathrm{DB}}/R_{\mathrm{ON}}$ tradeoff associated with drain-extended devices for high-voltage applications. Furthermore, it does not lead to any degradation in the digital performance of the device. The proposed modification in the layout does not need any extra mask or process step.

References

[1] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "I/O device optimization and performance comparison: Part I—Mixed signal performance of various high voltage drain extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[2] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "I/O device optimization and performance comparison: Part II—A novel scheme to optimize the mixed signal performance and hot carrier reliability of drain extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 458–465, Feb. 2010.

[3] D. Varghese, H. Kufluoglu, V. Reddy, H. Shichijo, S. Krishnan, and M. A. Alam, "Universality of off-state degradation in drain extended NMOS transistors," in *IEDM Tech. Dig.*, 2006, pp. 751–754.

[4] D. Varghese, H. Kufluoglu, V. Reddy, H. Shichijo, D. Mosher, S. Krishnan, and M. A. Alam, "OFF-State degradation in drain-extended NMOS transistors: Interface damage and correlation to dielectric breakdown," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2669–2678, Oct. 2007.

[5] G. Hurkx, D. Klaassen, and M. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Devices*, vol. 39, no. 2, pp. 331–338, Feb. 1992.

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