Microelectronics Journal 42 (2011) 758–765

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A novel architecture for improving slew rate in FinFET-based op-amps and OTAs

Rajesh A. Thakker [a,*], Mayank Srivastava [b], Ketankumar H. Tailor [a], Maryam Shojaei Baghini [a], Dinesh K. Sharma [a], V. Ramgopal Rao [a], Mahesh B. Patil [a]

[a] Department of Electrical Engineering, Indian Institute of Technology (IIT), Bombay, India
[b] Senior Engineer, 28nm/20nm ESD Development, Intel Mobile Communications, USA

ARTICLE INFO

Article history:
Received 23 September 2010
Received in revised form
12 January 2011
Accepted 17 January 2011
Available online 17 February 2011

Keywords:
High slew rate op-amp
Look-up table
FinFET
Hierarchical particle swarm optimization
Circuit design

ABSTRACT

A new architecture for improvement of slew rate (SR) of an op-amp or an operational transconductance amplifier (OTA) in FinFET technology is proposed. The principle of operation of the proposed architecture is based on a set of additional current sources which are switched on, only when OTA should provide a high current, usually for charge or discharge of large load capacitor. Therefore, the power overhead is less compared to conventional high SR designs. The commonly used two-stage Miller-compensated op-amp, designed and optimized in sub 45 nm FinFET technology with 1 V single supply voltage, is used as an example for demonstration of the proposed method. For the same FinFET technology and with optimal design, it is shown that the slew rate of the op-amp is significantly improved. The slew rate is improved from 273 to 5590 V/μs for an input signal with a rise time of 100 ps. The other performance measures such as gain and phase margin remain unchanged with the additional circuitry used for slew rate enhancement.

1. Introduction

In applications like switched-capacitor filters or switched op-amps, fast switching of output voltage from an initial value to a final value is desired. Therefore, settling time of the output should not be limited by the slew rate of the op-amp. This motivates developing special circuit structures which improve op-amp slew rates.

Table 1 shows comparison of important performance parameters of few of the reported slew rate-enhanced circuits in different CMOS technologies. A CMOS op-amp, implemented in 6 μm CMOS technology with internal transistor compensation, and slew rate of +36/−50 V/μs with power dissipation of 11.5 mW has been reported in early 80s [1]. In [2], a class AB op-amp using common mode feedback, implemented in 2 μm technology, has been demonstrated. This op-amp exhibits 2.5 V/μs slew rate at 10 pF load capacitance while dissipating 0.1 mW power. In [3], an input differentiator is used to turn on an additional bias current source at the input stage whenever the rate of change of input voltage is larger than preset value. The circuit proposed in [3] was implemented in 0.8 μm CMOS technology and could achieve a positive slew rate of 2667 V/μs at a load capacitance of 15 pF at the cost of 14 mW power dissipation. Its slew rate degrades as output capacitance charges (discharges) or as supply voltage reduces. In [4], an OTA cell with high slew rate was implemented in 0.5 μm CMOS technology. It used a class AB input stage to control the slew rate. However, the amount of slew rate enhancement depends on the value of input differential voltage. It could achieve a maximum slew rate of 100 V/μs at 80 pF load with 0.12 mW power dissipation. The class A/AB and AB/AB two-stage op-amps was fabricated in 0.5 μm CMOS technology which achieved a symmetrical slew rate of 16 V/μs [5]. A fast-transient switching DC–DC converter using a ΔΣ modulator, designed in 0.35 μm CMOS technology, could achieve 0.56 V/μs slew rate at 10 nF load capacitance with a power dissipation of 200 mW [6]. In [7], a low power class-AB CMOS OTA with rising and falling slew rates of 4.92 and 5.04 V/μs, respectively, at 10 pF load capacitance was designed and implemented in 0.18 μm CMOS technology. In [8], a fast settling slew rate enhancement technique for an op-amp using constant-g_m biasing was designed in 0.18 μm process. It used an auxiliary op-amp which slews at the same time as the main op-amp slews. It increased slew rate from 25 to 150 V/μs with a total static power dissipation of 5.8 mW. A SR controlled output driver which uses a phase-locked loop was reported in [9] and implemented in 0.18 μm CMOS technology. It could achieve a slew rate of 0.4–1 V/ns for a load capacitance of 15–40 pF. In [10], a two-stage op-amp with both gain and slew rate enhancement was simulated in 0.18 μm CMOS technology. It could achieve 26.8 V/μs slew rate and 74 dB DC gain with 362 μW power consumption. A 1 V digital OTA for

* Corresponding author. Tel.: +91 9426333130.
E-mail address: rathakker2008@gmail.com (R.A. Thakker).

0026-2692/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2011.01.010

Table 1
Comparison of reported work of slew rate enhanced circuits with that demonstrated in this paper. Here, A_v=voltage gain, SR=slew rate, C_L=load capacitance, PD=power dissipation, t_s=settling time, UGB = unity gain bandwidth, PM=phase margin, E/S = experimental/simulation.

Technology	A_v	SR, C_L	PD	t_s	UGB	PM	E/S
6 μm [1]	≥60 dB	+36/−50 V/μs, 32 pF	11.5 mW	0.25 μs	8 MHz	50°	E
2 μm [2]	70 dB	2.5 V/μs, 10 pF	0.1 mW	–	–	–	E
0.8 μm [3]	100.7 dB	≥2 V/ns, 15 pF	14.1 mW	+15 ns/−19 ns	55 MHz	–	S
0.5 μm [4]	43 dB	+36/−50 V/μs, 80 pF	120 μW	+29 ns/−57 ns	725 kHz	89.5°	E
0.5 μm [5]	–	16 V/μs, 10 pF	–	–	15 MHz	–	E
0.35 μm[6]	–	0.56 V/μs, 10 nF	200 mW	–	200 MHz	50°	S
0.18 μm [7]	48.97 dB	+4.92/−5.04 V/μs, 10 pF	1.96 μW	2.1 μs	57.27 kHz	78.18°	S
0.18 μm [8]	–	150 V/μs,-	5.76 mW	–	–	–	S
0.18 μm [9]	–	1 V/ns, 40 pF	–	–	–	–	E
0.18 μm [10]	74 dB	26.8 V/μs, 1.75 pF	362 μW	–	160 MHz	–	S
0.13 μm [11]	63.5 dB	16.29 V/μs, 34 pF	82 μW	734 ns	19.2 MHz	74.95°	S
90 nm [12]	17 dB	1354 V/μs, –	–	–	11.5 GHz	61.2°	E
45 nm, this work	83 dB	+1043/−176 V/μs, 1 pF	103 μW	+3.98/−19.2 ns	77.4 MHz	60°	S
	79.65 dB	+6171/−5590 V/μs, 20 fF	78 μW	+310/−600 ps	695 MHz	61°	S

switched capacitor applications with a slew rate of 16.29 V/μs and power dissipation of 82 μW was realized in 0.13 μm CMOS technology [11]. In [12], two-stage Miller and folded cascode op-amps were programmed digitally to enhance the gain, slew rate and compensation, and were implemented in standard 90 nm CMOS process. The performance parameters of folded cascode op-amp [12] with programmable characteristics are mentioned in Table 1.

There is some reported literature for slew rate improvement of BJT circuits. A high slew rate op-amp with class AB input stage was fabricated in 40 V complementary bipolar technology [14]. A symmetrical BJT voltage follower with high slew rate of 4950 V/μs was reported in [15].

There are also reported patents which focus on the class AB operation of input circuit to improve SR of the op-amp or OTA. Class AB operation reduces power overhead compared to the conventional high-bias current design. In [16], improvement in sinking of load current and ability to drive large capacitive loads were achieved by inserting source follower stage between folded cascoded gain stage and class AB stage. A phase inverter circuit was used to control the current source circuits to obtain a high slew rate over the voltage range of approximately 4 V [17]. A controllable assistant output stage was used in addition to the output stage in [18] to improve the slew rate. The output buffer and feedback circuitry-based slew rate control circuit, which also increases gate-oxide reliability of the IC is described in [19].

This paper presents a new power-efficient architecture for improvement of slew rate (SR) of an op-amp or an OTA. It is tested in 45 nm FinFET technology at a supply voltage of 1 V. Previously reported papers on slew rate improvement have been demonstrated in CMOS technologies older than 45 nm [1–19] and most of them are reported to operate at a supply voltage higher than 1 V. The circuit demonstrated in [11] works at 1 V but it offers very small slew rate of 16.29 V/μs. The digitally programmed folded cascode op-amp, implemented in 90 nm CMOS technology [12], resulted in maximum slew rate of 1354 V/μs for DC voltage gain of 17 dB. The proposed architecture in this paper enhances the slew rate by a set of additional current sources which are controlled by comparators. The comparators turn current sources on if absolute value of differential input voltage exceeds some threshold value during charge or discharge of circuit capacitor(s). It is also shown that the inclusion of comparators and current sources does not significantly affect other performance measures except power dissipation of OTA/op-amp. The power dissipation of op-amp/OTA also increases marginally compared to the relative increase in the slew rate. We also show that the proposed technique also works for fully differential FinFET OTAs with common mode feedback (CMFB) without effect on the stability of the OTA. The proposed architecture can be used for planar MOSFET as well. It is well known that multigate devices such as FinFETs have the advantage of very less short-channel effects compared to planar MOSFETs. Multigate devices are one category of promising devices in near future and therefore, in this paper, we have tested the proposed architecture using FinFET devices.

The paper is organized as follows. In Section 2, the basic principle of the proposed architecture is described. The circuit schematic and simulation results for the two-stage op-amp, with and without slew rate enhancement circuitry, are given in Section 3. The simulation results for the differential amplifier with CMFB circuit in combination with the slew rate enhancement are presented in Section 4. Finally, conclusions are summarized in Section 5.

2. Basic principle

The slew rate of an OTA or op-amp is proportional to the maximum current, usually available from the first stage of the circuit. Increase in the slew rate requires increase in the value of bias current source, which will increase the overall power dissipation of the circuit. Besides other performance measures of the op-amp will get affected. The objective of the basic idea, presented in this paper, is to achieve a high slew rate, with a low power overhead while maintaining other performance measures of op-amp (or OTA) unchanged. The principle of operation is detecting the onset of slewing operation of the circuit and accordingly activating the additional current sources in the appropriate directions. The additional current sources are activated only during the slewing operation of the op-amp circuit, and hence power dissipation and other performance measures of the basic op-amp circuit mostly remain unchanged.

The block diagram of the novel SR improvement circuit is shown in Fig. 1. There are mainly two sections in the proposed architecture, which are used for slew rate improvement. These sections constitute unsymmetrical comparators as detection circuits and additional switchable current sources as current boosting modules. As shown in the figure, additional current sources, I_1 to I_4, are controlled by comparators: COMP1 and COMP2. These comparators are sized in such a way to keep the output of the control logic circuit at a proper logic level when the absolute value of the differential input voltage is less than some threshold

value (denoted by V_{sw}). I_1 and I_3 are controlled by COMP1 while I_2 and I_4 are controlled by COMP2. I_1 and I_3 current sources are approximately equal in terms of value, and similarly, I_2 and I_4 current sources. During positive slewing operation, i.e., when V_{in1} is greater than V_{in2} by some marginal value, comparator COMP1 operates, and in negative slewing operation, i.e., when V_{in1} is less than V_{in2} by some marginal value, comparator COMP2 operates. The output of COMP1, $\overline{C}_1$, goes low when the difference between V_{in1} and V_{in2} exceeds certain voltage (i.e., switching voltage, V_{sw}) and hence current sources I_1 and I_3 are activated. The activation of I_1 and I_3 current sources, injects additional current into the compensation capacitor C_c. The activation of two current sources together completes the path from supply to V_{ss} for charging C_c and therefore, speeds up positive slewing operation. The value of V_{sw} is a design variable, which in fact determines the switching point of the detector circuit. Similarly, during negative slewing operation, the output of COMP2 becomes high, which activates I_2 and I_4 current sources and accordingly negative slew rate improves.

3. Circuit schematic and simulation results

3.1. FinFET technology

The principle explained in Section 2 and shown in Fig. 1, is implemented in 45 nm technology FinFET devices. The TCAD simulator [20] mobility parameters are first tuned to match with FinFET device experimental data (Fig. 2) [21,22]. The FinFET technology parameters used in this work are: minimum channel length (L) is 20 nm, effective oxide thickness (EOT) is 1.6 nm, fin width (W_{FIN}) is 6 nm, and fin height (H_{FIN}) is 30 nm. The channel doping is $1\times10^{15}\,cm^{-3}$ and the source/drain doping is $1\times10^{20}\,cm^{-3}$ with

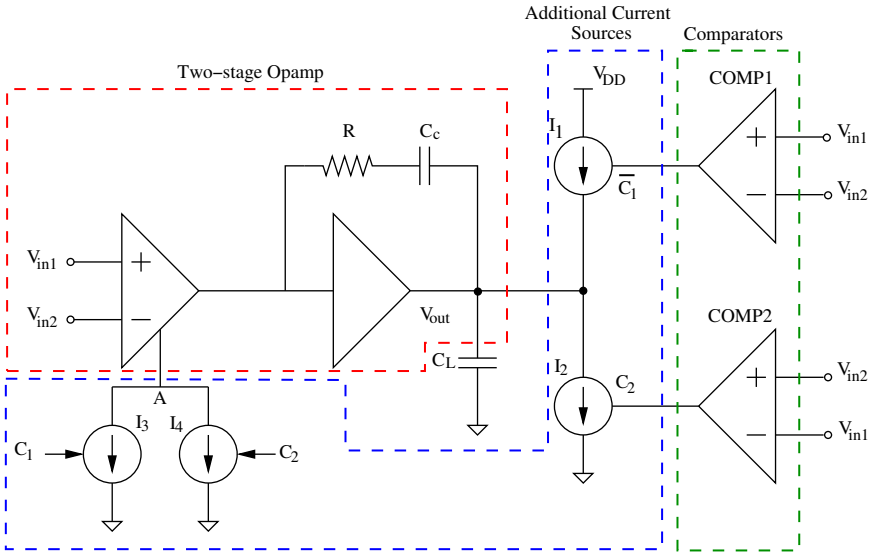

Fig. 1. Architecture of the SR improvement module employed in a two-stage op-amp circuit.

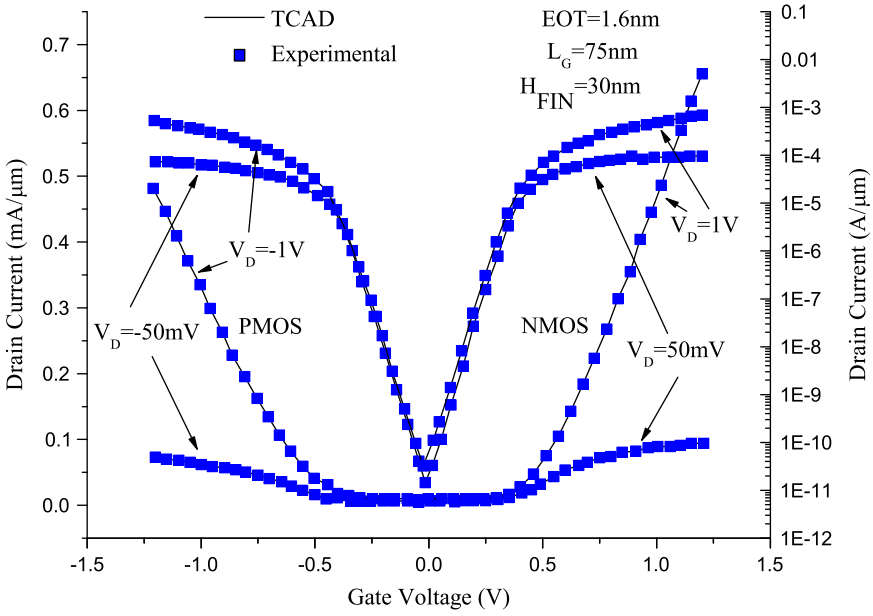

Fig. 2. Calibration of TCAD models for drift diffusion transport with experimental data [21,22].

an overlap distance (L_{OV}) of 2 nm and a 1 nm/decade Gaussian doping gradient into the channel.

3.2. Circuit schematic and design

The circuit schematic, used to verify the proposed principle, is shown in Fig. 3. As an example, the commonly used two-stage op-amp, shown in Fig. 3(a), is designed and optimized for maximizing slew rate under a given power constraint ($<50\ \mu W$). The power dissipation constraint considered in the design is less than some of the earlier reported work [1–4,6,10] on slew rate improvement. The circuit schematics for comparators (COMP1 and COMP2) along with the switchable current sources are given in Fig. 3(b) and (c). Look-up table (LUT) approach [23] implemented in the SEQUEL circuit simulation package [24] is used for simulation of the circuits in this

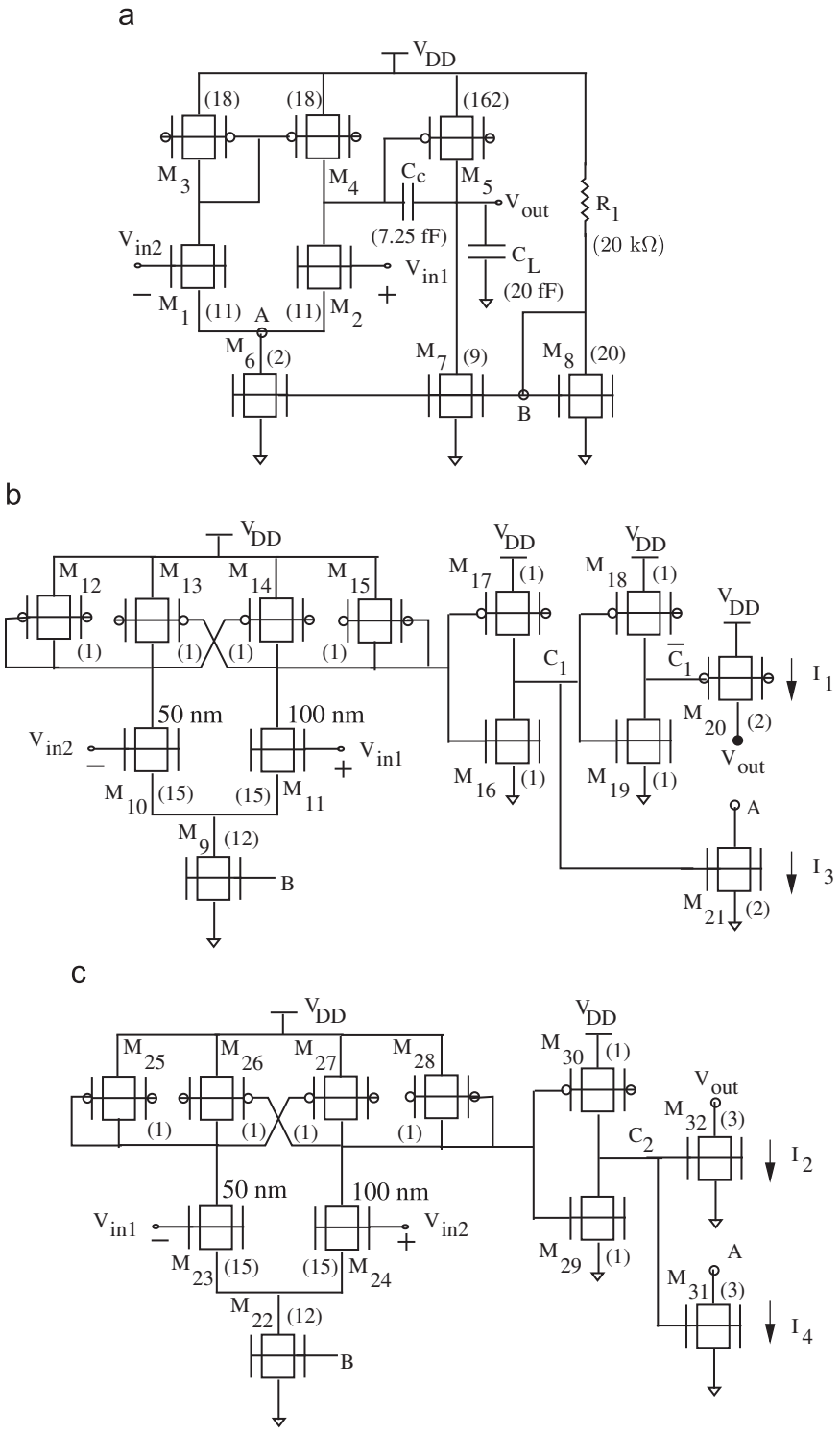

Fig. 3. The circuit schematic for slew rate improvement using FinFETs: (a) two-stage op-amp circuit, (b) unsymmetrical comparator COMP1 and I_1 and I_3 current sources and (c) unsymmetrical comparator COMP2 and I_2 and I_4 current sources. Numbers in brackets show number of fins for FinFET devices, and values for resistors and capacitors. Length of input transistors of two comparators is given in (b) and (c). Channel length of other transistors is 50 nm.

work. A hierarchical particle-swarm-optimization algorithm is used for optimization of FinFET circuits for desired specifications as described in detail in [23].

Op-amp circuit is designed using FinFET devices of channel length 50 nm. To obtain the required value of switching (sensing) voltage (V_{sw}), it is desirable to use asymmetric comparators, for example, by using asymmetric input devices. Asymmetry in the comparator may be implemented in different ways, e.g., by introducing mismatch between lengths or number of fingers of two corresponding input transistors. In this work, FinFET devices with different channel lengths are used in the input stage to achieve the required asymmetry. This means input transistors M_{10} and M_{11} have different channel lengths in COMP1 and similarly, transistors M_{23} and M_{24} in COMP2 are of different channel lengths. We have chosen 50 nm channel length for M_{10} and remaining transistors in COMP1 except M_{11} transistor. FinFET device with 100 nm channel length is chosen for M_{11} transistor. Similarly, in COMP2, 50 nm channel length for M_{23} and remaining transistors in COMP2 except M_{24}. The channel length of transistors M_{24} and M_{11} is 100 nm. Using this approach, COMP1 and COMP2 are made unsymmetrical. Look-up tables are generated using TCAD simulator for 50 and 100 nm devices to provide look-up tables for simulation of circuits using LUT simulator.

The automatic design approach (LUT-based optimizer), proposed by the authors for the design and optimization of FinFET-based circuits, is used to efficiently design and optimize all circuits demonstrated in this work [25]. Initially, the op-amp circuit is automatically designed using LUT-based optimizer for specifications given in Table 2. The resulted design (number of fins for FinFETs and other component values) is given in Fig. 3(a) and achieved specifications are shown in Table 2. The slew rate values, shown in Table 2, are obtained by keeping op-amp in unity gain configuration and applying input pulse signal with a rise and fall time of 100 ps. This circuit is referred as "two-stage opamp-1."

By running multiple design and optimization trials for "two-stage opamp-1," it was verified that the obtained design specifications, given in Table 2, are the best possible values. Comparator circuit is designed for the switching voltage V_{sw}=55 mV, using automatic design approach. It should be noted that input transistors of comparators have different channel lengths. The design for unsymmetrical comparators, i.e., number of fins for FinFET devices, is given in Fig. 3(b) and (c). The number of fins for FinFET devices in current sources is chosen to obtain best settling time during slewing operation.

The simulation results of op-amp circuit in combination with slew rate enhancement circuitry, referred as SR-improved op-amp, are given in Table 2. It can be seen from the table that slew rate is improved from 271 to 5590 V/μS and power dissipation increases from 46 to 78 μW. The increase in power dissipation is marginal in comparison to the improvement observed in slew rates. Other specifications of op-amp are not affected. For obtaining DC power dissipation (no signal) both inputs, V_{in1} and V_{in2} are connected to $V_{DD}/2$. For obtaining average power dissipation, a square wave with frequency of 100 MHz, and rise and fall time of 100 ps has been applied to the input. Obtained values are: 46 μW without slew rate enhancement circuitry and 71.7 μW with slew rate enhancement circuitry.

To find out, the best possible slew rate which can be obtained with the conventional two-stage op-amp without using any additional circuitry for slew rate enhancement, the two-stage op-amp was designed without any constraint on power dissipation. It gave a slew rate of 650 V/μS with a power dissipation of 113 μW. This circuit is referred as "two-stage opamp-2". This power dissipation is higher than the proposed circuit which is a combination of slew rate enhancement circuitry and "two-stage opamp-1." The slew rate for "two-stage opamp-2" is also almost one-tenth of the proposed circuit.

The transient response for all three circuits, two-stage opamp-1, two-stage opamp-2, and the proposed circuit (SR-improved op-amp), is shown in Fig. 4 for an input signal with a rise time of 100 ps. It can be seen that the proposed circuit shows a very high slew rate in comparison to other two circuits.

The slew rates of two-stage opamp-1 and proposed circuit are measured for an input signal with rise and fall time varying in the range of 25 ps to 2 ns. The simulation results are shown in Fig. 5.

Table 2
Desired and obtained specifications of two-stage op-amp circuit of Fig. 3 without and with slew rate enhancement circuitry. Op-amp circuit without slew rate enhancement circuitry (i.e., Fig. 3(a)) is referred as "Two-stage Opamp-1". The circuit with slew rate enhancement is referred as "SR-improved op-amp". All circuits are automatically designed and optimized.

Specifications and desired values	Best obtained values (two-stage opamp-1)	SR-improved op-amp
Gain $\geq$ 80 dB	79.65 dB	79.65 dB
Phase margin $\geq 65^\circ$	61°	61°
Unity gain frequency $\geq$ 500 MHz	695 MHz	695 MHz
Power dissipation $\leq$ 50 μW	46 μW	78 μW
Offset voltage $\leq$ 50 μV	83 μV	83 μV
Slew rate rise $\geq$ 500 V/μS	273 V/μS	6171 V/μS
Slew rate fall $\geq$ 500 V/μS	271 V/μS	5590 V/μS

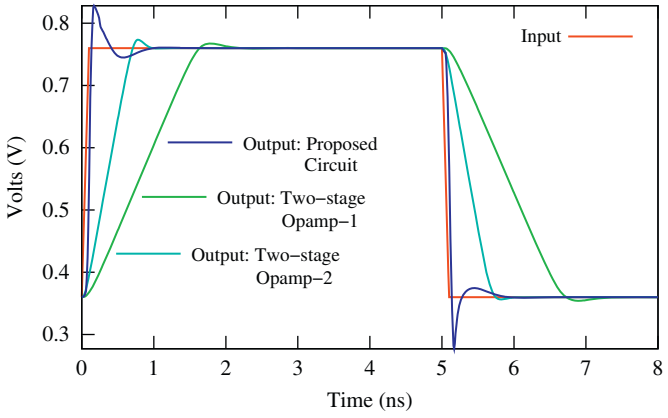

Fig. 4. The transient response of two-stage opamp-1, two-stage opamp-2, and the proposed circuit for an input signal with a rise time of 100 ps.

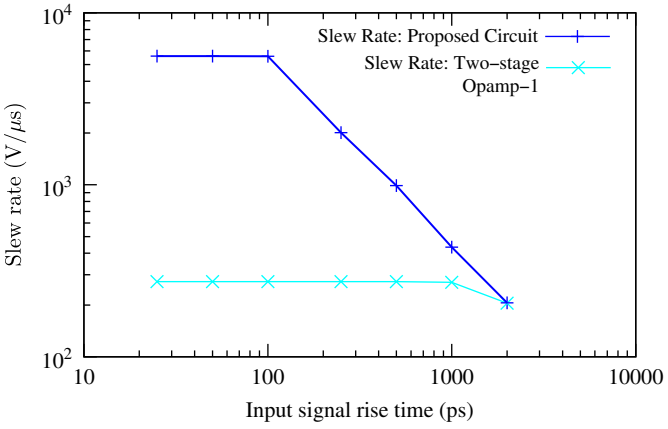

Fig. 5. The comparison of slew rates of two-stage opamp-1 and proposed circuit for an input signal with rise and fall time varying in the range of 25 ps to 2 ns.

It can be seen that the slew rate of two-stage opamp-1 is independent of input rise time. However, the slew rate of the proposed circuit, increases as rise time of the input signal decreases down to 100 ps and after that, it almost remains constant with marginal increase. The proposed circuit architecture is able to follow input signal until rise and fall time of input signal is decreased to 100 ps. Once it is reduced below 100 ps the comparator fails to detect difference of input and output signals at the same rate at which input signal changes. Therefore, comparator is not able to switch ON and switch OFF additional current sources at the same transition rate at which input signal changes (below 100 ps). Hence no more improvement is observed in the slew rate of the circuit.

Table 3 shows the settling time of all three circuits, "SR-improved Op-amp," "Two-stage Opamp-1," and "Two-stage Opamp-2". Settling time is measured as the time required for the output to reach and remain within 2% of its final value. It is measured for a load capacitance equal to 20 fF. It can be seen from the table that the settling time of "SR-improved Op-amp" is very small than that of "Two-stage Opamp-1." The settling time of "SR-improved Op-amp" is also better than that of "Two-stage Opamp-2" on the rising edge of input signal but they are comparable on the falling edge of input signal. As seen earlier, the "Two-stage Opamp-2" consumes more power, i.e., 113 μW in comparison to 78 μW of "SR-improved Op-amp" circuit. There are some overshoot and undershoot in the transient response shown in Fig. 4. Such transients occur because enhanced slew rate of op-amp (or OTA) is quite high, and hence by the time the corresponding comparator turns off, output goes beyond desired value. Overshoots and undershoots are controlled by adjusting value of current sources. In this work, we minimized it with adjustment of number of fins in FinFET devices used as current sources. Therefore, the appropriate settling time is achieved. Delay of comparators is another controlling factor which trades with the achieved slew rate.

We also tested the proposed architecture for a load capacitance of 1 pF. The two-stage op-amp was redesigned for load capacitance of 1 pF, and the comparator circuit shown in Fig. 3 was fine tuned for this new load capacitance. It increases the slew rate from 27.48 to 1043 V/μs for rising edge of input signal and from 22.19 to 176 V/μs for falling edge of input signal. The power dissipation was increased from 57 to 103 μW. Other specifications such as phase margin (60°), unity gain frequency (77.4 MHz), gain (83 dB), etc., were unchanged.

Table 3
Settling time in pico seconds (ps) for "SR-improved Op-amp," "Two-stage Opamp-1," and "Two-stage Opamp-2" for a load capacitance of 20 fF and for an input signal with rise/fall time of 50 ps. Here, $t_{s,r}$ stands for settling time on rising edge of input signal and $t_{s,f}$ for settling time on falling edge of input signal.

	SR-improved op-amp	Two-stage opamp-1	Two-stage opamp-2
$t_{s,r}$	310	1490	620
$t_{s,f}$	600	1610	660

4. Differential amplifier with CMFB circuit

In this section, we demonstrate the application of the slew rate improvement architecture for a differential amplifier with common mode feedback (CMFB) circuit. The results show that the stability of the differential amplifier with CMFB circuit does not get affected due to the inclusion of slew rate improvement architecture. The differential amplifier with CMFB circuit reported in [26] and shown in Fig. 6 is considered as an example in this work. This circuit is designed in 45 nm FinFET technology. The channel length for all FinFET devices is taken as 20 nm. The specifications of the designed circuit with and without slew rate enhancement are given in Table 4, and the number of fins for FinFET devices is shown in brackets in Fig. 6.

The slew rate improvement circuit (Fig. 3(b) and (c)) is redesigned for this example (circuit in Fig. 6). It can be seen from Table 4 that the slew rate improves from 875 to 1830 V/μS for the rising edge, and 775 to 1120 V/μS for the falling edge of the input signal with the incorporation of slew rate enhancement circuitry. The improvement in slew rate comes at the cost of increase in power dissipation from 100 to 175 μW without changing gain. The improvement in slew rate is not as good as the improvement, observed for the two-stage op-amp circuit (see Table 2), where the slew rate is increased from 273 to 5590 V/μS. This is because the differential amplifier with CMFB circuit includes three transistors, controlled by CMFB signal, operating as current sources.

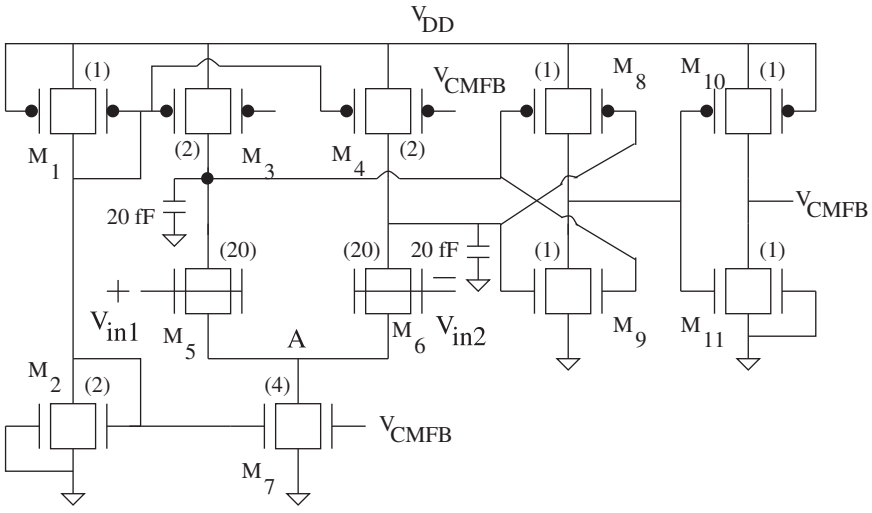

Fig. 6. Differential amplifier with common mode feedback (CMFB) circuit. The numbers in bracket shows the number of fins for the FinFET device. The channel length of FinFET device is 20 nm.

Table 4
Specification of differential amplifier (Fig. 6) with and without the slew rate improvement architecture. Settling time is measured for a step input signal with a rise and fall time of 50 ps.

Specifications	Differential amplifier	Differential amplifier with slew rate enhancement
Gain	29.22 dB	29.22 dB
Phase margin	90°	90°
Unity gain frequency	5.1 GHz	5.1 GHz
CMRR	84.96 dB	84.96 dB
Power dissipation	100 μW	175 μW
Offset voltage	83 μV	83 μV
Slew rate rise	875 V/μS	1830 V/μS
Slew rate fall	775 V/μS	1120 V/μS
Rise settling time	215 ps	75 ps
Fall settling time	395 ps	415 ps

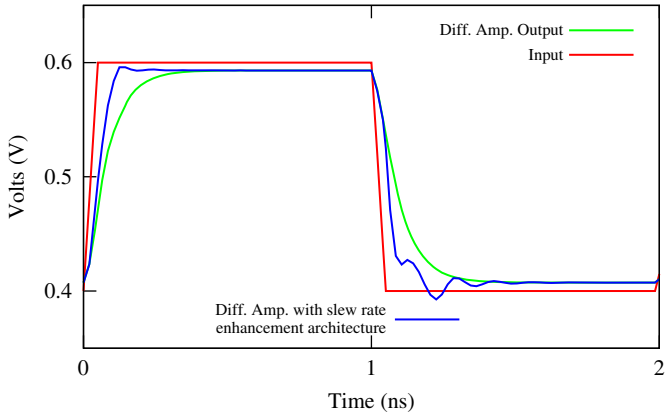

Fig. 7. The figure shows the transient response of differential amplifier with and without slew rate improvement architecture for an input signal with a rise and fall time of 50 ps.

The settling time for the differential amplifier with and without slew rate improvement architecture is measured for an input signal with a rise and fall time of 50 ps. It can be seen from Table 4 that the settling time improves considerably for the rising edge of the input signal, whereas it slightly deteriorates for the falling edge of the input signal. The one reason is the same; the unity gain frequency of the differential amplifier is a very high. The second reason is, the input common mode range of the comparator is not sufficient. The second reason can be taken care by using the comparators with better or rail-to-rail input common mode range. It should be noted that the average of settling time at rising and falling edge is better in case when the slew rate improvement circuit is present. The transient response of the differential amplifier with and without slew rate improvement architecture is shown in Fig. 7 for an input signal with a rise and fall time of 50 ps.

The above results clearly show that the stability of the differential amplifier with CMFB circuit does not get affected due to the presence of the slew rate improvement architecture.

It may be noted that the increase in power dissipation in a circuit with slew rate enhancement architecture come from the power dissipated in SR enhancement circuitry. Detect and control circuit (SR enhancement circuitry) can be shared among several op-amps in applications, where input of all op-amps is connected to similar signals. Therefore, the power dissipation in slew rate enhancement circuitry will be shared among multiple op-amps and the percentage increase in power dissipation will be further reduced. The sharing of detect and control parts of the slew rate enhancement circuitry among multiple op-amps will be covered in a separate work.

5. Conclusions

A novel architecture and technique for improving slew rate of op-amps or OTAs is presented. The proposed architecture is realized for two sample circuits optimized in 45 nm FinFET technology: (i) two-stage op-amp and (ii) differential amplifier with CMFB circuit. The slew rate of two-stage op-amp is increased from 273 to 5590 V/μs with a marginal increase in power dissipation from 46 to 78 μW for an input signal with a rise time of 100 ps. The slew rate of differential amplifier with CMFB improved from 875 to 1830 V/μS for the rising edge, and 775 to 1120 V/μS for the falling edge of the input signal with the incorporation of slew rate enhancement circuitry in the second circuit example. DC gain and stability of differential amplifier with CMFB circuit are not affected with the inclusion of slew rate improvement architecture.

Acknowledgments

The authors would like to thank Michael Fulde from Infineon for useful discussions and Center for Nanoelectronics, Department of Electrical Engineering, IIT-Bombay for support. Synopsis is gratefully acknowledged for Sentaurus licenses. Patent application for the proposed idea has been filed under application no. IN-800533 for Indian and US patents.

References

[1] B. Wu, J. Mavor, High slew rate CMOS operational amplifier employing internal transistor compensation, Microelectronics Journal 14 (5) (1983) 5–13.
[2] M.V. Ivanov, M. Ismail, V.N. Ivanov, High slew rate micro-power CMOS OTA with class AB input stage, in: Proceedings of the 40th Midwest Symposium on Circuits and systems, vol. 2, 1997, pp.1197–1200. doi:10.1109/MWSCAS.1997.662294.
[3] P.C. Subramaniam, et al., High slew-rate CMOS operational amplifier, Electronics Letter 39 (8) (2003) 640–641.
[4] A.J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, R.G. Carvajal, Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency, IEEE Journal of Solid-State Circuits 40 (5) (2005) 1067–1077.
[5] J. Ramirez-Angulo, R.G. Carvajal, A. Lopez-Martin, High slew rate two stage A/AB and AB/AB op-amps with phase lead compensation at output node and local common mode feedback, in: IEEE International Symposium on Circuits and Systems (ISCAS), 2008, pp. 288–291, doi:10.1109/ISCAS.2008.4541411.
[6] M. Song, D. Ma, A fast-transient over-sampled delta-sigma adaptive DC–DC converter for power-efficient noise-sensitive devices, in: ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2007, pp. 286–291.
[7] A.-R. Kim, H.-R. Kim, Y.-S. Park, Y.-K. Choi, B.-S. Kong, Low-power class-AB CMOS OTA with high slew-rate, in: International Symposium on System on Chip (SoC), 2009, pp. 313–316.
[8] S. Gopalkrishna, G. Krishna, B. Jalali-Farahani, A fast settling slew rate enhancement technique for operational amplifiers, in: 53rd IEEE International Midwest Symposium on Circuits and Systems, 2010, pp. 965–968.
[9] S.-K. Shin, et al., A slew rate controlled output driver using PLL as compensation circuit, in: Proceedings of IEEE ESSCIRC, 2002, pp. 207–210.
[10] A.P. Perez, Y.B. Nithin Kumar, E. Bonizzoni, F. Maloberti, Slew-rate and gain enhancement in two stage operational amplifiers, in: IEEE International Symposium on Circuits and Systems (ISCAS), 2009, pp. 2485–2488.
[11] S. Yin, Y. Sun, X. Li, Digital 1 V 82 μW pseudo-two-stage class-AB OTA, Tsinghua Science and Technology 14 (5) (2009) 601–605.
[12] S.C. dela Cruz, M.G.T. delos Reyes, T.C. Gaffud, T.V.F. Abaya, M.T.A. Gusad, M.D. Rosales, Design and implementation of operational amplifiers with programmable characteristics in a 90 nm CMOS process, in: European Conference on Circuit Theory and Design (ECCTD), 2009, pp. 209–212.
[13] J. Ramírez-Angulo, R.G. Carvajal, A. Torralba, C. Nieva, A new Class-AB differential input stage for implementation of low-voltage highslew rate op-amps and linear transconductors, in: Proceedings of IEEE International Symposium Circuits and Systems, ISCAS, vol. 1, May 2001, pp. 671–674, doi:10.1109/ISCAS.2001.921945.
[14] F. Moraveji, A wide-band, low-power, high slew rate voltage feedback operational amplifier, IEEE Journal of Solid-State Circuits 31 (1) (1996) 10–16.
[15] N. Charalampidis, K. Hayatleh, B.L. Hart, F.J. Lidgey, A wide bandwidth voltage-follower with low distortion and high slew rate, in: Proceedings of the 13th IEEE International Conference on Electronics, Circuits and Systems, (ICECS), December 2006, pp. 256–259. doi:10.1109/ICECS.2006.379774.

[16] J.T. Sundby, CMOS opamp with large sinking and sourcing currents and high slew rate, U.S. Patent No. 5325069, June 1994.
[17] M. Miura, Operational amplifier with self control circuit for realizing high slew rate throughout full operating range, U.S. Patent No. 6987420 B2, January 2006.
[18] K. Feng-Sung, Slew rate enhancement circuit via dynamic output stage, U.S. Patent No. 7164298 B2, January 2007.
[19] C.-H. Chuang, T.-K. Tseng, H.-C. Jiang, Slew-rate control circuitry with output buffer and feedback, U.S. Patent No. 7652511 B2, January 2010.
[20] Synopsys Sentaurus Design Suite [Online]. 〈http://www.synopsys.com〉.
[21] M. Srivastava, B. Verma, M.S. Baghini, C. Russ, D.K. Sharma, H. Gossner, V. Ramgopal Rao, Benchmarking the device performance at sub 22 nm node technologies using an SoC framework, in: IEEE Electron Devices Meeting, 7–9 December 2009, pp. 505–508.
[22] K. von Arnim, et al., A low-power multi-gate FET CMOS technology with 13.9 ps inverter delay, large-scale integrated high performance digital circuits and SRAM, in: IEEE Symposium on VLSI Technology, 12–14 June 2007, pp. 106–107.
[23] R.A. Thakker, C. Sathe, A.B. Sachid, M.S. Baghini, V. Ramgopal Rao, M.B. Patil, A novel table-based approach for design of FinFET circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (July) (2009) 1061–1070.
[24] M.B. Patil, A new public-domain program for mixed-signal simulation, IEEE Transactions on Education 45 (2) (2002) 187–193.
[25] R.A. Thakker, C. Sathe, A.B. Sachid, M.S. Baghini, V. Ramgopal Rao, M.B. Patil, Automated design and optimization of circuits in emerging technologies, in: Proceedings of the 14th Asia and South Pacific Design Automation Conference, January 2009, pp. 504–509.
[26] M. Srivastava, M.S. Baghini, D.K. Sharma, V. Ramgopal Rao, A novel and robust approach for common mode feedback using IDDG FinFET, IEEE Transactions on Electron Devices 55 (11) (2008) 3274–3282.