

# A Tunnel FET for $V_{DD}$ Scaling Below 0.6 V With a CMOS-Comparable Performance

Ram Asra, Mayank Shrivastava, *Member, IEEE*, Kota V. R. M. Murali, Rajan K. Pandey, Harald Gossner, *Member, IEEE*, and V. Ramgopal Rao, *Senior Member, IEEE*

**Abstract**—We propose a modified structure of tunnel field-effect transistor (TFET), called the sandwich tunnel barrier FET (STBFET). STBFET has a large tunneling cross-sectional area with a tunneling distance of  $\sim 2$  nm. An orientation-dependent nonlocal band-to-band tunneling (BTBT) model was employed to investigate the device characteristics. The feasibility of the STBFET realization using a complementary metal–oxide–semiconductor-compatible process flow has been shown using advanced process calibration with Monte Carlo implantation. STBFET gives a high  $I_{ON}$ , exceeding  $1 \text{ mA}/\mu\text{m}$  at  $I_{OFF}$  of  $0.1 \text{ pA}/\mu\text{m}$  with a subthreshold swing below  $40 \text{ mV}/\text{dec}$ . The device also shows better static and dynamic performances for sub-1-V operations. STBFET shows a very good drain current saturation, which is investigated using an ab initio physics-based BTBT model. Furthermore, the simulated  $I_{ON}$  improvement is validated through analytical calculations. We have also investigated the physical root cause of the large voltage overshoot of TFET inverters. The previously reported impact of Miller capacitance is shown to be of lower importance; the space-charge buildup and its relaxation at the channel drain junction are shown to be the dominant effect of large voltage overshoot of TFETs. The STBFET are shown to have negligible voltage overshoots compared with conventional TFETs.

**Index Terms**—Band-to-band tunneling (BTBT), depletion region, epitaxial channel region, high- $k$  spacer, inverter circuits, Miller capacitance, sandwich tunnel barrier, space charge and relaxation, tunneling field-effect transistor (TFET), voltage overshoot.

## I. INTRODUCTION

COMPLEMENTARY metal–oxide–semiconductor (CMOS) technology has scaled down from micrometer feature sizes to nanoscale regimes in order to achieve low-power and high-performance devices and circuits. Device geometry has been reduced as the gate length  $L_G$ , gate dielectric thickness  $T_{ox}$ , and junction depth have been decreased by about 3 orders of magnitude. For lower OFF-current  $I_{OFF}$ , a better gate control

Manuscript received September 9, 2010; revised March 17, 2011; accepted May 12, 2011. Date of publication July 8, 2011; date of current version June 22, 2011. The review of this paper was arranged by Editor G. Jeong.

R. Asra and V. R. Rao are with the Center of Excellence in Nanoelectronics, Department of Electrical Engineering Indian Institute of Technology (IIT) Bombay, Mumbai 400076, India (e-mail: ram.asra@gmail.com; rrao@ee.iitb.ac.in).

M. Shrivastava is with the Intel Mobile Communications, Hopewell Junction, NY, 12533 USA (e-mail: mayank.shrivastava@intel.com).

K. V. R. M. Murali and R. K. Pandey are with the IBM Semiconductor Research and Development Center, Bangalore 560045, India.

H. Gossner is with the Intel Mobile Communications, 85579 Neubiberg, Germany (e-mail: harald.gossner@intel.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TED.2011.2140322

of the channel is needed in the OFF-state [1]. In order to meet the ON-current  $I_{ON}$  requirements, the threshold voltage  $V_{TH}$  needs to be scaled with  $V_{DD}$ . However,  $I_{OFF}$  exponentially increases with  $V_{TH}$  reduction and is given by

$$I_{OFF} = I_{DS} \cdot 10^{-V_{TH}/SS} \quad (1)$$

with  $SS = \eta(kT/q) \ln 10$  and  $\eta = 1 + (C_{dep}/C_{ox})$ . In (1), SS is the subthreshold slope of the device and depends on junction capacitance  $C_{dep}$  and gate capacitance  $C_{ox}$ . SS is a nonscalable parameter, and minimum subthreshold swing  $SS_{min}$  is  $60 \text{ mV}/\text{dec}$  at room temperature. Hence,  $V_{TH}$  has become a nonscalable parameter to limit the  $I_{OFF}$ . However, due to the short-channel effects (SCEs), SS is far worse than an ideal value of  $60 \text{ mV}/\text{dec}$ . In order to limit  $I_{OFF}$  while scaling down  $V_{TH}$ , it is important to look for new device structures that achieve subthreshold swing below  $60 \text{ mV}/\text{dec}$ . Recently, many CMOS devices such as the nanowire gate-all-around (GAA) metal–oxide–semiconductor field-effect transistors (MOSFETs) [1], fin-shaped FET [2], carbon nanotube FET, impact-ionization MOSFETs (I-MOSFET) [3], and TFETs [4] have been demonstrated to minimize SCE and to lower the source–drain leakage current. Among these devices, only TFET and I-MOSFET promise SS less than  $60 \text{ mV}/\text{dec}$  and improved short-channel performance. We propose sandwich tunnel barrier FET (STBFET) with  $1.4 \text{ mA}/\mu\text{m}$  of  $I_{ON}$  at an  $I_{OFF}$  of  $0.1 \text{ pA}/\mu\text{m}$  with SS less than  $40 \text{ mV}/\text{dec}$ .

## II. CALIBRATION OF TFET

In order to understand and validate the STBFET device performance, we first calibrate the conventional TFET using ab initio band-to-band tunneling (BTBT) model. This calibration is used as the basis for all the devices evaluated in this paper. Shown in Fig. 1(a) is a gated p-i-n diode. The ON- and OFF-state currents of the device are due to BTBT in a reverse-biased p-n junction. An increase in the gate voltage leads to a sharp band bending at  $P^+$  source–channel interface, as shown in Fig. 1(b). This reduces the tunneling distance  $d_{Tunnel}$  to about  $5 \text{ nm}$ , where charge carriers can tunnel from the valence band to the conduction band leading drive current.

A nonlocal BTBT model developed in Finite Element Device Analysis [5], [6] for the TFET calibration has been used. The model uses the complex band structure of Si to compute the orientation-dependent effective mass and complex  $k$ -vector in the tunneling region. The tunneling probability is calculated using the transfer matrix formalism to calculate

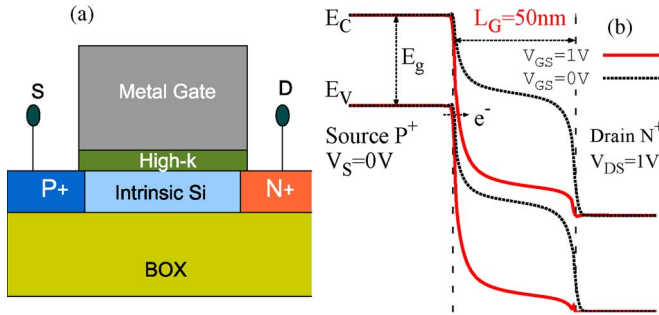


Fig. 1. (a) Schematic of a conventional silicon-on-insulator TFET structure with high- $k$  and metal gate. (b) Energy band diagram of a simulated n-TFET with  $V_{DS}$  of 1 V. At  $V_{GS} = 0$  V, the band bending is such that no electronic states are available for tunneling from the source into the channel region. However, at  $V_{GS} = 1$  V, there is very sharp band bending at the source-channel interface, enabling the valence band electrons to tunnel into the conduction band in the channel.

TABLE I  
EXPERIMENTAL DEVICE PARAMETERS THAT ARE ALSO  
USED FOR THE DEVICE CALIBRATION

Parameter	Value	Unit	Parameter	Value	Unit
$L_G$	600	nm	$N^+$ doping	$1.5 \times 10^{20}$	$\text{cm}^{-3}$
Nanowire thickness	70	nm	$P^+$ doping	$5 \times 10^{18}$	$\text{cm}^{-3}$
Dielectric (HfO <sub>2</sub> )	5	nm	-	-	-

the drive current. This model has been successfully used to quantitatively model the gate-induced drain leakage currents in 45-nm low-power devices and vertical diode of different orientations, viz., along [100], [110], and [111] orientations [6]. Here, calibration of a p-TFET with experimental data is shown in Fig. 2(a). A nonlocal BTBT with field-dependent mobility, Shockley-Read-Hall, and Hurkx recombination models have been used for simulations. The TFET parameters used for the simulation are same as those of the experimental device [4] and are listed in Table I. We carried out simulations in three distinct transport orientations, namely, [100], [110], and [111]. Notice that [110] and [111] transport give an order of magnitude higher BTBT current compared with [100] transport for the gate voltage window from  $-0.5$  to  $-1.5$  V. For higher gate voltages, all the three orientations give similar BTBT currents, which is to be expected given the narrowing of the tunnel barrier, hence, reduced sensitivity to the effective mass of the carriers. The simulation results for the BTBT clearly show an excellent match with experimental results, as shown in Fig. 2(a). With equivalent oxide thickness (EOT) scaling, gate transverse field increases, which in turn leads to charge carrier quantization in the channel. To properly include the quantum effects in the simulation, the modified local density approximation (MLDA) and density of states (DOS) quantum correction models are applied to calculate the carrier distribution in the channel. In Fig. 2(b) MLDA and DOS quantum correction models are well calibrated again with Schrodinger-Poisson (SP) solution [7].

Notice that the conventional silicon TFET devices suffer from low  $I_{ON}$  because of the larger tunnel distance [8].  $I_{ON}$  can be increased by using lower band-gap materials at the source [9], using abrupt doping profiles at the source-channel interface or by introducing a lateral strain [10].  $I_{ON}$  can be increased

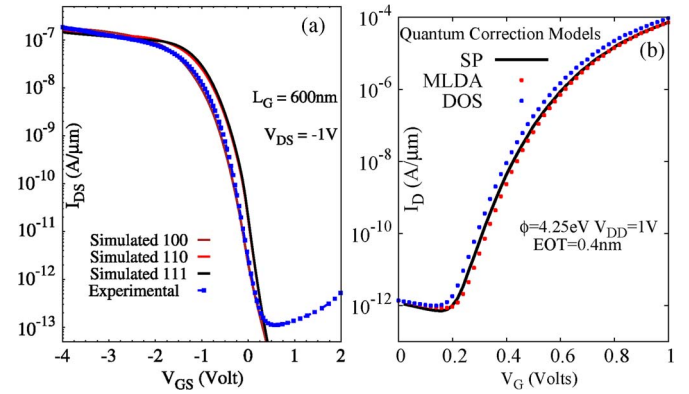


Fig. 2. (a) Simulated p-channel TFET transfer characteristics for [100], [110], and [111] crystallographic orientations are well matched with the experimental characteristics. The gate length of the device is 600 nm, with 5 nm of HfO<sub>2</sub> as the gate dielectric. Si body thickness is 70 nm, with  $N^+$  source doping of  $1.5 \times 10^{20} \text{ cm}^{-3}$  and  $P^+$  drain doping of  $5 \times 10^{18} \text{ cm}^{-3}$ . With  $V_{DS} = -1.0$  V and  $V_{GS} = -4.0$  V,  $I_{ON}$  is  $0.2 \mu\text{A}/\mu\text{m}$ . (b) The TFET transfer characteristics with various quantum correction models (original MLDA-based and DOS models) are calibrated with the SP solution.

by the aforementioned methods; however, the reported values are much lower than that of the MOSFET devices. Additionally, it has been reported that only increasing the  $I_{ON}$  of the conventional TFETs is not sufficient to improve the circuit performance [11]. In this paper, we propose a modified TFET device structure, which is called the STBFET. The proposed device shows high  $I_{ON}$  at  $I_{OFF}$  of  $0.1 \text{ pA}/\mu\text{m}$ , low SS below  $40 \text{ mV}/\text{dec}$ , and MOSFET-like output characteristics.

### III. STBFET DEVICE STRUCTURE AND OPERATION

The structure of the proposed n-channel STBFET along with device parameters is shown in Fig. 3. The channel region is a 2-nm-thin epitaxially grown Si layer, which can be realized using low-temperature molecular beam epitaxy [12] or chemical vapor deposition (CVD). CVD is the dominating Si/SiGe epitaxy process used in CMOS industry and is used to produce high-quality monocrystalline epitaxial devices [13]. This process can be extended to achieve abrupt degenerate doping profiles [13], [14] at slightly elevated substrate temperatures such as  $600^\circ\text{C}$ , which is also effective in reducing the defects [15]. Gate stack consists of a high- $k$  dielectric and metal gate with an appropriate work function.

Unlike a conventional TFET structure, the  $P^+$  source is under the gate and channel region. Boron doping of  $2 \times 10^{20} \text{ cm}^{-3}$  for source and phosphorus doping of  $5 \times 10^{19} \text{ cm}^{-3}$  for drain are used for the simulations. Here, we have assumed a lateral doping profile of  $2 \text{ nm}/\text{dec}$ , which has been realized in the literature using advanced annealing processes [16]. The  $N^+$  drain is located on either side of the high- $k$  spacers. High- $k$  spacers are used to reduce the channel resistance by using the gate-fringe effect [17].

A simulated device cross section of STBFET is shown in Fig. 3, along with the electron density and the depletion width contours.  $P^+$  source and  $N^+$  drain are separated by a 20-nm-thick high- $k$  spacer. At  $V_{GS} = 0$  V and  $V_{DS} = 1$  V, there is no channel inversion under the gate and spacer region. Under such a bias condition, the device can be analyzed as a p-i-n

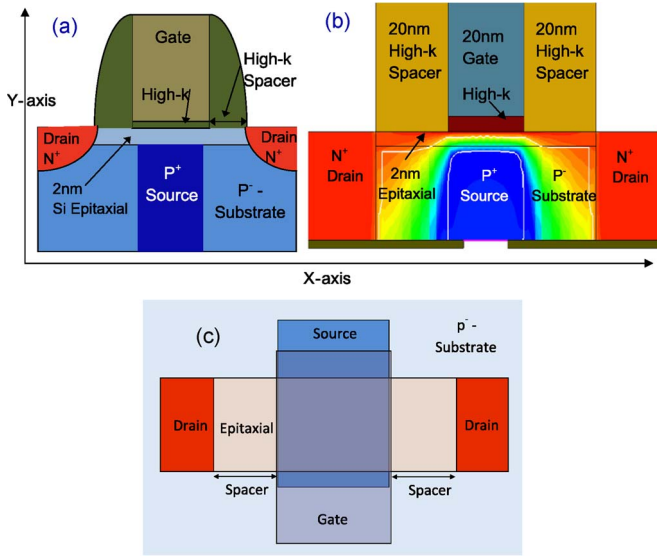


Fig. 3. (a) A cross-sectional view of the STBFET with metal gate, high- $k$  gate dielectric, high- $k$  spacer, and a 2-nm-thick Si channel layer. Unlike conventional TFETs,  $P^+$  source is under the gate below the epitaxial layer, and the drain is on both sides of the spacer. (b) A cross-sectional view of the STBFET at  $V_{DS} = V_{GS} = 1$  V is shown along with the electron density and the depletion width (white line). The source doping of  $2 \times 10^{20} \text{ cm}^{-3}$  and drain doping of  $5 \times 10^{19} \text{ cm}^{-3}$  has been used for the simulation. (c) The top view of the device, which illustrates the contacts taken at the top.

diode with a  $P^+$  source and an  $N^+$  drain separated by a lightly doped/intrinsic region and a separation equivalent to the thickness of high- $k$  spacer. Hence, the tunnel direction is lateral, and the tunnel distance becomes equal to spacer thickness, which is 20 nm for the optimized device in this paper. It is well understood that at such a tunnel distance BTBT current has to be extremely low, which is responsible for the device's excellent OFF-state behavior. Furthermore, with the increase in the gate bias, an inversion layer forms in the epilayer underneath the MOS gate and the high- $k$  spacers. Under such a bias condition, the device can be analyzed as a  $P^+N^+$  reverse biased diode with a tunnel distance equivalent to the epilayer thickness. This switches the tunneling direction from lateral to vertical direction, thus reducing the  $d_{\text{Tunnel}}$  to about 2 nm, as shown in Fig. 3(b). This abrupt change in the tunnel distance leads to a steep subthreshold swing and a large BTBT current. A high- $k$  spacer is required to achieve high  $I_{\text{ON}}$ , without which the ON-current degrades due to the high channel resistance. This increase in the ON-current and the steep subthreshold swing compensates for the increase in parasitic capacitance due to the high- $k$  spacer. In Fig. 3(c), the top view of the STBFET is shown with the contacts patterned on the top of the device. Note that the active source tunneling cross-sectional area  $A_{\text{Tunnel}}$  is equal to the  $(W \times L)$  area of the gate. This tunneling area is much larger than the tunneling cross-sectional area in conventional TFETs, which is partly responsible for higher  $I_{\text{ON}}$  observed in STBFET.

#### A. STBFET Device Simulation Result and Analysis

A physical explanation for high  $I_{\text{ON}}$  and excellent output current saturation in STBFET compared with a conventional

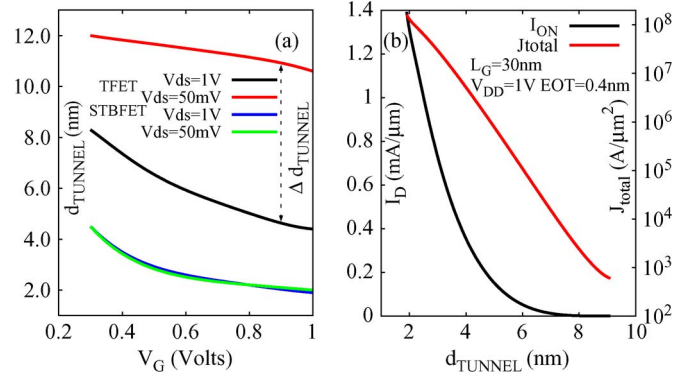


Fig. 4. (a) Simulation results show the tunneling distance as a function of  $V_{GS}$  and  $V_{DS}$  for the STBFET and a conventional TFET. In the STBFET,  $d_{\text{Tunnel}}$  is half that of the TFET at  $V_{GS} = 1$  V. In addition, in the STBFET, the effect of drain electric field on  $d_{\text{Tunnel}}$  is negligible as  $\Delta d_{\text{Tunnel}}$  is negligible compared with  $\Delta d_{\text{Tunnel}}$  of the TFET. (b) Total current density as a function of  $d_{\text{Tunnel}}$  for the STBFET is shown. Variation in  $d_{\text{Tunnel}}$  is achieved by varying the epitaxial layer thickness.

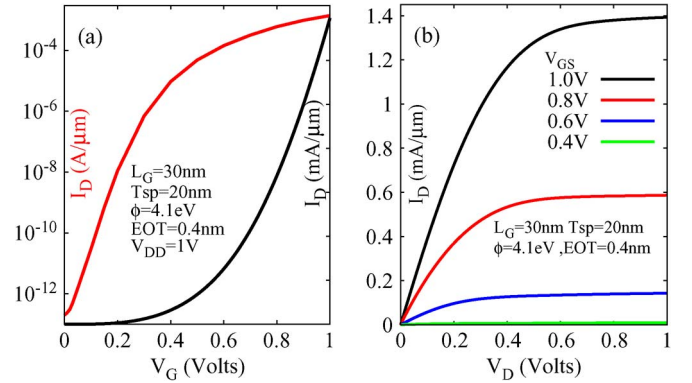


Fig. 5. (a) Transfer characteristics of the n-channel STBFET. (Shown on the log scale)  $I_{\text{OFF}}$  of the device is  $0.1 \text{ pA}/\mu\text{m}$  and (also shown on the linear scale)  $I_{\text{ON}} \sim 1.4 \text{ mA}/\mu\text{m}$ . The STBFET shows an SS below 40 mV/dec. (b) The Simulation result shows that the output characteristics of an n-channel STBFET has very good saturation like long-channel MOSFET.

TFET is provided. In a conventional TFET, it is very difficult to decrease  $d_{\text{Tunnel}}$  below 4 nm as  $d_{\text{Tunnel}}$  is controlled by the gate and drain electric fields [8]. However, in the STBFET,  $d_{\text{Tunnel}}$  can be lowered down to 2 nm as it is determined by the epitaxial layer thickness  $t_{\text{epi}}$ , as shown in Fig. 3(b). In Fig. 4(a), the minimum  $d_{\text{Tunnel}}$  for the STBFET is half that of the TFET. High  $I_{\text{ON}}$  of the STBFET is due to small tunneling distance  $d_{\text{Tunnel}}$ , which leads to a higher BTBT current density  $J_{\text{Tunnel}}$ . In STBFET,  $J_{\text{Tunnel}} = 1.6 \times 10^8$ , which is more than 2 orders of magnitude higher than that of a TFET ( $J_{\text{Tunnel}} = 8.0 \times 10^5$ ), as shown in Fig. 4(b). Because of the combined effects of the aforementioned parameters,  $I_{\text{ON}}$  of the STBFET is much higher than that of a conventional TFET.

The transfer characteristics of an n-channel STBFET are shown in Fig. 5(a) for epitaxial layer thickness of 2 nm and gate length  $L_G$  of 20 nm. The gate work function of STBFET is set to 4.1 eV. The simulated  $I_{\text{ON}}$  is  $1.4 \text{ mA}/\mu\text{m}$  when compared with  $70 \text{ } \mu\text{A}/\mu\text{m}$  in a conventional silicon TFET at  $V_{DS} = V_{GS} = 1.0$  V. Additionally, the STBFET shows very low  $I_{\text{OFF}}$  ( $0.1 \text{ pA}/\mu\text{m}$ ) and a steep subthreshold swing below 40 mV/dec. The output characteristic of the STBFET shows



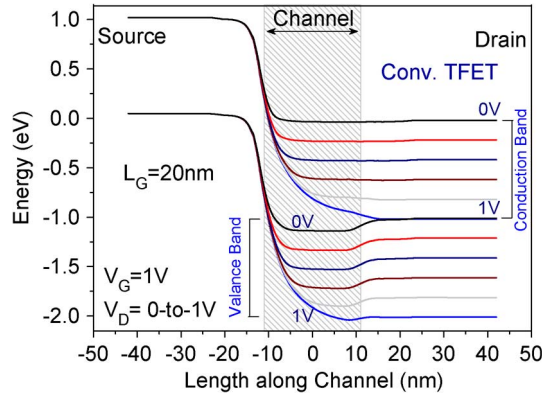


Fig. 6. Energy band diagram of conventional TFET for  $V_{GS}$  of 1 V and  $V_{DS}$  from 0 to 1 V in steps of 0.2 V is shown. For increase in  $V_{DS}$ , from 0 to 1 V, bands are flat in the channel and in the  $N^+$  doped drain region. However, there is a large band bending at the source–channel interface. The slope of the band bending increases with the drain bias. This shows that the total applied drain voltage drops across the source–channel tunnel junction. This results in decreasing tunnel width, and hence, good saturation is not observed.

a good saturation of drain current [see Fig. 5(b)]. In TFETs, drain-current saturation is affected by the tunnel distance saturation, which is a function of  $V_{GS}$  and  $V_{DS}$ . At a given  $V_{GS}$ ,  $\Delta d_{\text{Tunnel}} = (d_{\text{Tunnel}, V_{DS}=0 \text{ V}} - d_{\text{Tunnel}, V_{DS}=1 \text{ V}})$  is a function of  $V_{DS}$ , as shown in Fig. 4(a). The tunnel distance has reached its minimum value at  $V_{DS} = 50 \text{ mV}$ , and it does not reduce further with applied drain voltage. Thus,  $\Delta d_{\text{Tunnel}}$  for STBFET as a function of drain bias is negligible, as compared with  $\Delta d_{\text{Tunnel}}$  of a conventional TFET.  $d_{\text{Tunnel}}$  saturation, i.e.,  $\Delta d_{\text{Tunnel}} = 0$  in STBFET, is the cause of excellent output current saturation.

A physical explanation for the  $d_{\text{Tunnel}}$  saturation can be understood as follows. Conventional TFETs have two threshold voltages, i.e., gate threshold voltage and drain threshold voltage [18]. This is based on the tunnel width narrowing with respect to  $V_{GS}$  and  $V_{DS}$ . However, it is worth mentioning that STBFET has only one threshold voltage, i.e., gate threshold voltage as the drain voltage negligibly reduces the tunnel width. We have investigated this effect, and the results are shown in Figs. 6 and 7. Fig. 6 shows the energy band diagram of a conventional TFET for  $V_{GS}$  of 1 V and  $V_{DS}$  from 0 to 1 V in steps of 0.2 V. For increase in  $V_{DS}$ , i.e., from 0 to 1 V, bands are flat in the channel region and in the  $N^+$  doped drain region. However, there is a large band bending at the source–channel interface. From the slope of the band bending, it can be implied that the applied drain voltage essentially appears across the tunnel junction, which is at the source–channel interface. Hence, with increase in  $V_{DS}$ , the tunnel distance reduces, and the field across the tunnel junction increases. This causes the drain current to increase, and hence, saturation in the output characteristics cannot be observed. However, in the case of the STBFET, the band bending (due to drain voltage) at the tunnel junction is negligibly small. The energy band diagram (along  $x$ -axis in the epitaxial region) of the STBFET for  $V_{GS}$  of 1 V and  $V_{DS}$  from 0 to 1 V in steps of 0.2 V is also shown in Fig. 7. In the STBFET, an increase in  $V_{DS}$  leads to a large band bending in the spacer–channel region, with negligible drop across the source–channel region. Since the voltage drop across the tunnel

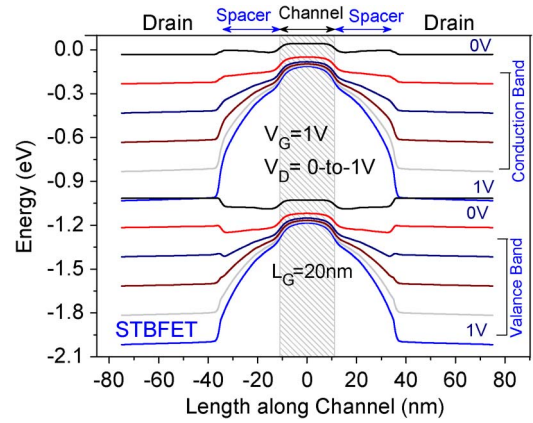


Fig. 7. Energy band diagram (along  $x$ -axis in the epitaxial region) of the STBFET for  $V_{GS}$  of 1 V and  $V_{DS}$  from 0 to 1 V in steps of 0.2 V is shown. For increase in  $V_{DS}$ , from 0 to 1 V, there is large band bending in the spacer–channel region only. This shows that the most of the drain voltage drops in the spacer–channel region. There is only 0.1 eV of band bending that has been observed in the channel region under the gate due to the drain bias. It is clear that the total  $V_{DS}$  drops across the spacer–channel region and not at the tunnel junction. Hence, the STBFET shows very good saturation in the output characteristics.

junction does not vary with the drain bias, there is negligible modulation of the tunnel distance. This results in excellent output saturation characteristics of the STBFET.

### B. Analytical Calculations of $ON$ -Current

In TFETs, the physical significance of  $V_{\text{TH}}$  definition is the saturation of tunnel width narrowing [18]. In the conventional TFET, the  $d_{\text{Tunnel}}$  keeps on reducing even for  $V_{GS}$  larger than 1 V. However, in the case of STBFET,  $V_{\text{TH}}$  is defined as the  $V_{GS}$  required for the formation of inversion layer, which is similar to that of a MOSFET. As the channel is in weak inversion,  $d_{\text{Tunnel}}$  is reduced to its minimum value of 2 nm. Further increase in  $V_{GS}$  only increases the carrier concentration in the inversion layer. Because of the epitaxial layer in the channel, the doping profile can be approximated to that of an extreme retrograde profile (Low–High).  $V_{\text{TH}}$  of a retrograde doping profile is given by the following [19]:

$$V_{\text{TH}} = V_{\text{fb}} + 2\psi_B + \frac{qN_a}{C_{\text{ox}}} \sqrt{\frac{4\epsilon_{\text{si}}\psi_B}{qN_a} + t_{\text{epi}}^2} - \frac{qN_a t_{\text{epi}}}{C_{\text{ox}}} \quad (2)$$

where  $V_{\text{fb}}$  is the flatband voltage,  $N_a$  is the substrate doping,  $\psi_B$  is the bulk potential, and  $\epsilon_{\text{si}}$  is the permittivity of silicon.

The importance of the epitaxial layer in the STBFET is realized from the fact that without the epitaxial layer the threshold voltage [19] would be greater than 4 V for a source doping of  $2 \times 10^{20} \text{ cm}^{-3}$ . Hence, for sub-1-V operation, vertical tunneling is not possible without the epitaxial layer in the channel. As the substrate doping is high ( $\geq 10^{20}$ ),  $t_{\text{epi}} \gg (4\epsilon_{\text{si}}\psi_B/qN_a)^{1/2}$  and (2) can be reduced to the following [19]:

$$V_{\text{TH}} = V_{\text{fb}} + 2\psi_B + \frac{\epsilon_{\text{si}} 2\psi_B}{t_{\text{epi}} \times C_{\text{ox}}} \quad (3)$$

The  $V_{\text{TH}}$  of a steep retrograde doping profile for 2 nm of  $t_{\text{epi}}$  is about 0.2 V. Hence, a thin epitaxial layer enables the vertical

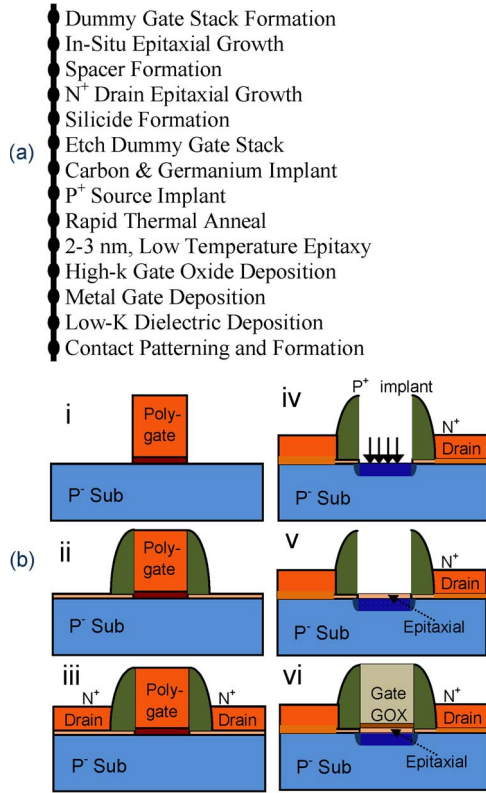


Fig. 8. (a) Proposed CMOS compatible process flow for the STBFET device and (b) CMOS-compatible process flow chart (i–vi) for the STBFET device.

tunneling for sub-1-V operation. A well-established method for  $V_{TH}$  extraction of nonlinear device called linear extrapolation of  $I_D/g_m^{1/2}$  versus  $V_{GS}$  plot gives  $V_{TH}$  of 0.23 V for the case of STBFET. This is very close to the  $V_{TH}$  calculated from (3). Note that  $I_D/g_m^{1/2}$  versus the  $V_{GS}$  method is not suitable for the conventional TFET as it cannot linearize the  $I_D$ – $V_{GS}$  curve.

In order to further justify the observed high  $I_{ON}$  in the STBFET, the device parameters are used with analytical expressions to calculate the field and ON-current [20] as

$$I = A_{Tunnel} \times A \times V_{eff} \times E \times \exp\left(-\frac{B}{E}\right). \quad (4)$$

In (4), the constants  $A$  and  $B$  are given by  $A = (q^3 \sqrt{2m^*}/E_G/4\pi^2 \times \hbar^2)$  and  $B = (4\sqrt{m^*}\sqrt{E_G^3}/3q \times \hbar)$ , where  $m^*$  is the carrier effective mass,  $E_G$  is the band gap,  $\hbar$  is the reduced Planck constant, and  $V_{eff}$  is the effective bias at the tunnel junction. For the effective mass, widely accepted parabolic effective mass approximation [21], [22] has been used. The analytical expression shown in (4) is in agreement with the tunneling current of  $p^+ - n^+$  tunnel junctions [20].  $E$  is the vertical electric field and can be obtained in two ways. First, using  $E$  from the device simulator, (4) gives  $I_{ON}$  of 1.6 mA/ $\mu\text{m}$ . Second,  $E$  has been calculated using the following [20]:

$$E = \frac{(V_{GS} - V_{TH}) + V_{Tunnel}}{(t_{epi} + 3T_{ox})} \quad (5)$$

where  $qV_{Tunnel}$  is the minimum energy-band bending needed for tunneling and must be greater than  $E_G$ . The ratio of silicon

TABLE II  
PROCESS PARAMETERS FOR THE SIMULATION OF N-CHANNEL STBFET

Parameter	Value	Unit	Parameter	Value	Unit
Carbon Dose	$10^{15}$	$\text{cm}^{-2}$	$N^+$ doping	$10^{20}$	$\text{cm}^{-3}$
Boron Dose	$10^{15}$	$\text{cm}^{-2}$	$\phi_m$	4.1	eV
Implant Energy	1.3-2	keV	EOT	0.4	nm
Tilt Angle	15-18	Degree	Spacer	20-25	nm
Aneal Temp.	980	$^{\circ}\text{C}$	Spacer-k	20	-
Aneal Time	2	Sec	tepi	2	nm

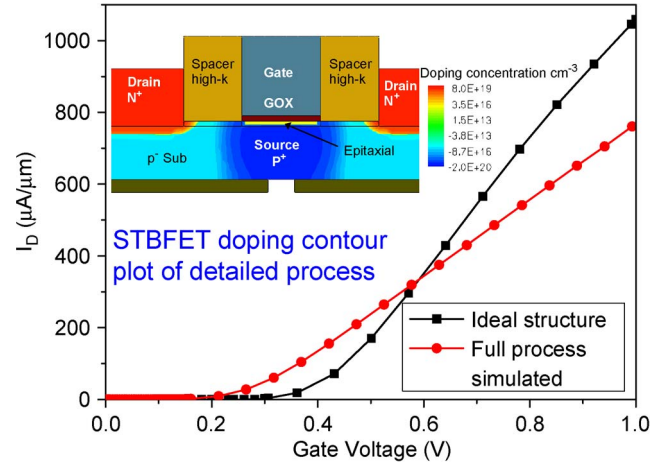


Fig. 9. Advanced process calibration with Monte Carlo simulated implantations has been used for the STBFET process simulation. The figure shows the transfer characteristics of an STBFET device obtained after full process simulation. A small degradation in the  $I_{ON}$  due to boron diffusion in the epitaxial region under the spacer is observed compared to that of an ideal structure. This process simulation shows the feasibility of proposed device architecture in a CMOS pilot line. (Inset) The 2-D actual doping profiles obtained after an extensive process simulation.

to  $\text{SiO}_2$  permittivity is taken as 3. The electric field calculated from (5) gives  $I_{ON}$  of 1.3 mA/ $\mu\text{m}$  for a  $t_{epi}$  of 2 nm. Both  $I_{ON}$  values are in agreement with the technology computer-aided design (TCAD) simulations. Mobility degradation models are not included in the analytical equations, and hence, the calculated current values are slightly higher than that of the simulated values.

#### IV. CMOS-COMPATIBLE PROCESS FLOW

In Fig. 8(a) and (b), a CMOS-compatible process flow for the STBFET is shown. We have carried out extensive process simulations to look at the feasibility of STBFET device fabrication. Advanced process calibration is carried out with Monte Carlo implantation for the STBFET process simulation [23]. Optimized process parameters of the simulated device are shown in Table II. CVD can be used to achieve abrupt degenerate doping profiles at a higher substrate temperature of 600  $^{\circ}\text{C}$  [13], [14]. During  $P^+$  activation, there is diffusion into the epitaxial region under the high- $k$  spacer, which leads to a slightly increased channel resistance. Fig. 9 shows the transfer characteristics of STBFET obtained after detailed process simulations. A small degradation in ON-current due to boron diffusion in the spacer–channel region is observed. This process shows the feasibility of proposed device architecture in

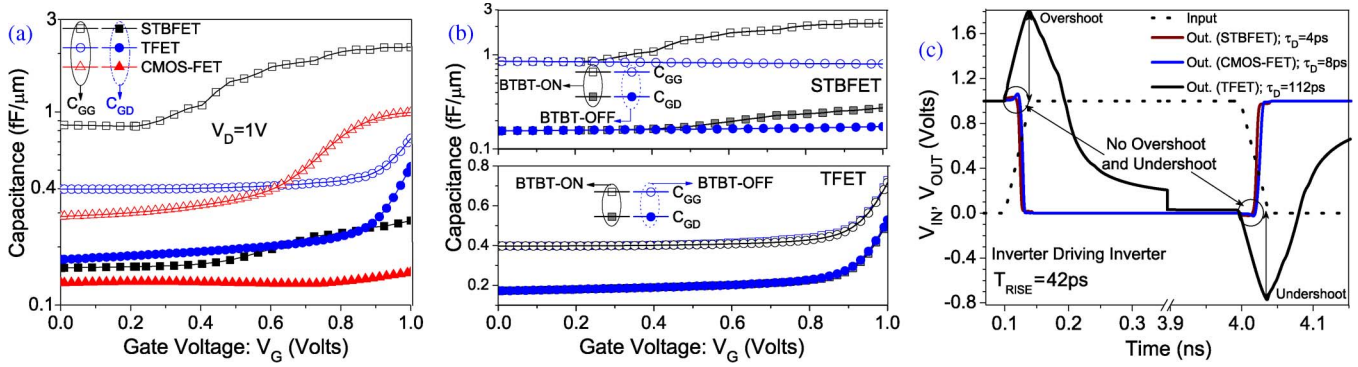


Fig. 10. (a)  $C_{GD}$  is 12% of  $C_{GG}$  for the STBFET, 72% for the TFET, and 15% for the CMOS-FET. The STBFET have the highest  $C_{GG}$  due to high- $k$  spacers but very small  $C_{GD}$ . Hence, the  $C_{GD}$  component in the STBFET is very small, as compared with conventional TFET. (b) In the STBFET, the BTBT model increases  $C_{GD}$  and  $C_{GG}$ , showing that electrons from the valence band of underneath source respond faster to the small signal gate voltage. However, in conventional TFETs, the BTBT model has no effect on the capacitances as carriers from the drain edge respond to the small signal gate voltage. (c) Transient characteristics showing the overshoot phenomenon versus time for the STBFET, TFET, and CMOS-FET inverters. The STBFET and MOSFET inverters show negligible overshoot, whereas the TFET shows a large overshoot of 0.8 V.

a CMOS pilot line. One of the main technology challenges with the realization of the STBFET structure is the growth of the thin undoped epitaxial region over a heavily doped  $P^+$  source with an abrupt doping transition. There are literature reports where such a growth process has been experimentally demonstrated [13], [14]. This is crucial for realization of the high performance of the proposed STBFET structure.

## V. DYNAMIC PERFORMANCE AND DEVICE PARASITICS

The total gate capacitance  $C_{GG}$  and gate-to-drain overlap capacitance  $C_{GD}$  of the three devices (MOSFET, conventional TFET, and STBFET) as a function of gate voltage are shown in Fig. 10(a).  $C_{GD}$  is 72% of  $C_{GG}$  for the TFET, 15% for the MOSFET, and 12% for the STBFET. In the case of a conventional TFET,  $C_{GD}$  is the main contributor of  $C_{GG}$ . However, in the case of STBFET,  $C_{GS}$  is the main component of the  $C_{GG}$ . As shown in Fig. 10(b), in the case of STBFET with the BTBT model turned off,  $C_{GG}$  and  $C_{GD}$  are reduced to their minimum value (given by EOT and high- $k$  spacer), whereas there is no change observed in the case of conventional TFET. This is because in the STBFET, the electrons from the valence band of  $P^+$  source respond faster to the small signal gate voltage. However, in the TFETs, electrons from the conduction band of  $N^+$  drain respond faster to the small signal gate voltage. Transient characteristics showing the overshoot phenomenon versus time for STBFET, TFET, and CMOS-FET inverters are shown in Fig. 10(c). The STBFET and MOSFET inverters show negligible overshoot, whereas the TFET shows a large overshoot of 0.8 V. This is because the STBFET does not suffer from the large Miller capacitance, as is the case with a conventional TFET [24].

In order to further benchmark the STBFET performance in comparison to the conventional TFET and MOSFET technologies, we have performed detailed mixed-mode inverter simulations using Sentaurus. Fig. 11(a) shows the transfer characteristic of the STBFET, conventional TFET, and CMOS-FET-based inverters. The currents in p- and n-channel devices are made equal by increasing the width of the p-channel device. Because of this, the inverter has a switching threshold equal to  $V_{DD}/2$  and a comparable low and high noise margins.

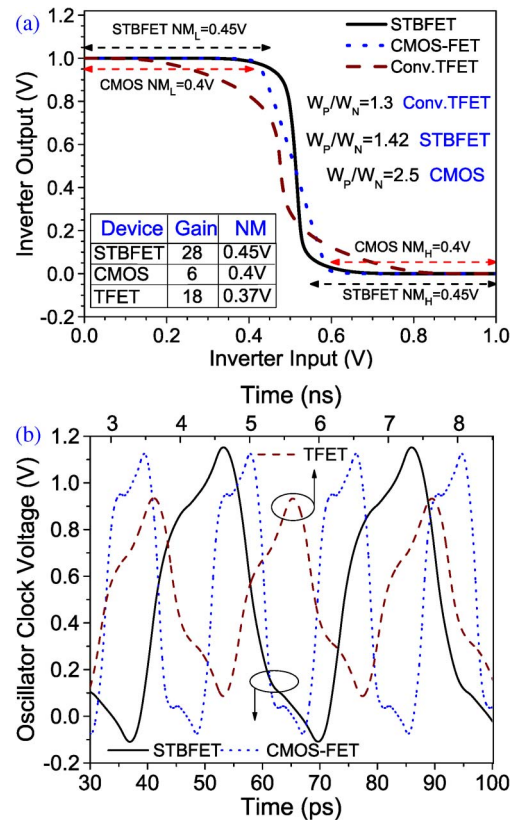


Fig. 11. (a) Voltage transfer characteristic of the STBFET, the CMOS-FET, and the conventional TFET. The STBFET has the highest gain and better noise margin, as compared with the CMOS-FET and the conventional TFET. (b) The TFET ring oscillator has very large time period ( $\sim 2$  ns), compared with the STBFET and the CMOS-FET (20 ps). Furthermore, peak voltages are less than  $V_{DD}$  in case of the TFET.

As the inverter gain depends on the SS of the device, STBFET has the highest gain compared with that of the conventional TFET and the CMOS-FET. Higher inverter gain leads to the better noise margin in the STBFET, as compared with the other two devices. In Fig. 11(b), a three-stage ring oscillator is simulated using the STBFET, the conventional TFET, and a MOSFET. As shown, the STBFET and the MOSFET show a similar dynamic performance. The main reason for the observed



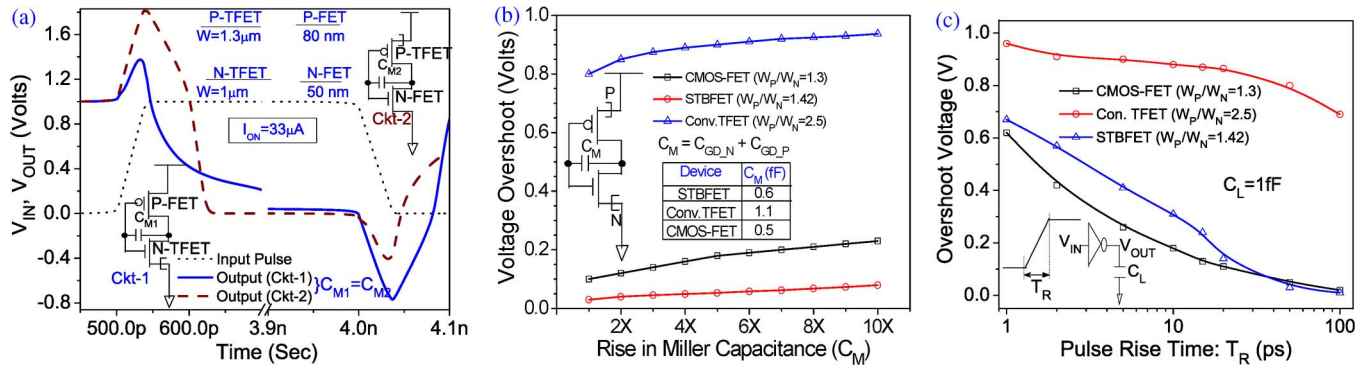


Fig. 12. (a) Result of two different inverter circuit configurations for a conventional TFET. Circuit configuration 1 (pull-up: p-MOSFET; pull-down: n-TFET) have reduced overshoot from 0.8 to 0.37 V. Circuit configuration 2 (pull-up: p-TFET; pull-down: n-MOSFET) have reduced undershoot from  $-0.8$  to  $-0.3$  V. This unbalanced overshoot/undershoot behavior indicates that this is not a node phenomena involving the Miller capacitance. (b) The effect of the Miller capacitance on the overshoot. For  $10\times$  increase in the Miller capacitance, there is less than 0.1 V increase in the overshoot in all the three devices. It shows that the overshoot has a weak dependence on the Miller capacitance. (c) The effect of pulse rise time on the overshoots. The overshoot exponentially falls in the case of the STBFET and the CMOS-FET. However, TFET has significantly higher overshoot even at larger pulse rise time and is due to the large space-charge buildup at the drain junction.

improvement in the dynamic performance can be attributed to the fact that, in the STBFET, the  $P^+$  source is under the gate region within about 2 nm of tunneling distance. This makes the valence band electrons from  $P^+$  source to respond to the small signal gate voltage much faster, compared with the carriers from the  $N^+$  drain.

As shown in the transient characteristics, which is shown in Fig. 10(c), the STBFETs show negligible voltage overshoot, which is commonly observed in tunnel FETs, as reported earlier [21]. This has been attributed to the large Miller capacitance present in the conventional TFETs. To investigate this phenomenon further, transient simulations of two different inverter circuits with a constant Miller capacitance between the input and output nodes are performed. Fig. 12(a) shows the results for a conventional TFET. In circuit configuration 1 (pull-up: p-MOSFET; pull-down: n-TFET), the overshoot has significantly reduced, and the undershoot is unchanged. In circuit configuration 2 (pull-up: p-TFET; pull-down: n-MOSFET), the undershoot has significantly reduced, and the overshoot is unchanged. This unbalanced overshoot/undershoot behavior indicates that this is not a node phenomena involving Miller capacitance. Furthermore, Fig. 12(b) shows that the Miller capacitance is not the major cause of overshoot as for a  $10\times$  increase in the Miller capacitance there is less than a 0.1 V increase in the overshoot for all the three devices. Fig. 12(c) shows the overshoot as a function of input pulse rise time for all the three devices. The overshoot in the case of STBFET and CMOS-FET exponentially drops, but the TFET has a very small reduction in overshoot with increasing pulse rise time.

To further understand the cause of overshoot phenomenon, transient simulations of inverter circuits for the STBFET, the TFET, and the MOSFET are performed. Space-charge contour plots in Fig. 13 show that the overshoot is related to localization of space charge and its time-dependent relaxation. In all the devices (TFETs, MOSFETs, and STBFETs), a large space-charge buildup at the drain junction for a rise time of 1–2 ps is observed. This vanishes in the case of STBFET and MOSFET when the rise time increases to 10 ps. However, for a conventional TFET, space charge remains unchanged even for

a rise time of 100 ps. This proves that overshoot is due to a space-charge buildup and its relaxation instead of the Miller capacitance.

## VI. SUPPLY VOLTAGE SCALING

In order to reduce the dynamic power consumption in CMOS devices, the voltage scaling is absolutely essential. All the three devices, the conventional TFET, the MOSFET, and the STBFET are simulated for a 0.6 V of supply voltage with an EOT of 0.4 nm, and  $L_G = 20$  nm. The static and dynamic performance of STBFET, compared with other devices, is shown in Table III. For 0.6 V of  $V_{DD}$ , the spacer thickness is reduced to 12 nm. This reduces parasitic capacitance and channel resistance. For n-channel STBFET, we have used silicon for all the regions, while for a p-channel device, a SiGe with 50% mole fraction is used for the epilayer. For a reduction in supply voltages, low-band-gap materials are best suited for TFETs. For example, p-STBFET with a 50% Ge mole fraction gives  $I_{ON}$  comparable to that of n-STBFET. The STBFET has a much higher  $I_{ON}$  to  $I_{OFF}$  ratio compared with a MOSFET. For the Dynamic power consumption and delay, a three-stage ring oscillator has been simulated with a 0.6-V supply. For the overshoot, a transient simulation of a single stage inverter with a pulse rise time of 42 ps has been performed. From Table III, it is clear that the STBFET achieved higher  $I_{ON}$ , lower  $I_{OFF}$ , and a comparable dynamic performance as that of the MOSFETs.

## VII. CONCLUSION

In summary, a novel, high-performance silicon TFET has been proposed. The ON-state tunneling distance of this device is defined by the physical thickness of a very thin epilayer. A CMOS-compatible process flow of the STBFET device has been proposed and implemented in a TCAD process simulation. Based on this, the performance of the device has been evaluated and compared with standard MOSFET and TFET devices applying calibrated tunneling models in a numerical device simulation. These calculations indicate high  $I_{ON}$  of STBFET in the range of 0.8 mA/ $\mu\text{m}$  at  $I_{OFF}$  of  $\sim 100$  pA/ $\mu\text{m}$  for  $V_{DS} =$

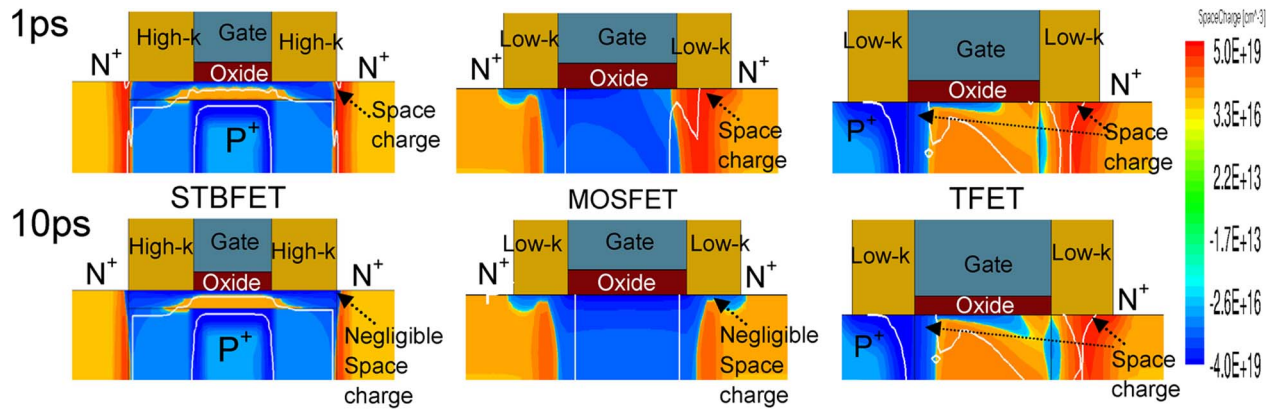


Fig. 13. Space-charge contours of the three devices. All the devices show a large space-charge buildup at the channel–drain junction for 1–2 ps of rise time, which vanishes in the case of the STBFET and the MOSFET when the rise time increases to 10 ps. However, for the conventional TFET, the space charge remains unchanged even for the rise time of 100 ps. This proves that the overshoot is due to the space-charge buildup and its relaxation, instead of the Miller capacitance.

TABLE III  
PERFORMANCE COMPARISON OF THREE DEVICES FOR 0.6 V OF  $V_{DD}$

Device	$I_{ON}$ mA/ $\mu$ m	$I_{OFF}$ nA/ $\mu$ m	$I_{ON}/I_{OFF}$	Dynamic Power( $\mu$ W)	Delay	Overshoot
nMOSFET	0.41	213	1.9e3	14	26ps	NO
pMOSFET	0.26	127	2.0e3			
nSTBFET	0.74	0.2	3.7e6	77	21ps	NO
pSTBFET	0.81	2.2	3.5e5			
nTFET	4.23e-3	1e-3	4.2e6	0.25	14ns	0.56V
pTFET	1.05e-3	1e-3	1.0e6			

$V_{GS} = 0.6$  V. For  $V_{DS} = V_{GS} = 1$  V,  $I_{ON}$  is 1.4 mA/ $\mu$ m at  $I_{OFF}$  of  $\sim 0.1$  pA/ $\mu$ m. Smaller  $I_{OFF}$  is due to thicker spacer in case of 1-V operation. The STBFET, as a result, have much higher  $I_{ON}$ -to- $I_{OFF}$  ratio compared with the MOSFETs. The improvement of  $I_{ON}$  is also analytically validated in this paper. Due to the specific device topology employed in STBFET, the device shows several distinct advantages. The tunneling current in this device scales with the gate area, instead of gate width leading to high  $I_{ON}$ .  $I_{OFF}$ , is essentially dependent on spacer thickness and is very low. The proposed device also shows an excellent output current saturation and overcomes the voltage overshoot of switching inverter stages due to the elimination of space-charge regions at the channel to drain interface. High gain and good noise margin of inverter chains have been shown from the simulations.

Together, these results make the STBFET a very promising device candidate for high-performance systems operating at voltages below 1 V.

## REFERENCES

- [1] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong, "Vertical silicon-nanowire formation and gate-all-around MOSFET," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 791–794, Jul. 2008.
- [2] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C. Y. Yang, C. Tabery, C. Ho, Q. Xiang, T. J. King, J. Bokor, C. Hu, M. R. Lin, and D. Kyser, "FinFET scaling to 10 nm gate length," in *IEDM Tech. Dig.*, 2002, pp. 251–254.
- [3] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than  $kT/q$ ," in *IEDM Tech. Dig.*, 2002, pp. 289–292.
- [4] K. E. Moselund, H. Ghoneim, M. T. Bjork, H. Schmid, S. Karg, E. Lortscher, W. Riess, and H. Riel, "Comparison of VLS grown Si NW tunnel FETs with different gate stacks," in *Proc. Eur. Solid State Device Res. Conf.*, Sep. 2009, pp. 448–451.
- [5] E. M. Buturla, J. B. Johnson, S. S. Furkay, and P. Cottrell, "A New 3D device simulation formulation," in *Proc. 6th Int. Conf. NASCODE*, Dublin, Ireland, 1989, pp. 291–296.
- [6] R. K. Pandey, K. V. R. M. Murali, S. S. Furkay, P. J. Oldiges, and E. J. Nowak, "Crystallographic-orientation-dependent gate-induced drain leakage in nanoscale MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2098–2105, Sep. 2010.
- [7] A. Appaswamy, M. Bajaj, R. Pandey, S. Furkay, and K. Murali, "A modified local density approximation based channel quantization model for nanoscale MOSFETs," in *Proc. 15th Int. Workshop Phys. Semicond. Devices*, 2009, pp. 759–762.
- [8] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high- $\kappa$  gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.
- [9] K. Bhuwarka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering," *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 909–917, May 2005.
- [10] N. Patel, A. Ramesha, and S. Mahapatra, "Drive current boosting of n-type tunnel FET with strained SiGe layer at source," *Microelectron. J.*, vol. 39, no. 12, pp. 1671–1677, Dec. 2008.
- [11] A. Pal, A. B. Sachid, H. Gossner, and V. R. Rao, "Insights into the design and optimization of tunnel-FET devices and circuits," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 1045–1053, Apr. 2011.
- [12] S. Rommel, T. Dillon, P. Berger, P. Thompson, K. Hobart, R. Lake, and A. C. Seabaugh, "Epitaxially grown Si resonant interband tunnel diodes exhibiting high current densities," *IEEE Electron Device Lett.*, vol. 20, no. 7, pp. 329–331, Jul. 1999.
- [13] S. Y. Park, R. Anisha, P. R. Berger, R. Loo, N. D. Nguyen, S. Takeuchi, and M. Caymax, "Si/SiGe resonant interband tunneling diodes incorporating  $\delta$ -doping layers grown by chemical vapor deposition," *Electron Device Lett.*, vol. 30, no. 11, pp. 1173–1175, Nov. 2009.
- [14] N. Jin, R. Yu, S. Y. Chung, P. R. Berger, and P. E. Thompson, "Strain engineered Si/SiGe resonant interband tunneling diodes with outside barriers grown on  $\text{Si}_{0.8}\text{Ge}_{0.2}$  virtual substrates," *Electron Device Lett.*, vol. 29, no. 6, pp. 599–602, Jun. 2008.
- [15] G. Hurkx, H. de Graaff, W. Kloosterman, and M. Knuvers, "A new analytical diode model including tunneling and avalanche breakdown," *IEEE Trans. Electron Devices*, vol. 39, no. 9, pp. 2090–2098, Sep. 1992.
- [16] T. Fukaya, R. Yamada, Y. Tanaka, S. Matsumoto, T. Suzuki, G. Fuse, T. Kudo, and S. Sakuragi, "Effect of low temperature annealing prior to non-melt laser annealing in ultra-shallow junction formation," in *Proc. 15th Int. Conf. Adv. Thermal Process. Semicond.*, Oct. 2007, pp. 317–320.
- [17] A. B. Sachid, C. R. Manoj, D. K. Sharma, and V. R. Rao, "Gate fringe-induced barrier lowering in underlap FinFET structures and its optimization," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 128–130, Jan. 2008.
- [18] K. Boucart and A. M. Ionescu, "Threshold voltage in tunnel FETs: Physical definition, extraction, scaling and impact on IC design," in *Proc. 37th ESSDERC*, Sep. 2007, pp. 299–302.
- [19] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. New York: Cambridge Univ. Press, 2009.
- [20] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 297–300, Apr. 2006.



- [21] P. M. Solomon, J. Jopling, D. Frank, C. D'Emic, O. Dokumac, P. Ronsheim, and W. Haensch, "Universal tunneling behavior in technologically relevant P/N junction diodes," *J. Appl. Phys.*, vol. 95, no. 10, pp. 5800–5812, May 2004.
- [22] J. Wang, A. Rahman, A. Ghosh, G. Klimeck, and M. Lundstrom, "On the validity of the parabolic effective-mass approximation for the IV calculation of silicon nanowire transistors," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1589–1595, Jul. 2005.
- [23] S. Tian, "Predictive Monte Carlo ion implantation simulator from sub-eV to above 10 MeV," *J. Appl. Phys.*, vol. 93, no. 10, pp. 5893–5904, May 2003.
- [24] S. Mookerjee, R. Krishnan, S. Datta, and V. Narayanan, "Effective capacitance and drive current for tunnel FET (TFET) CV/I estimation," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 2092–2098, Sep. 2009.



**Ram Asra** was born in Uttar Pradesh, India, in 1980. He received the M.S. degree in electronic science with very large scale integration specialization from Kurukshetra University, Kurukshetra, India, in 2003. He is currently working toward the Ph.D. degree in the Center for Excellence in Nanoelectronics, Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai, India.

He worked on fabrication of microelectromechanical-systems-based pressure sensors for *in vivo* applications from 2004 to 2006. His current

research interests include steep subthreshold complementary metal-oxide-semiconductor devices for sub-1-V operations at extremely small gate lengths. He is the holder of two patent applications.



**Mayank Shrivastava** (S'09–M'10) was born in Lucknow, India, in 1984. He received the B.S. degree in engineering from Rajiv Gandhi Technological University, Bhopal, India, in 2006 and the Ph.D. degree from the Indian Institute of Technology (IIT) Bombay, Mumbai, India, in 2010.

From April 2008 to October 2008 and May 2010 to July 2010, he was a Visiting Research Scholar with Infineon Technologies AG, Munich, Germany. He worked for Infineon Technologies, East Fishkill, NY, from 2010 to 2011. He is currently with Intel Mobile

Communications, Hopewell Junction, NY, as a Senior Electrostatic Discharge (ESD) Engineer for International Semiconductor Development Alliance. He is the holder of eight patent applications and has published more than 25 papers in international conferences/journals in the field of ESD, input-output (I/O) devices, fin-shaped field-effect transistors (FinFETs), and nonvolatile memory. His current research interests include ESD- and hot-carrier-degradation-aware I/O device design, ESD-aware technology development, FinFET, and ultrathin-body planar silicon-on-insulator devices, nonvolatile analog memory, electrothermal modeling, and simulation.

Dr. Shrivastava served as a Reviewer for the IEEE TRANSACTIONS ON ELECTRON DEVICES, *IEEE Electron Device Letters*, and the *Journal of Microelectronics Reliability*. He was the recipient of Intel's AAF-2008 Best Research Paper Award in circuit design category, the Industrial Impact Award from IIT Bombay in 2010, Biography publication by the International Biographical Center, Cambridge, U.K., in the 2000 Outstanding Intellectuals of the 21st Century in 2010, an award for his Ph.D. thesis from IIT Bombay named Excellence in Thesis Work in the year 2010, and the TR35-2010 Young Innovator Award.



**Kota V. R. M. Murali** received the M.S. and Ph.D. degrees from Massachusetts Institute of Technology, Cambridge.

He is the Lead Scientist and Senior Manager of Nanodevice Modeling Group at IBM Semiconductor Research and Development Center, Bangalore, India. He has been a Visitor in IBM Watson and Almaden Research Centers and is also an Adjunct Faculty Member at the Indian Institute of Technology Bombay, Mumbai, India. His research interests are in the areas of nanoscale materials and devices

for electronics, spin and superconducting-based quantum devices, and energy technologies.



**Rajan K. Pandey** received the M.Sc. degree physics degree from Banaras Hindu University, Varanasi, India, in 1998 and the Ph.D. degree from the Indian Institute of Technology Kanpur, Kanpur, India, in 2006, working on electronic structure of semiconductor quantum dots.

After a postdoctoral research from University of California, Irvine, he worked with Motorola Laboratories, Bangalore, India. In 2008, he joined IBM India Semiconductor Research and Development Center, Bangalore, India, where he is working on multiscale modeling of next-generation complementary metal-oxide-semiconductor devices.



**Harald Gossner** (M'06) received the Dipl. Phys. degree in physics from Ludwig Maximilian University, Munich, Germany, in 1990 and the Ph.D. degree in electrical engineering from the Universität der Bundeswehr, Munich, in 1995.

For 15 years he has been working on the development of electrostatic discharge (ESD) protection concepts for bipolar, bipolar complementary metal-oxide-semiconductor (CMOS), and CMOS technologies with Siemens and Infineon Technologies. Recently, he has joined Intel Mobile Commu-

nications as a Senior Principal Engineer with Intel Mobile Communications, Hopewell Junction, NY, overseeing the development of robust mobile systems. He has authored and coauthored more than 80 technical papers and one book in the field of ESD and device physics. He is the holder of 30 patents on the topics mentioned.

Dr. Gossner has served in the technical program committees of IEEE International Electron Devices Meeting, the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium, and the International ESD Workshop. He is currently the Cochair of the Industry Council on ESD Target Levels. He was the recipient of the best paper award from the EOS/ESD Symposium in 2005.



**V. Ramgopal Rao** (M'98–SM'02) received the M.Tech. degree from the Indian Institute of Technology (IIT) Bombay, Mumbai, India, in 1991 and the Dr. Ing. degree from the Universität der Bundeswehr, Munich, Germany, in 1997.

From 1997 to 1998 and again in 2001, he was a Visiting Scholar with the Department of Electrical Engineering, University of California at Los Angeles, Los Angeles. He is currently an Institute Chair Professor with the Department of Electrical Engineering and the Chief Investigator for the

Center of Excellence in Nanoelectronics, IIT Bombay. He has over 280 publications in the area of electron devices nanoelectronics in refereed international journals and conference proceedings and has 15 patents issued or pending.

Dr. Rao is a Fellow of the Indian National Academy of Engineering, the Indian Academy of Sciences, and the National Academy of Sciences in India. He is a Distinguished Lecturer of the IEEE Electron Devices Society and has served on the program/organizing committees of a large number of international conferences in the area of electron devices. He was the Chairman of the IEEE Applied Physics/Electron Device Bombay Chapter from 2002 to 2003 and currently serves on the executive committee of the IEEE Bombay Section, aside from being the Vice-Chair of the IEEE Asia-Pacific Regions/Chapters Subcommittee. He is an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES in the complementary metal-oxide-semiconductor devices and technology area and serves on the Editorial Boards of various other international journals. He was the recipient of the coveted Shanti Swarup Bhatnagar Prize in Engineering Sciences awarded by the Honorable Prime Minister of the Government of India, in 2005 for his work on electron devices. He is also a recipient of the 2004 Swarnajayanti Fellowship Award from the Department of Science Technology, the 2007 IBM Faculty Award, the 2008 Materials Research Society of India Annual Prize, and the 2009 TechnoMentor Award from the Indian Semiconductor Association.