A Drain-Extended MOS Device With Spreading Filament Under ESD Stress

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***Abstract*—Based on 3-D TCAD simulations, a ten-times improvement in the ESD performance of drain-extended NMOS device is predicted by incorporating deep p-implant underneath the n^+ drain region. The proposed modification does not degrade the intrinsic MOS characteristics, thus enabling a self-protection ESD concept. Moreover, a detailed physical insight toward the achieved improvement is given.**

***Index Terms*—Drain-extended MOS (DeMOS), ESD, LDMOS, moving filament, spreading filament.**

I. Introduction

In ORDER to protect input/output (I/O) cells from ESD events, either one needs to add ESD protection devices with these cells or the I/O cell itself can be designed with an ESD robust (or self-protected) device. The later approach is preferred since it costs very less additional parasitic and silicon area. Drain-extended MOS (DeMOS) devices provide the required performance and reliability robustness for high-voltage (HV) mixed-signal applications in advanced CMOS technologies. However, they commonly suffer from early failures under ESD like stress conditions due to filament formation and nonuniform current distribution [1]–[3]. This can be a major roadblock for their application in system-on-chip designs. In order to make DeMOS devices self-protected, there have been two proposals made by researchers. The first is embedded SCR with DeMOS, which was proved to significantly improve the ESD robustness of DeMOS device without sacrificing its intrinsic behavior [4]. However, this approach has serious latch-up concerns. The second approach is to achieve moving current filaments beyond the onset of instability [5], [6]. However, this approach is hard to realize due to nontrivial device design parameters.

Keeping the ESD requirements for DeMOS devices in mind, we propose a new self-protected DeMOS device in this letter. The proposed device is a standard drain-extended NMOS (DeNMOS) device [Fig. 1(a)] along with a deep p-implant underneath the n^+ drain diffusion region [Fig. 1(b)]. Such a deep p-implant can be incorporated, for example, by using an ESD implant, which is regularly used in CMOS technologies in order to enhance ESD performance of NMOS devices [7]. The doping level of the so-called ESD-implant is lower than the one of the drain diffusion and higher than that of the well region.

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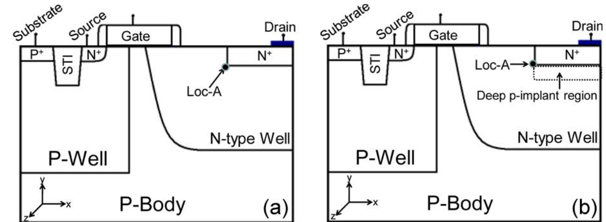

Fig. 1. Devices under study. (a) Standard DeNMOS device, i.e., without p-implant. (b) Proposed DeNMOS device, i.e., with deep p-implant, under the n^+ drain region. Any out diffusion of deep p-region toward the left of n^+ drain must be avoided as it degrades the MOS behavior.

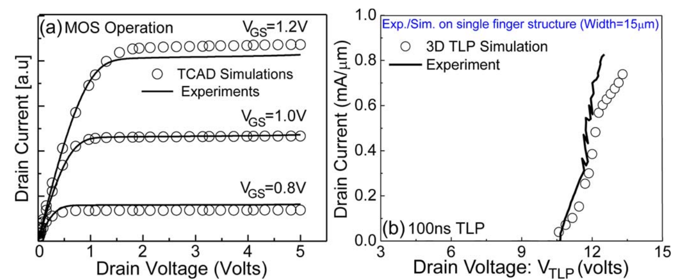

Fig. 2. Calibration of mobility, avalanche, and electrothermal model parameters (including thermal boundary conditions) for a STI-type DeMOS device [1], [2]. (a) Calibration of mobility models, including quantum corrections for MOS operation, and (b) calibration of avalanche generation and high field velocity saturation models and thermal boundary conditions for HV high-current operation.

Based on 3-D TCAD simulations, a more than ten-times improvement in the ESD performance is predicted, without affecting the intrinsic MOS performance.

II. Simulation Framework and Results

A well-calibrated process and device simulation deck is used for the 3-D TCAD simulations, as used in our previous works on STI-type DeMOS device [1], [2]. Mobility, high field velocity saturation, and avalanche generation models were calibrated for MOS operating biases [Fig. 2(a)] as well as for HV high-current operations [Fig. 2(b)]. Thermal boundary conditions in the Z-direction were set to simulate full structure. Predictive capability of filamentary behavior using a well-calibrated 3-D TCAD setup is well proven and has been demonstrated in our recent works [1], [2].

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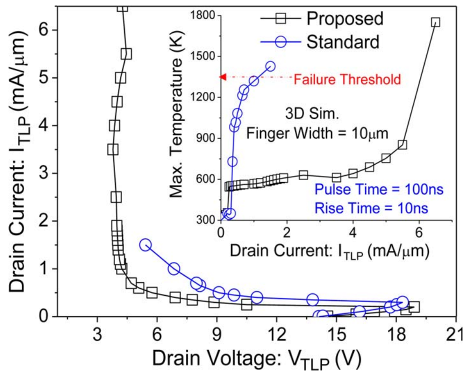

Fig. 3. TLP characteristics and maximum lattice temperature of both the devices extracted from 3-D TCAD simulations under grounded gate, source, and substrate connection.

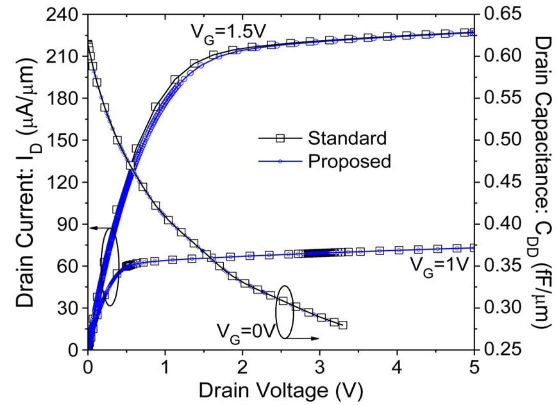

Fig. 5. Comparison of intrinsic characteristics ($I_D - V_D$ and drain capacitance) of the standard and proposed DeNMOS devices.

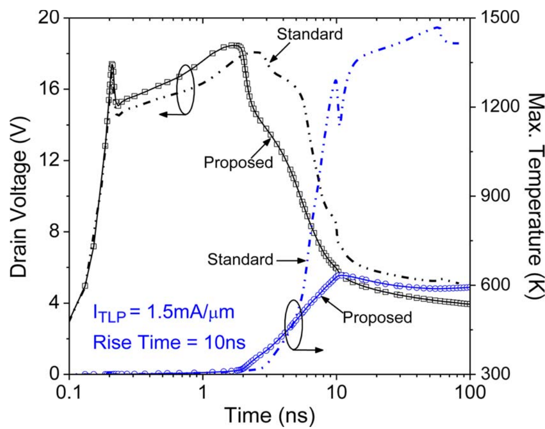

Fig. 4. Transient voltage waveform and maximum lattice temperature across the device evolution over time for both the devices extracted from 3-D TCAD simulations.

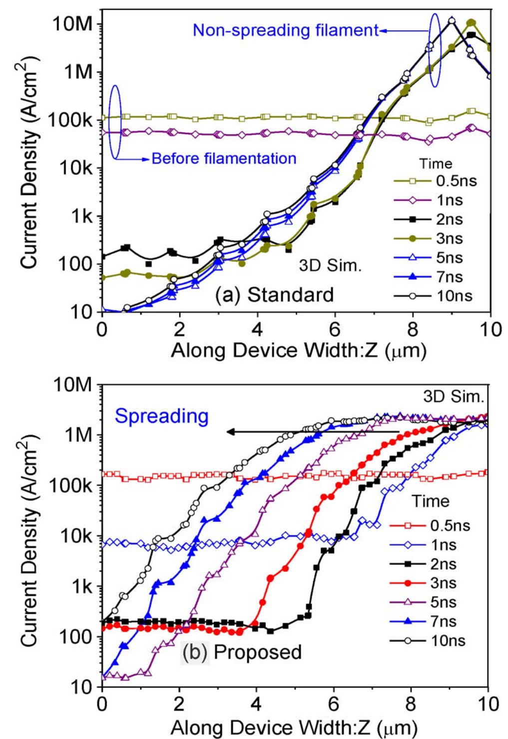

Fig. 6. Current density distribution (at Loc-A) w.r.t. time along the width of the devices. (a) Standard. (b) Proposed.

A. TLP Characteristics and $It2$ Improvement

Fig. 3 shows that the standard DeNMOS device fails below 0.5 mA/μm; however, the proposed device survives TLP currents above 5 mA/μm (i.e., approximately ten-times improvements). This is attributed to significantly lower lattice heating after instability or filament formation in the proposed device, as evident from the inset of Fig. 3.

Note that the additional p-region under drain n^+ does not lead to any change in the well breakdown voltage. Fig. 4 shows that the standard device leads to significant temperature rise within 5–10 ns, which is due to filament formation [3]; however, the proposed device does not lead to excess temperature rise right after current filamentation.

B. Intrinsic MOS Behavior

Since the additional p-implant does not lie in the path of MOS conduction and does not influence the carrier drift in the drain extension, the proposed modification does not degrade the intrinsic MOS characteristics (i.e., I_{ON}, on-resistance, breakdown voltage, parasitic drain capacitance, etc.) of the device, as shown in Fig. 5.

C. Insight Toward $It2$ Improvement

Figs. 6 and 7 show that the standard device has a dense filament formation after space charge modulation, which eventually gets stuck at the corner [Fig. 6(a)] and leads to a temperature rise within a few nanoseconds [Fig. 7(a)]. However, the proposed device leads to the formation of a relaxed current filament, which gradually spreads with time over the whole device width [Fig. 6(b)]. This attributes to a relaxed temperature rise [Fig. 7(b)] even at very high TLP currents, which eventually leads to very high $It2$ value.

Fig. 8(a) explains that there were no differences in the parasitic bipolar triggering mechanism between the standard and proposed devices. However, the device with deep p-implant

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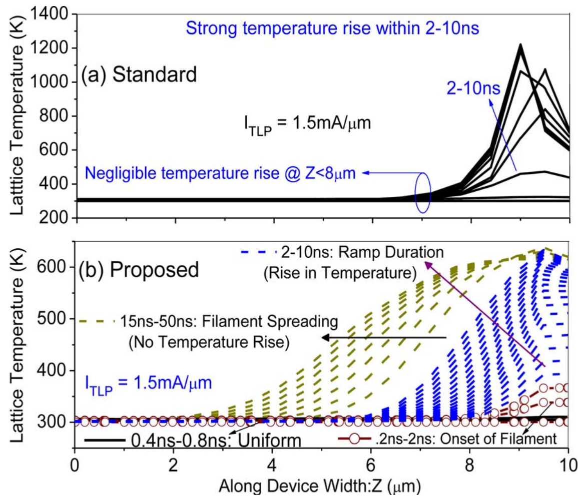

Fig. 7. Temperature distribution (at Loc-A) along the width and its evolution-over-time increments for the device. (a) Standard. (b) Proposed.

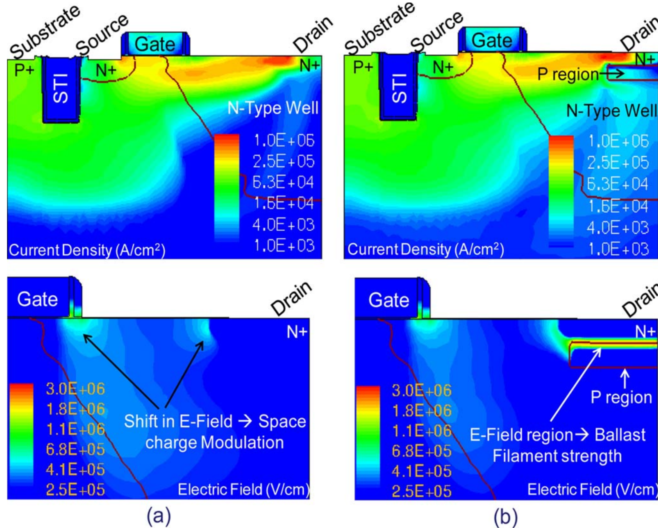

Fig. 8. Current and electric field distribution in the DeNMOS device. (a) Standard. (b) Proposed.

forms an additional metallurgical p-n junction underneath the n^+ drain diffusion. The additional electric field built underneath the drain diffusion [Fig. 8(b)] 1) plays a key role in relaxing (reducing) the strength (density) of current filament during the onset of charge modulation and 2) allows the device to generate impact ionization carriers across the whole width. Formation of an initially widened current filament (Fig. 7) mitigates the lattice heating right after instability, and impact-ionization-generated carriers across the whole width allow the device to further spread the current filament.

Filament spreading is driven by lower impact ionization inside the filament (hotter region) compared to region outside the filament (cooler region). Note that filament spreading can only happen when the rate of lattice heating during current instability is less compared to the rate at which filament spreads. Lower rate of lattice heating was achieved by widening of current filament, as discussed previously.

Furthermore, Fig. 9 validates that the electrothermal effects lead to filament spreading along the full device width. When

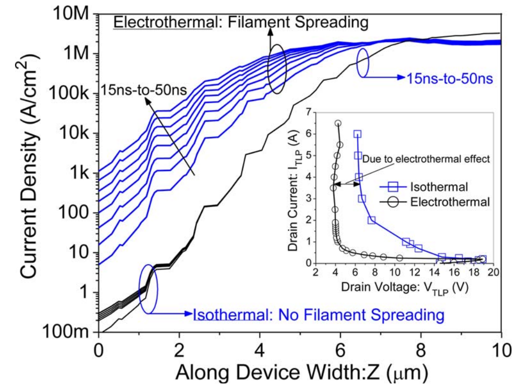

Fig. 9. Differences between the current distributions (along the device width and its evolutions over time) extracted from electrothermal and isothermal TCAD simulations at Loc-A.

isothermal simulations were performed, the device exhibits a relaxed filament formation; however, the filament does not spread across the complete device width and remains stuck at one corner. On the other hand, the same filament spreads across the width of the device when an electrothermal simulation (drift diffusion transport simulation including lattice heating) was performed.

III. Conclusion

In this letter, we have proposed to incorporate ESD p-implant in DeNMOS device. Using detailed 3-D TCAD simulations, we have demonstrated more than ten-times improvement in ESD performance without giving up on the intrinsic MOS characteristics of the drain-extended device. We found that deep p-implant under the drain n^+ region promotes current filament spreading and relaxes the temperature rise right after the formation of such a filament in the DeNMOS device, which eventually survives the usual catastrophic snapback and filamentation.

References

[1] M. Shrivastava, C. Russ, H. Gossner, S. Bychikhin, D. Pogany, and E. Gornik, "ESD robust DeMOS devices in advanced CMOS technologies," in *Proc. EOS/ESD Symp.*, 2011, pp. 1–10.

[2] M. Shrivastava, S. Bychikhin, D. Pogany, J. Schneider, M. S. Baghini, H. Gossner, E. Gornik, and V. R. Rao, "Filament study of STI type drain extended NMOS device using transient interferometric mapping," in *Proc. IEEE Int. Electron Device Meeting*, 2009, pp. 417–420.

[3] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, and V. Ramgopal Rao, "On the failure mechanism and current instabilities in RESURF type DeNMOS device under ESD conditions," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2009, pp. 841–845.

[4] C. Duvvury, J. Rodriguez, C. Jones, and M. Smayling, "Device integration for ESD robustness of high voltage power MOSFETs," in *IEDM Tech. Dig*, 1994, pp. 407–410.

[5] R. M. Steinhoff, J.-B. Huang, P. L. Hower, and J. S. Brodsky, "Current filament movement and silicon melting in an ESD-robust DENMOS transistor," in *Proc. EOS/ESD Symp.*, 2003, pp. 1–10.

[6] M. Denison, M. Blaho, P. Rodin, V. Dubec, D. Pogany, D. Silber, E. Gornik, and M. Stecher, "Moving current filaments in integrated DMOS transistors under short-duration current stress," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1695–1703, Oct. 2004.

[7] K. Chatty, D. Alvarez, R. Gauthier, C. Russ, M. Abou-Khalil, and B. J. Kwon, "Process and design optimization of a protection scheme based on NMOSFETs with ESD implant in 65 nm and 45 nm CMOS technologies," in *Proc. EOS/ESD Symp.*, 2007, pp. 7A.2.1–7A.2.10.

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