# Device–Circuit Co-design for Beyond 1 GHz 5 V Level Shifter Using DeMOS Transistors

Peeyusha Saurabha Swain, Mayank Shrivastava, *Member, IEEE*, Harald Gossner, *Senior Member, IEEE*, and Maryam Shojaei Baghini, *Senior Member, IEEE*

***Abstract*— This paper presents a device–circuit co-design approach to achieve a low swing, high speed 1.2–5 V level shifter (LS) using drain extended MOS (DeMOS) transistors for system on chip applications in advance CMOS technologies. Limiting factors of the high-voltage devices during transients are identified and accordingly it is shown that the maximum operating frequency of traditional LS can be increased by at least a factor of two. It is demonstrated that optimization of key device parameters of the DeMOS transistor enhances the maximum clock frequency to more than 1 GHz while preserving the device breakdown voltage and duty cycle of the level shifted signal.**

***Index Terms*— Device–circuit co-design, level shifter (LS), overlap region, shallow trench isolation drain extended MOS (STI-DeMOS).**

## I. Introduction

HIGH-VOLTAGE devices such as laterally diffused MOS or drain extended MOS (DeMOS) are used for many applications in microelectrical mechanical systems, automotive and telecommunication systems, display drivers, and interfacing circuits. Growing popularity of system on chip demands reliable high-voltage (HV) devices at input–output (I/O) interfaces. The conventional MOS transistors are not suitable for HV I/O due to low breakdown voltage of core devices. Shallow trench isolation DeMOS (STI-DeMOS) transistors take advantage of both high breakdown voltage and compatibility with low voltage CMOS process [1]. Optimized construction and drain topology of these devices allow device design using thin oxide with high performance concerning breakdown voltage, parasitic resistance, and capacitances [2].

In this paper, we show how layout parameters and doping profile of DeMOS transistors are optimized for the use in HV level shifters (LSs). Maximum $I_{ON}$ does not automatically lead to the best performance of LS. Device and circuit need to be co-optimized for a high speed, HV LS, e.g., for controlling integrated high-speed power amplifiers.

This paper is organized as follows. Section II reviews state-of-the-art LS circuits followed by technology computer-aided design (TCAD) simulation methodology. Section III investigates the STI-DeMOS transistors. Section IV presents a detailed study of the behavior of the LS circuit. Device–circuit co-design and discussions are given in Sections V and VI, respectively. Section VII provides the conclusion.

Manuscript received May 11, 2013; accepted September 18, 2013. Date of current version October 18, 2013. The review of this paper was arranged by Editor M. Darwish.

P. S. Swain and M. S. Baghini are with the Department of Electrical Engineering, IIT Bombay, Mumbai 400076, India (e-mail: peeyushs@ee.iitb.ac.in; mshojaei@ee.iitb.ac.in).

M. Shrivastava was with the Intel Corporation Mobile and Communications Group, Munich 80336, Germany. He is now with the Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore 560012, India (e-mail: mayank@dese.iisc.ernet.in).

H. Gossner is with the Intel Corporation Mobile and Communications Group, Munich 80336, Germany (e-mail: harald.gossner@intel.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2013.2283421

## II. Test Vehicle and Methodology

### A. High Voltage LSs

According to various LSs reported in the literature for digital outputs, we classify them into five categories. Table I compares these LS architectures. There are a few LSs, which use mixture of architectures. For example a 1-GHz LS using both stacked and capacitor coupling concepts has been reported in [3]. However, the circuit is complex and also has disadvantages listed in Table I.

We have selected, redesigned, and resimulated two common HV LS architectures reported in [4] and [5]. These two LSs are shown in Fig. 1. We classify them as multiple stacked and single-stack De-n-MOS-De-p-MOS (SSDeNP) LSs, respectively. We have migrated the designs from 350 to 65-nm CMOS technology having low and high supply voltages of 1.2 V ($V_{ddL}$) and 5 V ($V_{ddH}$), respectively. Multiple stacked LS do not need HV transistors except for the devices used in the output driver. However, SSDeNP LS is preferred due to its simplicity, low number of transistors, and no requirement of extra bias voltages. For our simulation, which is calibrated with 65-nm parameters, we use two thick oxide inverter stacks for reliable operation at 5.0 V supply [Fig. 1(a)]. Multiple stacked LS needs extra bias voltages for the stacked inverters in addition to the large area requirement of triple well n-MOS transistors. This situation is further aggravated if $V_{ddH}$ increases. On the other hand, SSDeNP LS [Fig. 1(b)] well adapts to any $V_{ddH}$ provided $V_{ssH}$ is kept at $V_{ddH}-V_{ddL}$.

Basic structure of SSDeNP LS [Fig. 1(b)] has been reported by Moghe but in 0.35-$\mu$m technology [5]. In this paper, swing from $V_{ssH}-V_{ddH}$ is only 1.2 V. So, output of the LS does not toggle if high $V_{th}$ transistors are used (Table II). Therefore, we replace P1, P2, P5, and P6 [Fig. 1(b)] with low $V_{th}$ transistors.

In this paper, we show how device–circuit co-design of the SSDeNP LS leads to a significant improvement in the speed, symmetry, and voltage shift at a reasonable power dissipation.

TABLE I
CLASSIFICATION OF LSs

| Type | Operation | Shortcomings | Reference |
|---|---|---|---|
| Level shifter with active load | Mirror circuit controls the gate bias of the output buffer. | Complex architectures and process variation sensitive. | [6], [7], [8] |
| Capacitive coupled level shifter | Bootstrapping capacitor shifts the input signal level to control the gate of the output buffer. | High area requirement and coupled noise from input to the buffer transistors. | [9], [10], [11] |
| Diode stacked level shifter | A stack of diodes provides biasing voltages to the transistors which directly or indirectly control the output buffer. | High static power consumption and critical in design. | [12], [13] |
| Multiple transistor stacked level shifter | A stack of transistors pass the signal from input to the gate of pull-up PMOS transistors in the output buffer. | Area and no of bias voltages are proportional to the $V_{ddH}$ level. | [4] |
| Single De-n-MOS and De-p-MOS transistor stacked level shifter | A single stack of De-n-MOS and De-p-MOS transistors pass the signal from input to the gate of pull-up PMOS transistors in the output buffer. | High speed single-stack De-n-MOS-De-p-MOS level shifter is not reported in [5]. | [5] |

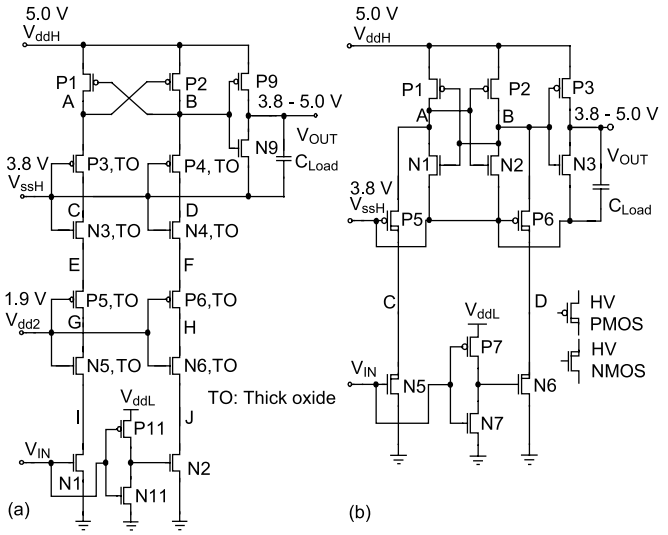


Fig. 1. LS architectures. (a) Multiple stacked type and (b) single-stack De-n-MOS-De-p-MOS (SSDeNP) type.

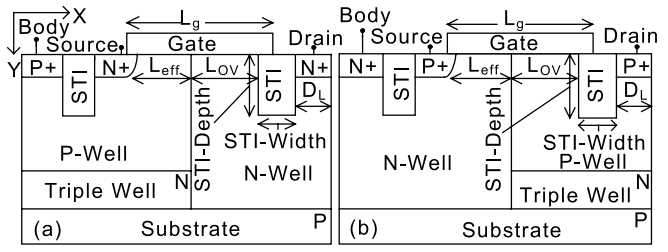


Fig. 2. (a) STI-De-n-MOS device. (b) STI-De-p-MOS device.

### B. TCAD Methodology

Fig. 2 shows the structure of STI-De-n-MOS and STI-De-p-MOS transistors. Due to the STI region, the field near the drain and gate to drain capacitance reduce but ON resistance increases as $I_{ON}$ has to travel around it [2]. The STI DeMOS has higher packing density than LDDMOS and is more reliable than non-STI DeMOS, as explained in [2].

TABLE II
COMPARISON OF TWO DIFFERENT LS PERFORMANCES (WITH 1.2 V OF BOTH INPUT AND OUTPUT SWING AND LOAD CAPACITANCE IS 200 fF) (TCAD SIMULATION)

| Performance parameters | LS of Fig. 1.a | LS of Fig. 1.b with high $V_{th}$ transistors | LS of Fig. 1.b with low $V_{th}$ transistors |
|---|---|---|---|
| Average delay (ps) | 771 | Didn't toggle even with lower load capacitance | 640 |
| Duty cycle (%) | 48.5 | | 49.2 |
| Rise to fall time ratio | 1.0 | | 0.94 |
| Max. clk freq.y (MHz) | 300 | | 650 |

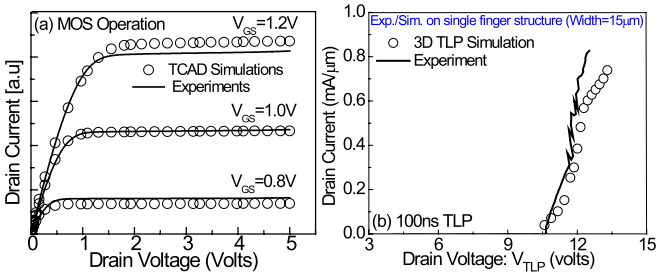


Fig. 3. Calibration of models used in TCAD simulations for STI type DeMOS devices [14], [15]. (a) Calibration of mobility models including quantum corrections and (b) calibration of avalanche generation and high field velocity saturation models for HV operation. Reprinted from [16].

In this paper, we use mixed mode TCAD simulation using a well-calibrated process and device simulation deck, deployed in the previous work from our group on STI-DeMOS device [14], [15]. TCAD models are calibrated with the experimental data, as shown in Fig. 3, justifying the model used.

## III. PRELIMINARY INVESTIGATION ON STI-DeMOS DEVICE

We perform a device level optimization for STI-De-n-MOS and STI-De-p-MOS transistors for various device layout parameters. These transistors sustain $V_{DS}$ and $V_{GD}$ levels up

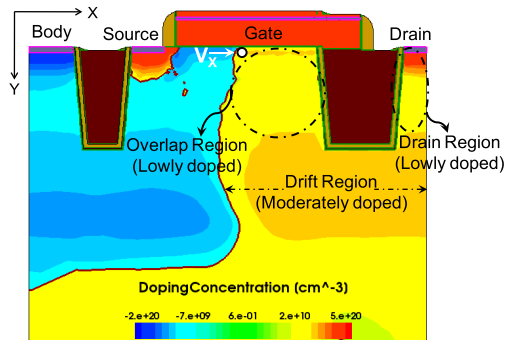


Fig. 4. STI-De-n-MOS device drift region doping profile. $V_X$ is the actual drain-to-source voltage of intrinsic MOS device (TCAD simulation).

to 10 V. As shown in Fig. 4, drift region of the DeMOS transistor has two low-doped regions (in the overlap and drain regions) due to retrograde doping profile of the well. These regions form local junctions with the adjacent moderately doped region [17]. According to the bias, these junctions accumulate or deplete mobile charges. Thus, a high electric field is created, which leads to a considerable potential drop in these regions and hence absolute value of the inner drain potential ($V_X$) is reduced. $V_X$ defines the $I_{\rm ON}$ and operating region of the device.

Except overlap and drain region other part of drift region is moderately doped ($\sim 10^{18}$ cm$^{-3}$). Potential drop in this moderately doped region is much less as compared with overlap and drain regions due to its lower resistance. Potential drop in other regions depends on the difference in doping levels, applied bias, and their width, as shown in Fig. 5.

In this paper, we vary layout parameters such as effective gate length ($L_{\rm eff}$), gate-well overlap length ($L_{\rm OV}$), and STI width (Fig. 2), and observe the impact on the circuit performance. Width of the transistor is a layout parameter, which is decided based on the current drive.

In Fig. 6, we show the parasitic capacitances in the drift region. $C_3$ is the main component of gate to drain overlap capacitance $C_{\rm gd}$. In case of STI-De-p-MOS [Fig. 6(b)], $C_{\rm db}$ comprises of capacitances $C_4$, $C_5$, and $C_6$. $C_4$ is an L-shaped capacitance due to the overlap region. $C_5$ and $C_6$ are due to the region below the STI and drain extension regions. These two regions are usually at higher reverse bias potential as compared with the overlap region. So, individual contribution of $C_5$, $C_6$, and $C_4$ to $C_{\rm db}$ depends on the area, drain voltage, and doping concentration. Dissimilarity in $C_{\rm db}$ of STI-De-n-MOS and STI-De-p-MOS is due to placement of their triple well structures.

## IV. LS Topology and Circuit Optimization

In this section, we present the application of STI-DeMOS in a high-speed LS changing the digital signal swing from 0–1.2 to 3.8–5 V in 65-nm CMOS process (Section II-B).

STI-DeMOS devices, investigated in this paper, sustain high $V_{\rm DS}$ and $V_{\rm GD}$ voltage levels (i.e., $\sim$10 V). However, the thin

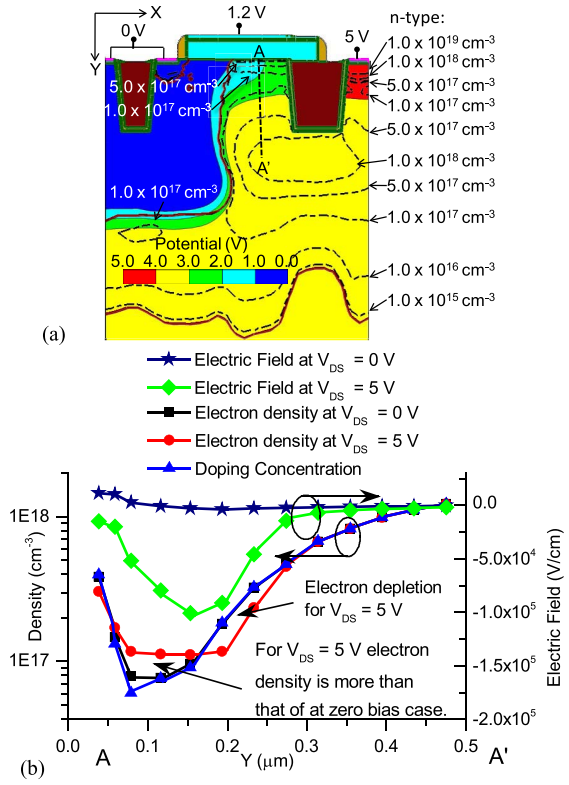


Fig. 5. (a) Potential contour in STI-DeMOS device for a drain bias of 5 V and doping concentration contour. (b) Local junction formation due to retrograde doping profile and corresponding high electric field (TCAD simulation).

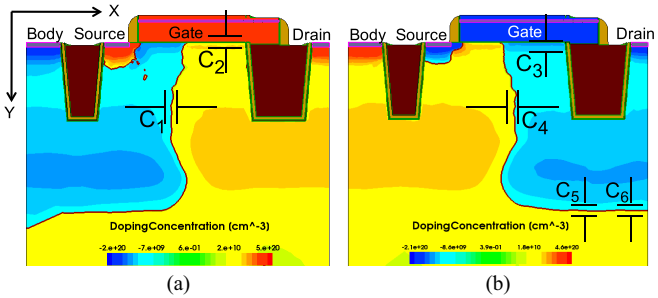


Fig. 6. Capacitances of (a) De-n-MOS and (b) De-p-MOS devices within the drift region, which vary with layout parameters and doping of the well surrounding the drain. $C_1$, $C_4$, $C_5$, and $C_6$ contribute to $C_{\rm db}$; $C_2$ and $C_3$ contribute to $C_{\rm gd}$ (TCAD simulation).

gate oxide limits the maximum absolute value of $V_{\rm GS}$ to 1.2 V. Therefore, these devices are asymmetrical.

Fig. 7 shows the LS circuit of SSDeNP type comprising a pair of STI-De-p-MOS devices (P5 and P6), a pair of STI-De-n-MOS transistors (N5 and N6), a latch, an inverter and output buffer chain using low-voltage transistors. Rise and fall time of the input signal is considered as 30 ps (30 ps is the practical rise and fall time in 65-nm CMOS technology). The motivation is to use appropriate devices available in calibrated setup in 65-nm technology (Section II-B) and optimize the DeMOS devices to obtain the best performance from LS. For this purpose, a device–circuit co-design approach is followed. Most of the parameters are layout related and hence the approach provides the guidelines for circuit designers.

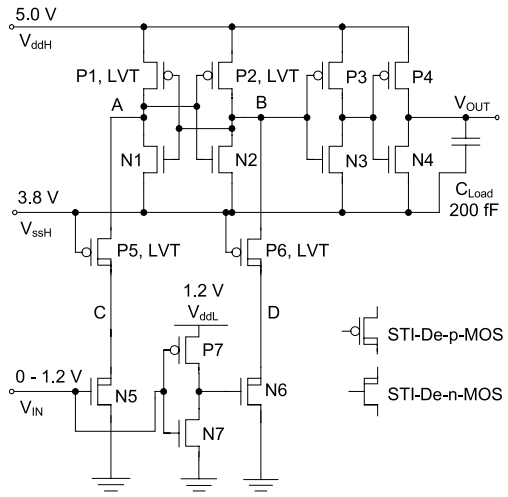


Fig. 7. LS circuit used in this paper.

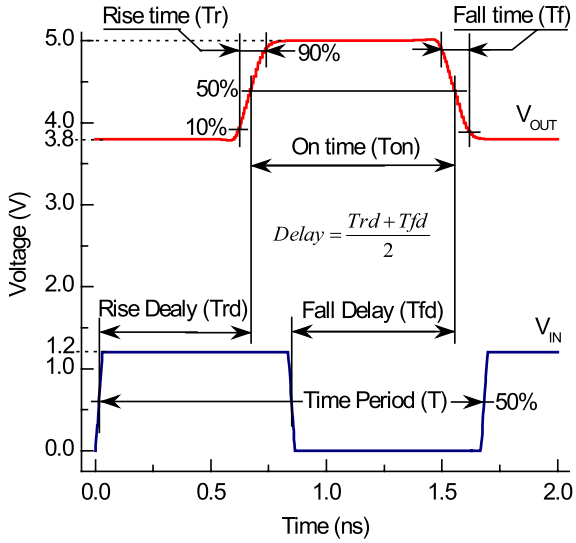


Fig. 8. Typical waveforms for the LS circuit (TCAD simulation).

The LS circuit requires three power supply levels, $V_{ddL} = 1.2$ V, $V_{ssH} = 3.8$ V, and $V_{ddH} = 5.0$ V. The latch (comprising P1, P2, N1, and N2) toggles between 3.8 and 5.0 V. Output of the latch is connected to a buffer chain, which drives the load capacitance. Although the buffer is designed to drive a 200-fF load, it can be redesigned according to any load. De-p-MOS devices P5 and P6 act as HV insulators with their sources connected to the latch outputs A and B, respectively. When input toggles P5 and P6 provide the corresponding pulse to the latch for changing its state. All DeMOS devices of the circuit are arranged in such a way that their gate to source voltage never exceeds 1.2 V and hence any overstress on gate-source oxide is avoided. As drain of P5 and P6 supports higher voltage than 1.2 V nodes C and D may vary from 0 to 5 V without overstress on any of the devices. Typical input and output waveforms of the investigated LS are shown in Fig. 8.

In a multiple supply system, the power-on sequence always begins with the highest supply voltage followed by the lowest

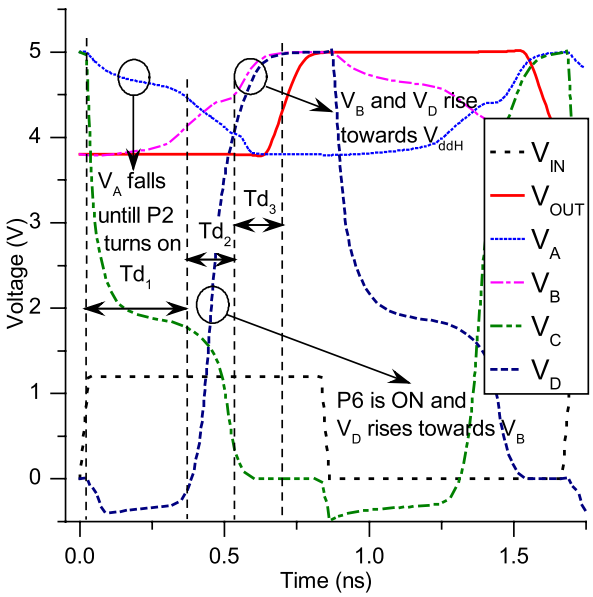


Fig. 9. LS delay partitioning. $V_A$, $V_B$, $V_C$, and $V_D$ are respective node voltages (Fig. 7). $V_{IN}$ is input signal and $V_{OUT}$ is the output signal (TCAD simulation).

supply voltage. In LS, since $V_{ssH}$ is generated from $V_{ddH}$, both supply levels ramp up simultaneously. This avoids any stress on the transistors. As soon as the lowest supply turns on, N5 or N6 turns on. This ties node A or B to 3.8 V irrespective of its initial voltage. Thus output of the LS is always predictable.

We measure the rise and fall delay as time elapsed between 50% of input swing and 50% of output swing (Fig. 8). In reported LSs for I/O applications, two performance measures, important in real designs, are often ignored [5], [8], [9], [18]. These are rise to fall time ratio and difference between the high–low and the low–high propagation delays, which translates into duty cycle. For an optimized LS, duty cycle of the final output should remain within 45%–50% and ratio of rise to fall time within 0.9 to 1.1.

Based on the operating region of individual transistors, the rise delay is divided into delays $Td_1$, $Td_2$, and $Td_3$, as shown in Fig. 9. A simple RC model, shown in Fig. 10, is used to analyze the details of the transient behavior.

When input signal changes from low to high

**Delay $Td_1$**

1) P1, P5, and N6 have been ON.
2) $V_A$ falls till $V_A = V_{ddH} - |V_{th}$ of P2|.
3) $Td_1 = f$(drive strength of P5 and N5, and $C_A$) $C_A$ and $C_C$ are capacitance at nodes A and C, respectively (Fig. 10). We ignore effect of $C_C$ as $V_C$ quickly drops.

**Delay $Td_2$**

4) The latch is metastable and $V_B$ does not change much.
5) P2 is ON and N6 is OFF
6) P6 is turned on and $V_D$ starts rising toward $V_B$.
7) $Td_2 = f$(drive strength of P6 and $C_D$). $C_D$ is node capacitance at node D.

**Delay $Td_3$**

8) P6 is ON, and N6 remains OFF.
9) $V_B$ rises due to positive feedback and $V_D$ follows $V_B$.

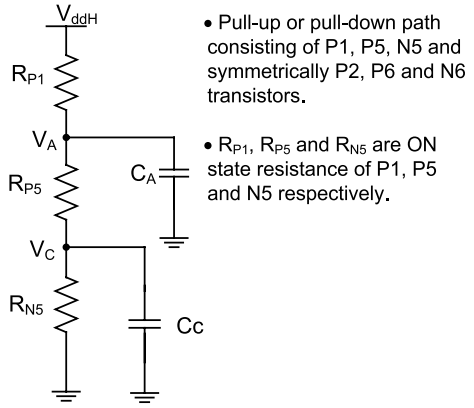


Fig. 10. Simple RC model showing pull-up and pull-down paths of the LS.

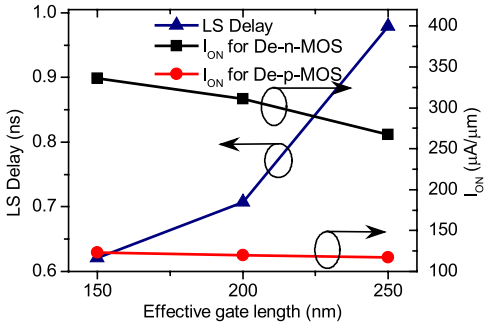


Fig. 11. Variation of average delay of the LS and $I_{ON}$ per unit width as a function of $L_{eff}$ in STI-De-n-MOS and STI-De-p-MOS (TCAD simulation).

10) $Td_3 = f$(drive strength of P2, and $C_B$ and $C_D$). $C_B$ is node capacitance at node B.

## V. Device–Circuit Co-Optimization

We consider the layout parameters $L_{eff}$, $L_{OV}$, STI width, and doping profile of the well-surrounding drain of the DeMOS (Fig. 15). Width of transistors P1, P5, and N5 (and by symmetry P2, P6, and N6) are chosen in proportion so that LS state will toggle as input changes. This is because pull-down path (Fig. 10) for node A (or B) is defined by these transistors.

### A. Optimization of $L_{eff,min}$

The DeMOS devices do not exhibit $I_{ON}/L_{eff}$ proportionality as the core devices show. This is due to their high resistance between the outer and inner drains. Therefore, the aspect ratio is not kept constant as $L_{eff}$ varies to be able to observe the effect of $L_{eff}$. Instead, widths of the transistors are kept constant. Fig. 11 shows an increase in the LS delay when $L_{eff}$ of both STI-De-n-MOS and STI-De-p-MOS transistors increases. $I_{ON}$ of STI-De-n-MOS decreases when $L_{eff}$ increases and hence LS delay increases. However, $I_{ON}$ variation of STI-De-p-MOS is marginal as $L_{eff}$ varies. The difference in $I_{ON}$ variation is due to the different effective resistance in the drift well.

$L_{eff}$ should be chosen with some margin from minimum possible values to reduce the leakage current due to punchthrough and effect of misalignment during fabrication.

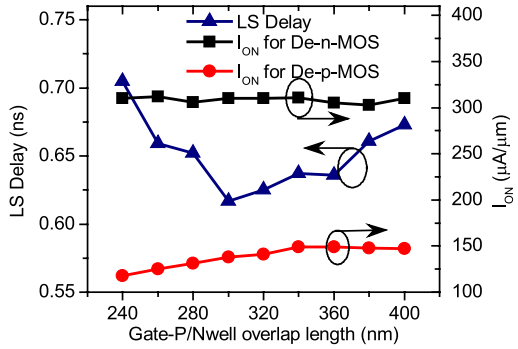


Fig. 12. Variation of average delay and $I_{ON}$ as parameter $L_{OV}$ is varied in both STI-De-n-MOS and STI-De-p-MOS (TCAD simulation).

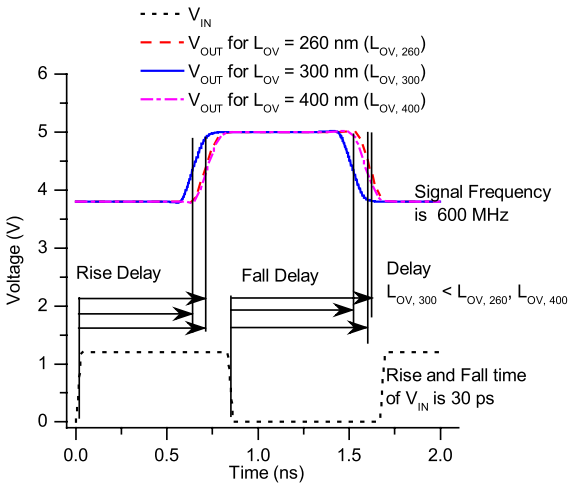


Fig. 13. Output waveforms of LS for different $L_{OV}$ values (TCAD simulation).

### B. Optimization of $L_{OV}$

Fig. 12 shows the delay variation of the LS circuit and variation of $I_{ON}$ (per unit width) in STI-DeMOS as a function of $L_{OV}$. Initially, the delay drops and then began to increase as $L_{OV}$ increases. $I_{ON}$ of STI-De-p-MOS increases for $L_{OV} = 240$ nm–$L_{OV} = 340$ nm. For STI-De-p-MOS, $C_{db}$ [$C_4$ with an L-shaped area in Fig. 6(b)] between the overlap region and the body well region increases as $L_{OV}$ expands. $C_{dg}$ [$C_3$ in Fig. 6(b)] also increases and so does node capacitances $C_C$ and $C_D$. Initially, $I_{ON}$ of P5 or P6 increases as overlap length increases (series resistance reduces until resistance of overlap region is negligible, compared with the drain region resistance) and hence decrease in delay $Td_1$ overcomes increase in $Td_2$ and $Td_3$ (due to increase in node capacitances). Therefore, delay decreases. At higher values of $L_{OV}$ increase in $Td_2$ and $Td_3$ dominates and so delay increases. Thus, an U-shaped delay curve is observed and it also shows that $L_{OV}$ at maximum $I_{ON}$ is not the optimal value. Rise and fall delay of final output of the LS circuit for three different values of $L_{OV}$ are compared in Fig. 13. The waveform for $L_{OV} = 300$ nm exhibits lower rise and fall delay as compared with $L_{OV} = 260$ nm and $L_{OV} = 400$ nm.

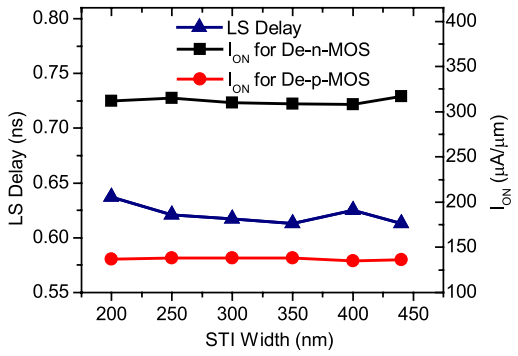


Fig. 14. Simulated average delay and $I_{ON}$ variation when STI width of both STI-De-n-MOS and STI-De-p-MOS is varied (TCAD simulation).

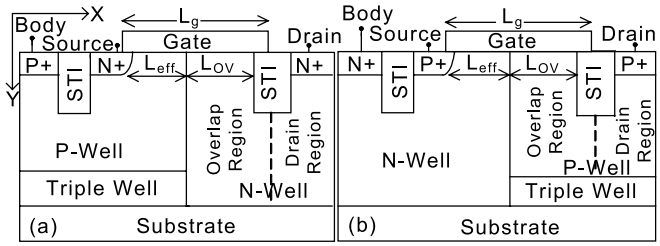


Fig. 15. Overlap and drain regions in STI-DeMOS device for studying the effect of doping profile variation. (a) STI-De-n-MOS. (b) STI-De-p-MOS.

### C. Optimization of STI Width

Fig. 14 shows the simulated delay of LS as a function of change in the STI width. As STI width increases the drift region under the STI extends. This region has a negligible resistance. Hence, $I_{ON}$ of both STI-De-p-MOS and STI-De-n-MOS marginally varies. Though potential in the drift region drops from drain to overlap region, the part of junction capacitance [$C_5$ in Fig. 6(b)] under STI region still has high reverse bias. So, contribution to the node capacitance is insignificant. In case of STI-De-n-MOS transistor, p-well is surrounded by the drain n-well and triple well [Fig. 2(a)]. So, change in STI width does not change drain n- and p-well substrate junction capacitance. Therefore, delay remains constant as STI width varies up to 440 nm. A narrow STI is preferred but it will increase gate to the drain fringe capacitance and will be subjected to process variations.

### D. Optimization of Doping Profile

For the study of doping profile, the well surrounding the drain (drift region) is considered in two distinct regions: overlap and drain region, as shown in Fig. 15. Overlap region is the well region underneath the gate n-/p-well overlap.

If doping in the overlap region increases, $C_{db}$ increases. Doping concentration of low-doped regions in the drift area also increases. This leads to less potential drop in these regions and higher potential available to the inner drain. Hence, $I_{ON}$ increases. Variation of delay and $I_{ON}$ with doping concentration is shown in Figs. 16 and 17. The doping profile is varied by varying implantation dose [Figs. 16(a) and (b) and 17(a) and (b)]. A reduction in the delay is observed when doping in overlap region of STI-De-n-MOS

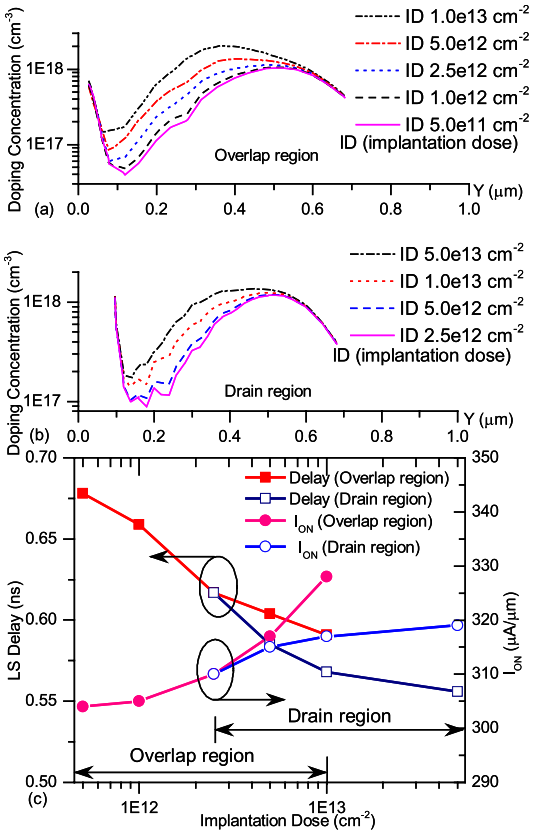


Fig. 16. (a) Doping concentration in the overlap region. (b) Doping concentration in the drain region. (c) Average delay and $I_{ON}$ variation, when implantation dose in n-well of STI-De-n-MOS is varied (TCAD simulation).

increases (Fig. 16) as $I_{ON}$ and $C_{db}$ (hence $C_D$) increases. So, $Td_2$ and $Td_3$ increase but $Td_1$ reduces and net delay reduces.

When doping profile in the drain region of STI-De-n-MOS is varied there is no change in $C_{db}$ and hence in $C_D$ [Fig. 6(a)]. Furthermore, lower is the potential drop in the drift region, higher potential will be available to the channel and hence the transistor begins to enter into saturation rapidly. So $I_{ON}$ and hence the delay begin to saturate [Fig. 16(c)].

For STI-De-p-MOS [Fig. 17(c)], when doping of overlap or drain region increases, the delay first reduces and then saturates. The $C_{db}$ and hence $C_D$ increase when doping of overlap region increases leading to increases in $Td_2$ and $Td_3$. However, $Td_1$ reduces since $I_{ON}$ of P5 and P6 increases. So, the overall delay depends on whether $Td_1$ or $Td_2$ and $Td_3$ dominate. As doping in the drain region increases $C_{db}$ does not vary much and hence increase in $I_{ON}$ reduces the delay. At higher doping concentrations, $I_{ON}$ is limited by overlap region and channel resistance. So, $I_{ON}$ and delay become steady.

## VI. Results and Discussion

Effect of $L_{eff}$ is different for DeMOS devices as compared with core devices because of drain resistance. The effect is not even same for STI-De-n-MOS and STI-De-p-MOS due to the difference in their drift region. We showed that

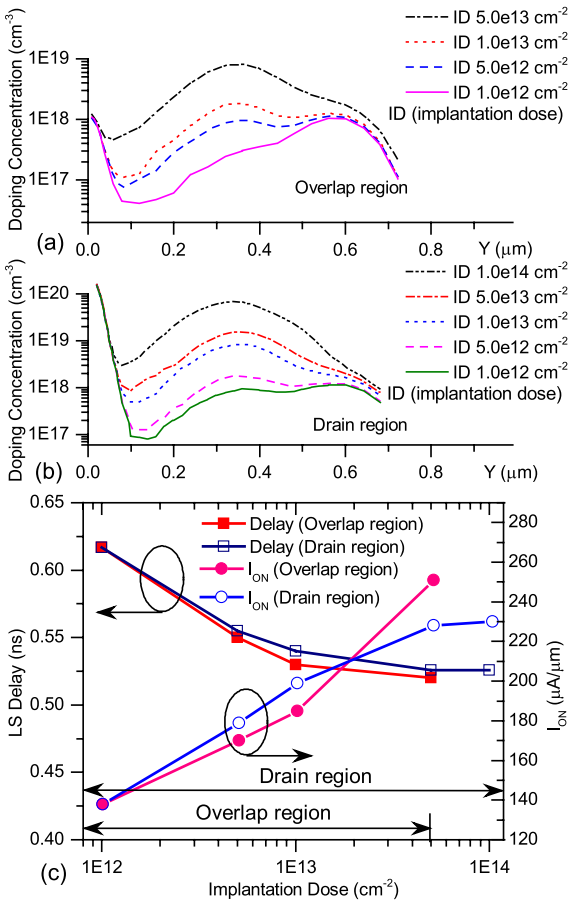


Fig. 17. (a) Doping concentration in overlap region. (b) Doping concentration in the drain region. (c) Average delay and $I_{ON}$ variation when implantation dose (doping profile) in p-well of STI-De-p-MOS is varied (TCAD simulation).

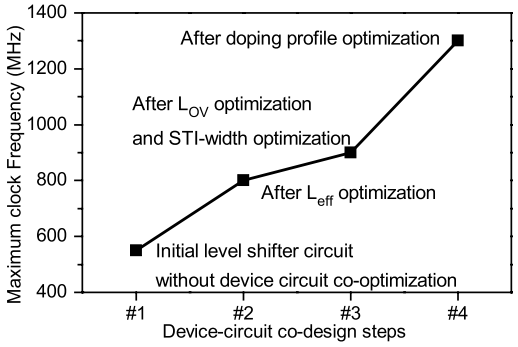


Fig. 18. Performance improvement of device–circuit co-optimized LS (TCAD simulation).

lower the $L_{\text{eff}}$ (limited by punchthrough) lower is the delay but $I_{\text{ON}}$ is not inversely proportional to $L_{\text{eff}}$ as long as the effects of other resistors are dominating. So, sensitivity of the delay to $L_{\text{eff}}$ is not predictable. The U-shaped delay as a function of $L_{\text{OV}}$ is due to significance of either $I_{\text{ON}}$ or parasitic capacitances.

For the target technology, the STI width up to 440 nm has a negligible effect on the LS speed. The optimum value for STI width should be chosen considering the process stability.

The difference in doping of low- and high-doped regions in the overlap and drain regions determines the amount of voltage drop. This voltage drop is measure of available voltage at the inner drain, determining the transistor operating region. The drift well region is different for STI-De-n-MOS and STI-De-p-MOS due to the triple well structure. Hence, parasitic components affect the circuit performance differently. The optimization flow is shown in Fig. 18.

TABLE III
PERFORMANCE COMPARISON OF LS WITHOUT AND WITH DEVICE–CIRCUIT CO-OPTIMIZATION (I/O SWING = 1.2 V, $C_{\text{Load}}$ = 200 fF) (TCAD SIMULATION)

| Performance parameters | Without device-circuit co-optimized | With device-circuit co- optimized |
|---|---|---|
| Average delay (ns) | 1 | 0.45 |
| Duty cycle (%) | 49.9 | 48 |
| Average power (mW) | 4.8 | 6.8 |
| Standby power (μW) | 1.0 | 1.1 |
| Max. clk. Freq. (MHz) | 550 | 1300 |

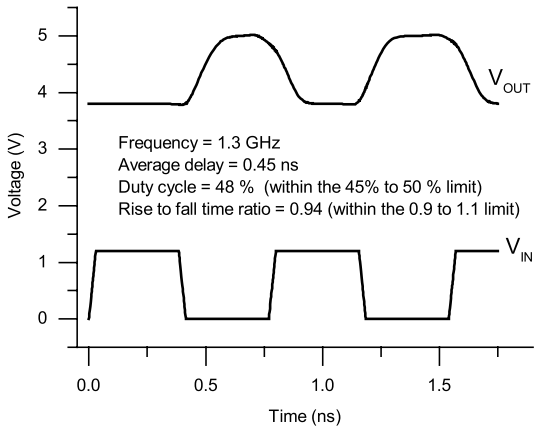


Fig. 19. Waveforms of device–circuit co-optimized LS (TCAD simulation).

Initial LS without optimization and device–circuit co-optimized LS are compared in Table III. In both cases, the LS circuit has nearly same transistor widths. The maximum clock frequency of operation is almost doubled for the co-optimized LS while keeping the duty cycle within the desired value. The junction breakdown voltage of STI-De-n-MOS and STI-De-p-MOS of the optimized LS circuit are 8.6 and 6.6 V, respectively. Simulated input/output waveforms of co-optimized circuit at 1.3 GHz are shown in Fig. 19.

## VII. CONCLUSION

Optimization of layout parameters of STI-DeMOS devices for LS application is presented. It is shown that how the characteristics of the well in the drift region affect the performance of the circuit for HV applications. We demonstrate that with proper optimization of layout parameters the operating frequency of LS can be increased close by twofold without scarifying duty cycle and breakdown voltage. We also show that the performance further improves if doping profile of drift zone is optimized.

## REFERENCES


[1] S.-F. Hsu and M.-D. Ker, "Dependence of device structures on latchup immunity in a high-voltage 40-V CMOS process with drain-extended MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 4, pp. 840–851, Apr. 2007.

[2] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part I: Mixed-signal performance of various high-voltage DeMOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[3] B. Serneels, M. Steyaert, and W. Dehaene, "A high speed, low voltage to high voltage LS in standard 1.2 V 0.13 $\mu$m CMOS," *Analog Integr. Circuits Signal Process.*, vol. 55, no. 1, pp. 85–91, Apr. 2008.

[4] D. Pan, H. W. Li, and B. M. Wilamowski, "A low voltage to high voltage LS circuit for MEMS application," in *Proc. Biennial Univ. Government Ind. Microelectron. Symp.*, 2003, pp. 128–131.

[5] Y. Moghe, T. Lehmann, and T. Piessens, "Nanosecond delay floating high voltage level shifters in a 0.35 $\mu$m HV-CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 485–496, Feb. 2011.

[6] M. Khorasani, L. van den Berg, P. Marshall, M. Zargam, V. Gaudet, D. Elliott, *et al.*, "Low-power static and dynamic high-voltage CMOS level-shifter circuits," in *Proc. IEEE ISCAS*, May 2008, pp. 1946–1949.

[7] J. Doutreloigne, H. De Smet, and A. Van Calster, "A versatile micropower high-voltage flat-panel display driver in a 100-V 0.7-$\mu$m CMOS intelligent interface technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2039–2048, Dec. 2001.

[8] Z. Huang, Y. Savaria, and M. Sawan, "A dynamically controlled and refreshed low-power level-up shifter," in *Proc. 47th IEEE Int. Midwest Symp. Circuits Syst.*, Jul. 2004, pp. 97–100.

[9] S. C. Tan and X. W. Sun, "Low power CMOS level shifters by bootstrapping technique," *Electron. Lett.*, vol. 38, no. 16, pp. 876–878, Aug. 2002.

[10] J. C. Lee and J. Y. Jeong, "High speed, small area, reliable, LTPS TFT-based level shifter for system-on-panel technology," in *Proc. IEEE ICICDT*, Jun. 2006, pp. 1–4.

[11] W.-K. Park, C.-U. Cha, and S.-C. Lee, "A novel level-shifter circuit design for display panel driver," in *Proc. 49th IEEE Int. Midwest Symp. Circuits Syst.*, Aug. 2006, pp. 391–394.

[12] P. Swaroop, A. J. Vasani, and M. Ghovanloo, "A high-voltage output driver for implantable biomedical stimulators and I/O applications," in *Proc. IEEE Int. Midwest Symp. Circuits Syst.*, Aug. 2006, pp. 566–569.

[13] E. J. Mentze, K. M. Buck, H. L. Hess, D. Cox, and M. Mojarradi, "A low voltage to high voltage level shifter in a low voltage, 0.25 $\mu$m, PD SOI process," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI*, Feb. 2004, pp. 218–221.

[14] M. Shrivastava, C. Russ, H. Gossner, S. Bychikhin, D. Pogany, and E. Gornik, "ESD robust DeMOS devices in advanced CMOS technologies," in *Proc. EOS/ESD*, Sep. 2011, pp. 1–10.

[15] M. Shrivastava, S. Bychikhin, D. Pogany, J. Schneider, M. S. Baghini, H. Gossner, *et al.*, "Filament study of STI type drain extended NMOS device using transient interferometric mapping," in *Proc. IEEE IEDM*, Dec. 2009, pp. 417–420.

[16] M. Shrivastava, H. Gossner, and C. Russ, "A drain extended mos device with spreading filament under ESD stress," *IEEE Electron Device Lett.*, vol. 33, no. 9, pp. 1294–1296, Sep. 2012.

[17] K. W. Boer, *Introduction to Space Charge Effects in Semiconductors*. New York, NY, USA: Springer-Verlag, 2010.

[18] W.-T. Wang, M.-D. Ker, M.-C. Chiang, and C.-H. Chen, "Level shifters for high-speed 1-V to 3.3-V interfaces in a 0.13-$\mu$m Cu-interconnection/low-k CMOS Technology," in *Proc. Int. Symp. VLSI Technol., Syst., Appl.*, 2001, pp. 307–310.


**Peeyusha Saurabha Swain** is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, Center for Excellence in Nanoelectronics, IIT Bombay, Mumbai, India.

His current research interests include high voltage device circuit co-design in nanoscale technology.

**Mayank Shrivastava** (S'09-–M'10) received the Ph.D. degree from the IIT Bombay, Mumbai, India, in 2010.

His current research interests include ESD protection, HV MOS devices for advanced CMOS, Nanoscale devices for advanced and beyond CMOS, device-circuit co-design, electro-thermal modelling, and RF power amplifiers design.

**Harald Gossner** (M'06-–SM'11) received the Ph.D. degree in electrical engineering from Universität der Bundeswehr, Munich, Germany, in 1995.

His current research interests include ESD protection design, EDA tool exploration, and system ESD design methodology for high voltage bipolar and BiCMOS.

**Maryam Shojaei Baghini** (M'00–SM'09) received the M.S. and Ph.D. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 1991 and 1999, respectively.

She is currently an Associate Professor with the Department of Electrical Engineering, IIT Bombay, Mumbai, India.