Part II: Design of Well Doping Profile for Improved Breakdown and Mixed-Signal Performance of STI-Type DePMOS Device

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***Abstract*—Shallow-trench isolation drain extended pMOS (STI-DePMOS) devices show a distinct two-stage breakdown. The impact of p-well and deep-n-well doping profile on breakdown characteristics is investigated based on TCAD simulations. Design guidelines for p-well and deep-n-well doping profile are developed to shift the onset of the first-stage breakdown to a higher drain voltage and to avoid vertical punch-through leading to early breakdown. An optimal ratio between the OFF-state breakdown voltage and the ON-state resistance could be obtained. Furthermore, the impact of p-well/deep-n-well doping profile on the figure of merits of analog and digital performance is studied. This paper aids in the design of STI drain extended MOSFET devices for widest safe operating area and optimal mixed-signal performance in advanced system-on-chip input–output process technologies.**

***Index Terms*—Avalanche breakdown, drain extended MOSFET (DeMOS), input–output (I/O), mixed-signal performance, OFF-state breakdown voltage, ON-state resistance, two-stage breakdown, well doping profile.**

I. Introduction

DRAIN EXTENDED MOSFETs (DeMOSs) and laterally diffused MOS (LDMOS) devices are versatile building blocks in input–output (I/O) interface circuits operating at different power supply voltages, mainly above the core supply level [1]. Due to an asymmetric drain structure, they provide a high breakdown voltage. Both p-type and n-type DeMOS devices can be easily integrated into the standard triple-well CMOS process technology. Since these devices need to handle larger operating voltages and currents relative to core logic devices, robustness under high-current and high-voltage operation is essential. A high OFF-state breakdown voltage (V_{BD}), a low ON-state resistance (R_{ON}), mixed-signal device performance, robustness against electrostatic discharge, and hot-carrier stresses are the main figure of merits of high-voltage devices [1], [2]. Device concepts, such as reduced surface field (RESURF) LDMOS [3] and superjunction LDMOS [4], improve the ON-resistance and OFF-state breakdown voltage. In [5], an n-type RESURF implant under field oxide is used to enhance LDMOS safe operating area (SOA) without degrading the OFF-state breakdown voltage and ON-resistance.

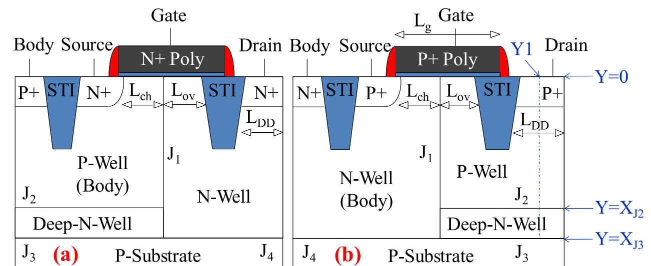

Fig. 1. Schematics of (a) STI-DeNMOS and (b) STI-DePMOS device structures under study. The design of doping concentration profile along the vertical cutline $Y1$ (through the middle of the drain diffusion region) and the role of junctions J_1–J_4 in improving breakdown performance of STI-DePMOS are described in Section III.

In [6], the physical mechanisms of two-stage drain breakdown characteristics were studied, which were measured on a shallow-trench isolation-type drain extended pMOS (STI-DePMOS) device structure (Fig. 1), as described in Section II. The analyses revealed that the coupling between junctions J_1, J_2, and J_3 [Fig. 1(b)], as the drain voltage is increased, is responsible for triggering of the two stages of breakdown. We showed that the first-stage breakdown occurs due to the vertical punch-through, resulting in poor SOA of the device, whereas the second-stage breakdown occurs due to avalanche breakdown of lateral n-well/p-well junction. This paper is organized as follows. Section II describes the device structures, the output characteristics of STI-DePMOS, and the simulation setup. Then, Section III investigates in depth the design of p-well and deep-n-well doping profile of an

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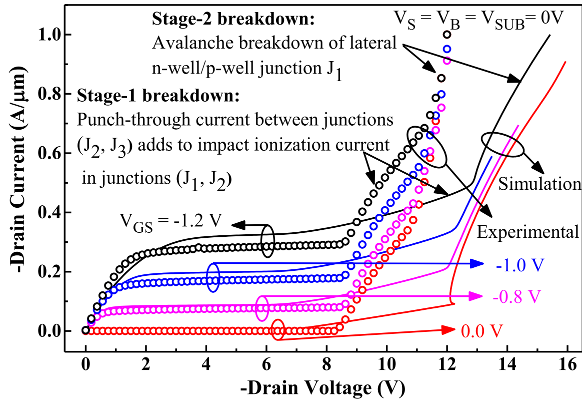

Fig. 2. Drain output characteristics of a (reference) STI-DePMOS device depicting a unique two-stage breakdown behavior. Both experimental and simulated dc characteristics are compared.

STI-DePMOS device. It provides insights into breakdown mechanisms for each profile design and describes how to improve both the OFF-state breakdown voltage and ON-state resistance. Section IV describes the impact of well doping profile on analog, RF, and digital performance figure of merits. Since the same triple-well CMOS process is used for both n- and p-type DeMOS devices, the impact of the optimal well doping for STI-DePMOS on the performance of STI drain extended NMOS (STI-DeNMOS) is studied in Section V. Finally, conclusions are drawn in Section VI.

II. Device Structure, I–V Characteristics, and Simulation Setup

A. Device Structure and I–V Characteristics

Fig. 1 shows the schematics of the STI-DeNMOS and STI-DePMOS devices under study. Each structure uses the three wells: 1) n-well; 2) p-well; 3) and deep-n-well. The deep-n-well of higher resistivity is added below p-well in a triple-well CMOS process to isolate analog and digital circuits in mixed-signal integrated circuits. The mixed-signal performance of STI-DeMOS devices is significantly degraded compared with non-STI-type DeMOS devices due to higher drift region resistance of the STI structure and subsurface carrier current path outside gate control [1]. All the device geometric parameters labeled in Fig. 1(a) and (b) are the same as those defined in [6]. These values are valid for both measured (actual) devices and simulated (reference) devices. As shown in Fig. 2, experimental and simulated I_D–V_D characteristics of STI-DePMOS exhibit a two-stage breakdown behavior. While the discrepancy in the quantitative values between the simulation and the experiment is due to the details of the doping profile, the qualitative two-stage breakdown behavior is properly reflected by the simulation. First- and second-stage breakdown in the simulated OFF-state drain characteristics are, respectively, triggered at $V_{DS} = -4.9$ and -12.1 V [6]. The simulated output characteristics in Fig. 2 are used as reference I_D–V_D characteristics that are to be optimized (in Sections III and IV) for high breakdown voltage and mixed-signal performance. For the simulated reference device, the OFF-state breakdown voltage (V_{BD}), which is defined as the V_{DS} value at $V_{GS} = 0$ V and $I_D = -0.1$ nA/μm, is -5.3 V. All process simulations in this paper are performed using [7]. The same device simulation models [8] as used in Part I of this paper [6] are used for dc, ac, and transient device simulations.

TABLE I

Modifications of p-Well and Deep-n-Well Doping Profiles of STI-DePMOS Devices Using Process Simulation

Device	P-Well Parameters	Deep-N-Well Parameters
A	Dose –, Energy ↓ Peak doping –, Depth ↓	Dose –, Energy – Peak doping ↑, Depth –
B	Dose –, Energy ↑ Peak doping ↓, Depth ↓	Dose ↑↑, Energy ↑↑ Peak doping ↑↑, Depth ↑
C	Dose ↓, Energy ↓ Peak doping –, Depth ↓	Dose ↓, Energy – Peak doping –, Depth –
D	Dose ↑, Energy ↓ Peak doping ↑, Depth ↓	Dose ↑, Energy – Peak doping –, Depth –
E	Dose ↑, Energy ↑ Peak doping ↑, Depth ↑	Dose ↑↑, Energy ↑↑ Peak doping ↑, Depth ↑
F	Dose ↑, Energy ↑ Peak doping ↑, Depth ↑	Dose ↑↑, Energy ↑ Peak doping ↑↑, Depth ↑
G	Dose ↓, Energy ↑ Peak doping ↓, Depth –	Dose –, Energy – Peak doping –, Depth –

The symbol ↑ means increase, ↑↑ greater increase, ↓ decrease, ↓↓ greater decrease and - means no significant change. The changes of *p*-well and deep-*n*-well parameters in modified devices are relative to reference device.

B. Simulation Setup for Modified Devices

As discussed in [6], the first-stage breakdown voltage of the STI-DePMOS device (punch-through voltage of p-well/deep-n-well/p-substrate) is determined by doping profiles of p-well/deep-n-well junction J_2 region, and the second-stage breakdown voltage is the avalanche breakdown voltage of p-well/n-well junction J_3. Since the breakdown characteristics are affected by p-well and deep-n-well layers [6], doping profiles in these layers are varied using process simulations. The doping profile in n-well (body) is kept unchanged. By varying implantation dose and energy parameters for p-well and deep-n-well in the reference device (described in Table I), devices with modified profiles (A, B, C, ..., G) are obtained. The changes in peak doping concentration in deeper regions of the two wells and the well depths $y = X_{J2}$ and $y = X_{J3}$ (at the end of a source/drain diffusion cycle) are also described in Table I. The values of doses and energies are selected so that p-well and deep-n-well have different peak doping and depths in the modified devices. Hence, devices with a wide range of OFF-state breakdown voltages (V_{BD}) could be obtained. Their OFF-state breakdown characteristics and ON-state resistance (R_{ON}) are investigated in detail in Section III. For each device, junction depths of p-well/deep-n-well junction J_2 ($y = X_{J2}$) and deep-n-well/p-substrate J_3 ($y = X_{J3}$) (with respect to the silicon surface at $y = 0$) get modified along the vertical cutline $Y1$ through the

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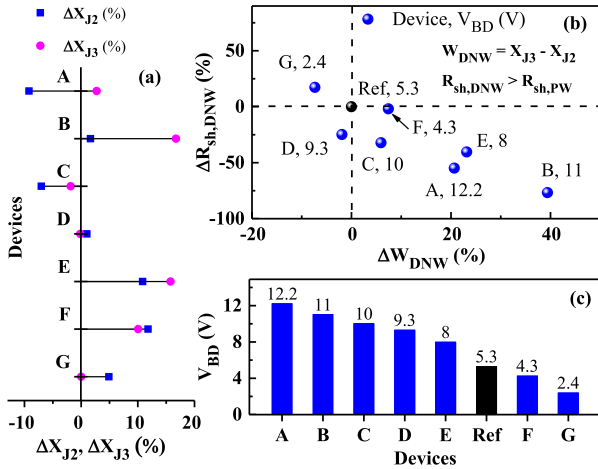

Fig. 3. Percentage change in (a) junction depths X_{J2} and X_{J3} and (b) width (W_{DNW}) (μm) and sheet resistance ($R_{\mathrm{sh,DNW}}$) (Ω/sq.) of a deep-n-well layer for different devices with respect to the reference device. Values of OFF-state breakdown voltage V_{BD} are also shown in (b). (c) V_{BD} decreases from device A to G.

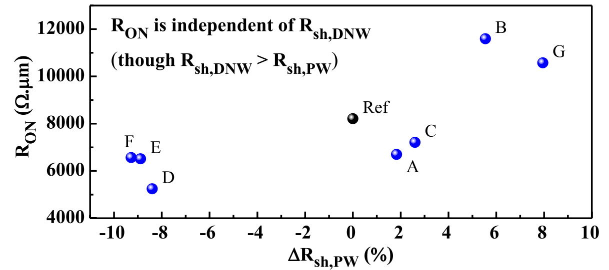

Fig. 4. Variation in ON-state resistance R_{ON} versus percentage change in the sheet resistance ($R_{\mathrm{sh,PW}}$) (Ω/sq.) of a p-well layer (with respect to the reference device) for different devices A–G. Devices B and G have higher R_{ON} compared with other devices due to their relatively higher $R_{\mathrm{sh,PW}}$.

middle of the drain diffusion region [Fig. 1(b)]. Also, sheet resistances (1) of p-well ($R_{\mathrm{sh,PW}}$) and deep-n-well ($R_{\mathrm{sh,DNW}}$) layers are altered. These sheet resistances inversely depend on integrated active dopant concentrations along the vertical cutline $Y1$ [Fig. 1(b)] through carrier concentrations n and p. R_{sh} is defined as

$$R_{\mathrm{sh}} = \frac{1}{\int_{y_1}^{y_2} q(n\mu_n + p\mu_p)dy} \quad (1)$$

where $y_1 = 0$ (X_{J2}) and $y_2 = X_{J2}$ (X_{J3}) for $R_{\mathrm{sh,PW}}$ ($R_{\mathrm{sh,DNW}}$). In (1), q is the electronic charge, n(p) is the electron (hole) concentration, μ_{n} (μ_{p}) is the electron (hole) mobility (both μ_{n} and μ_{p} are defined using a doping concentration-dependent model [7]), and y is an independent variable along the cutline $Y1$. For the simulated reference device, $R_{\mathrm{sh,PW}} = 82$ Ω/sq. and $R_{\mathrm{sh,DNW}} = 2694$ Ω/sq.

Figs. 3 and 4 describe the variation of $R_{\mathrm{sh,PW}}$ and $R_{\mathrm{sh,DNW}}$ for the modified devices with respect to the reference device. The junction depths (X_{J2} and X_{J3}) and the width of deep-n-well ($W_{\mathrm{DNW}} = X_{J3} - X_{J2}$) for the modified devices are shown in Fig. 3(a) and (b). The variations in sheet resistances [Figs. 3(b) and 4] are nonmonotonically related to those in junction depths (X_{J2}, X_{J3}). The dependence of V_{BD} and R_{ON} on $R_{\mathrm{sh,PW}}$, $R_{\mathrm{sh,DNW}}$, and W_{DNW} is discussed in Section III.

III. Design of Well Doping Profile of STI-DePMOS

Since $R_{\mathrm{sh,DNW}}$ is significantly larger than $R_{\mathrm{sh,PW}}$, $R_{\mathrm{sh,PW}}$ does not affect the OFF-state breakdown voltage (V_{BD}) (the value of V_{DS} at $V_{\mathrm{GS}} = 0$ V and $I_D = -0.1$ nA/μm). However, $R_{\mathrm{sh,PW}}$ affects the ON-state resistance (R_{ON}) (at $V_{\mathrm{DS}} = -0.1$ V and $V_{\mathrm{GS}} = -1.2$ V), because most of the linear drain current in the p-well region flows closer to the STI under gate-to-drain overlap. As shown in Fig. 3(b), the device V_{BD} is primarily determined by both $R_{\mathrm{sh,DNW}}$ and the width of the deep-n-well layer ($W_{\mathrm{DNW}} = X_{J3} - X_{J2}$). The devices are referred to with labels A, B, C, ..., G in decreasing order of their V_{BD} values [Fig. 3(c)]. The results show that device V_{BD} can be improved, if $R_{\mathrm{sh,DNW}}$ is decreased by at least 20% (devices A–E). W_{DNW} is increased for these devices, but slightly reduced for device D. However, the improvement in V_{BD} reduces at very low $R_{\mathrm{sh,DNW}}$ and very high W_{DNW} (device B). In addition, V_{BD} does not improve, if W_{DNW} is increased without significantly reducing $R_{\mathrm{sh,DNW}}$ (device F). In addition, V_{BD} significantly degrades at high $R_{\mathrm{sh,DNW}}$ and low W_{DNW} (device G).

The variations in R_{ON} with $R_{\mathrm{sh,PW}}$ in Fig. 4 show that R_{ON} increases at high $R_{\mathrm{sh,PW}}$. The values of V_{BD}, R_{ON}, $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ ratio, and V_T (constant current threshold voltage at $V_{\mathrm{DS}} = -0.1$ V and $I_D = -0.1$ μA/μm) for different devices are compared in Fig. 5. Since R_{ON} is not significantly affected by variations in $R_{\mathrm{sh,DNW}}$ and W_{DNW}, both V_{BD} and R_{ON} for STI-DePMOS can be controlled independently as long as $R_{\mathrm{sh,PW}}$ is significantly smaller than $R_{\mathrm{sh,DNW}}$ [Fig. 5(a)] (unlike the conventional LDMOS devices in [4] and [5]). Device A has not only maximum breakdown voltage, but also maximum $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ ratio. In addition, device D has minimum ON-state resistance. Since doping in n-well (channel) is kept unchanged, threshold voltages V_T are relatively unchanged [Fig. 5(b)]. Since at $V_{\mathrm{DS}} = -0.1$ V and $V_{\mathrm{GS}} = -1.2$ V, the current density in the channel region in n-well for different devices is higher than the current density in the p-well drift region, and the variations in V_T and channel resistance have little contribution to R_{ON}. In fact, R_{ON} monotonically varies with $R_{\mathrm{sh,PW}}$ (Fig. 4).

The OFF-state drain breakdown characteristics of the modified devices are compared with the reference device in Fig. 6. Devices A and B show a negative slope in the breakdown region, whereas other devices show a positive slope. For the sake of clarity, the devices in Fig. 6 are distinguished with three different colors, depending on their V_{BD} values (relative to the reference device) and slope of their breakdown characteristics. It must be noted that the technology-dependent variables W_{DNW} ($=X_{J3} - X_{J2}$), $R_{\mathrm{sh,PW}}$, and $R_{\mathrm{sh,DNW}}$ are calculated for the vertical profile through the middle of drain diffusion, where the doping concentration gradients are primarily vertical (1-D). Nevertheless, the actual 2-D nature of doping profile at the junctions between p-well, deep-n-well, and n-well (body) (junction lines in Figs. 7–9) also affects V_{BD} and R_{ON}, as seen in the deviations in V_{BD} and R_{ON}

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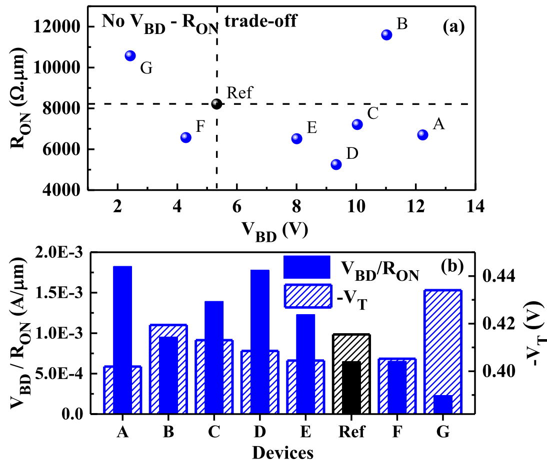

Fig. 5. (a) Comparison of OFF-state breakdown voltage V_{BD} and ON-state resistance R_{ON} of different devices A–G, showing no tradeoff between V_{BD} and R_{ON}. (b) Comparison of (left) V_{BD}/R_{ON} ratio and (right) constant current threshold voltage V_T (at $V_{DS} = -0.1$ V, $I_D = -0.1$ μA/μm) of different devices. Device A has both maximum $V_{BD}$and maximum V_{BD}/R_{ON} ratio. Device D has minimum R_{ON}.

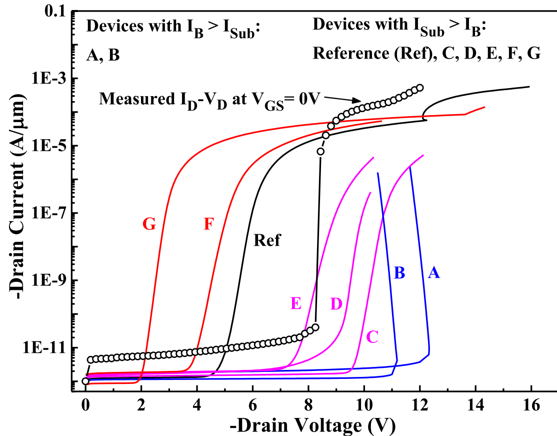

Fig. 6. Simulated OFF-state breakdown characteristics (I_D–V_D at $V_{GS} = 0$ V on log-Y scale) of different devices A–G. Devices A and B (blue lines) show a negative slope in the breakdown region, whereas other devices [devices C, D, and E with high V_{BD} (magenta lines) and devices F and G with low V_{BD} (red lines)] show a positive slope. Measured I_D–V_D at $V_{GS} = 0$ V is also shown for comparison. Legend shows a comparison between n$^+$-body (I_B) and p-substrate (I_{Sub}) currents in the breakdown region for different devices (explained further in Section III).

in Figs. 3(b) and 4. Still, for the initial design, the study based on these variables provides enough physical insights for optimal well doping design to maximize the V_{BD}/R_{ON} ratio. The detailed physics behind the impact of width and sheet resistance of deep-n-well layer on breakdown characteristics is studied below.

1) Breakdown Physics for Devices A and B: We first investigate breakdown physics for devices A and B, which show distinct negative slope (snapback) in their breakdown characteristics (Fig. 6). For these devices, body current (I_B) (at n-well contact) is found to dominate over substrate current (I_{Sub}) (at the bottom of p-substrate) in the breakdown region (not shown). The sheet resistance of deep-n-well is reduced, and the width of deep-n-well is increased. This helps in reducing field spreading in the deep-n-well layer when p-well/deep-n-well junction J_2 is under high reverse bias.

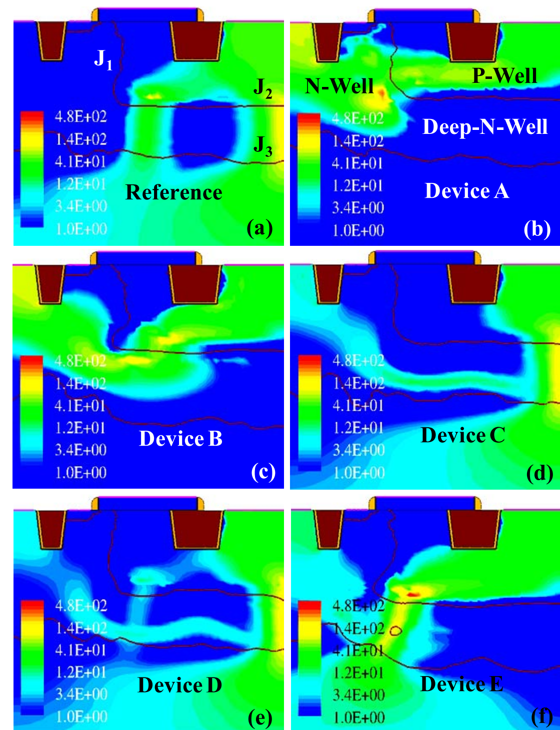

Fig. 7. Conduction current density (A/cm^2) contour at $V_{GS} = 0$ V and $I_D = -0.1$ μA/μm in different STI-DePMOS devices. (a) Reference. (b) Device A. (c) Device B. (d) Device C. (e) Device D. (f) Device E. Devices in (b)–(f) have higher V_{BD} compared with the reference device (a).

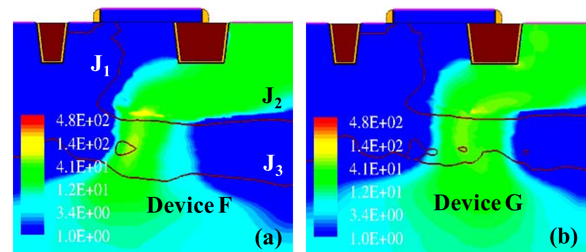

Fig. 8. Conduction current density (A/cm^2) contour at $V_{GS} = 0$ V and $I_D = -0.1$ μA/μm in different STI-DePMOS devices. (a) Device F. (b) Device G. Devices in (a) and (b) have lower V_{BD} compared with the reference device [Fig. 7(a)]. The contour range is kept the same as that of conduction current density in Fig. 7 for the sake of comparison.

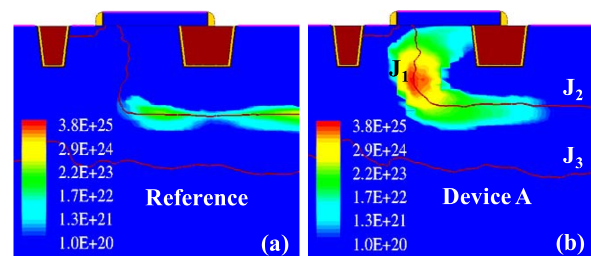

Fig. 9. II (1/cm^3) contour at $V_{GS} = 0$ V and $I_D = -0.1$ μA/μm in (a) reference device and (b) device A. The II hot spot peaks at junction J_2 for the reference device, whereas it peaks at junction J_1 for device A. However, for all other modified devices B–G, the II hot spot dominates over junction J_2 (not shown).

Figs. 7 and 8 show for different devices the conduction current density contours in the OFF-state at drain current level $I_D = -0.1$ μA/μm (which is well above the breakdown point

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of $I_D = -0.1$ nA/μm). Since conduction current density is far lower in the p-substrate region than in the p-well and the deep-n-well for devices A and B, vertical punch-through is avoided, effectively decoupling junctions J_2 and J_3, unlike the reference device (Fig. 7). In addition, dominant OFF-state current flow is through lateral n-well/p-well junction J_1 for device A [Fig. 7(b)], whereas current flow spreads in the deep-n-well through the bottom-left junction between J_1 and J_2 for device B [Fig. 7(c)]. Hence, the reduction in improvement of V_{BD} for device B compared with device A is because of higher breakdown voltage of lateral junction J_1 (for A) compared with the bottom-left junction region between J_1 and J_2 (for B) (which is determined by relative doping concentration distribution around junctions J_1 and J_2). Dominant impact ionization (II) hot spot at $I_D = -0.1$ μA/μm and $V_{GS} = 0$ V is shifted from vertical p-well/deep-n-well junction J_2 for the reference device to lateral n-well/p-well junction J_1 for device A (Fig. 9). For other devices, peak II occurs at junction J_2 (not shown). Hence, breakdown in device A shows the STI-DeNMOS-like breakdown behavior [6], despite the differences in field distribution due to junction J_2. Hence, these results indicate that in order to eliminate the two-stage breakdown behavior, the p-well/deep-n-well doping profile should be designed with moderately low sheet resistance (compared with p-well) and moderately high width of deep-n-well layer. This design helps to reduce the peak field around junction J_2 and field spreading in the deep-n-well, thus enhancing the device breakdown voltage and SOA.

2) Breakdown Physics for Devices C–G: Each of the remaining devices C–G exhibit a positive slope in their breakdown characteristics (Fig. 6). In addition, I_{Sub} dominates over I_B in the breakdown region. The breakdown current flow spreads in deep-n-well and p-substrate for each of these devices, indicating the occurrence of punch-through [Figs. 7(d)–(f) and 8]. Their breakdown voltage is determined by drain voltage at the onset of punch-through. It is worth investigating the differences in breakdown voltages for these devices. Devices C–E, which have lower $R_{sh,DNW}$ (but the reduction in $R_{sh,DNW}$ is lower compared with devices A and B) and higher W_{DNW}, have a higher punch-through voltage. Punch-through voltage slightly reduces for device F, because of the 2-D nature of field and current distribution. If $R_{sh,DNW}$ is increased and W_{DNW} is decreased, punch-through voltage drops leading to poor breakdown voltage (device G). Hence, device breakdown voltage can be improved, if punch-through voltage is increased (by reducing $R_{sh,DNW}$).

Furthermore, we compare the OFF-state field distribution in STI-DePMOS devices as a function of their well doping profiles (Fig. 10). When devices are biased at $V_{GS} = 0$ V and $I_D = -0.1$ μA/μm, field distribution has local maxima in different locations. In the silicon region, local peak fields occur along the silicon surface close to the left-side of the STI edge, in the bulk region at lateral junction J_1, and also in vertical junction J_2, whereas in gate oxide (GOX), peak field occurs close to the left-side of the STI edge. These peak locations are marked along the cutlines in Fig. 10(a). Fig. 10(b) compares peak fields along four different cutlines in silicon and GOX regions for different devices. The variations in peak field values are a result of differences in their doping concentration profiles and V_{DS} at $V_{GS} = 0$ V and $I_D = -0.1$ μA/μm, which affect their field distributions in different junctions in silicon and GOX. Since peak field in GOX (that occurs close to the left-side of the STI edge) is below 2.6 MV/cm, GOX reliability is not much of an issue. Peak fields that occur along silicon surface (cutline $X2$) closely follow the variations of peak fields at the lateral junction J_1.

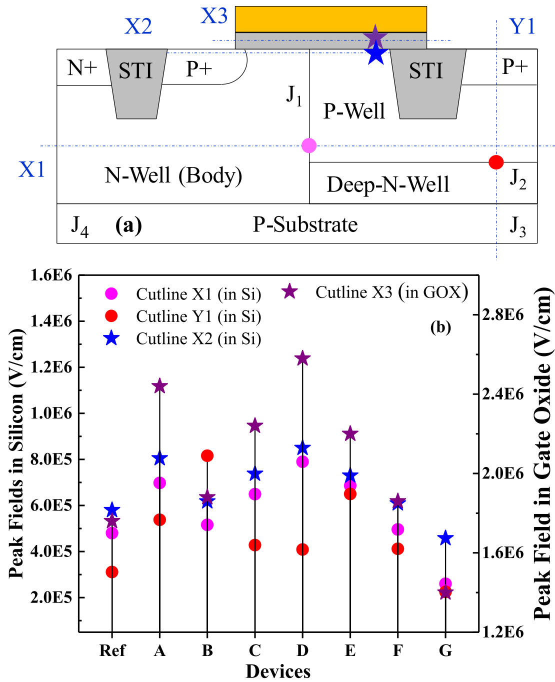

Fig. 10. (a) Cross section of STI-DePMOS showing locations of 1) vertical cutline $Y1$ through the middle of the drain diffusion region, 2) lateral cutline $X1$ at 0.5-μm depth below the silicon surface, 3) lateral cutline $X2$ at 1-nm depth below the silicon surface, and 4) lateral cutline $X3$ through the middle of GOX. Markers represent peak field spots. (b) Comparison of peak electric fields (V/cm) along different cutlines [shown in (a)] for different STI-DePMOS devices at $V_{GS} = 0$ V and $I_D = -0.1$ μA/μm. Fields across n-well (body)/p-substrate junction J_4 are comparatively negligible.

As shown in Fig. 11, field distribution around junction J_2 along the vertical cutline $Y1$ for devices B and E have relatively high peak field and less field spreading in their deep-n-well layers compared with other devices, which is determined by their junction depths J_2 and J_3 and doping profiles on either side of junction J_2. Devices with punch-through show high field spreading in their deep-n-well.

IV. Impact on Mixed-Signal Performance of STI-DePMOS Device

In this section, we compare mixed-signal performance of the modified STI-DePMOS devices having higher (improved) V_{BD} compared with the reference device. Devices A, C, D, and E have lower R_{ON}, whereas device B has higher R_{ON} compared with the reference device [Fig. 5(a)].

A. Analog and RF Performance

The analog and RF device figure of merits and small-signal capacitance–voltage (C–V) characteristics are illustrated

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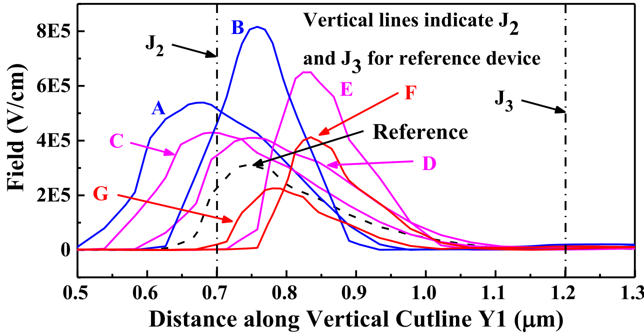

Fig. 11. Electric field (V/cm) distribution along the vertical cutline $Y1$ [shown in Fig. 10(a)] at $V_{GS} = 0$ V and $I_D = -0.1$ μA/μm in the reference device and devices A–G. The field at p^+/p-well interface is much smaller than at junction J_2. Device A has a relatively low peak field and less field spreading in its deep-n-well layer.

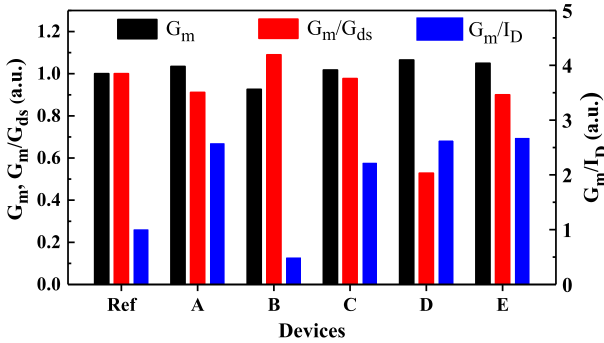

Fig. 12. Left: Peak transconductance (G_m) at $V_{DS} = -5$ V, and intrinsic transistor voltage gain (G_m/G_{ds}) (dB) at gate overdrive voltage $|V_{GS}| - |V_T| = 0.1$ V at $V_{DS} = -5$ V. Right: transconductance per unit drain current (G_m/I_D) at $V_{DS} = -5$ V are compared for different devices. The values are normalized with respect to those of the reference device.

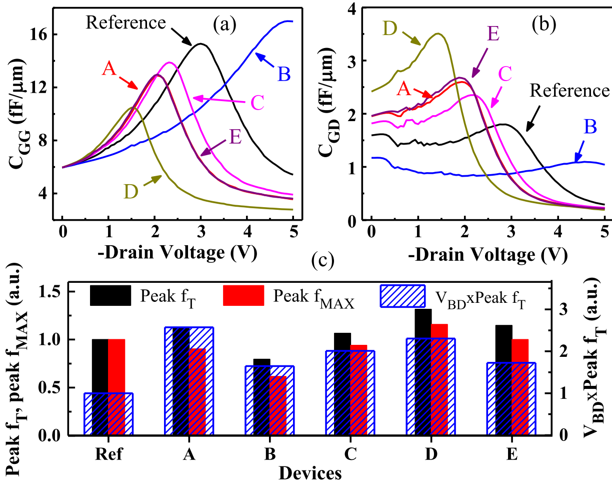

Fig. 13. (a) C_{GG}–V_D and (b) C_{GD}–V_D plots at $V_{GS} = -1.2$ V for different devices. (c) Comparison of peak intrinsic cutoff frequency (f_T), peak intrinsic maximum oscillation frequency (f_{MAX}) (at $V_{DS} = -5$ V and $|V_{GS}| > |V_T|$) (on the left y-axis), and the product $V_{BD} \times$ peak-f_T (on the right y-axis) for different devices.

in Figs. 12 and 13. As shown in Fig. 12, peak transconductance (G_m) and transconductance per unit drain current (G_m/I_D) (transconductance efficiency) at $V_{DS} = -5$ V are higher for devices with lower R_{ON} relative to other devices. However, intrinsic transistor voltage gain (G_m/G_{ds}) at $V_{DS} = -5$ V and $|V_{GS}| - |V_T| = 0.1$ V

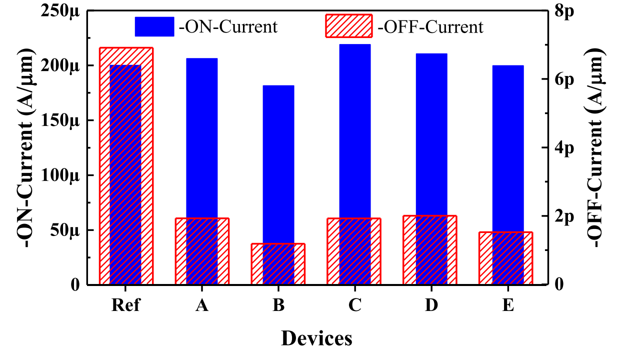

Fig. 14. Comparison of (left) ON-state drain current (I_{ON}) (at $V_{GS} = -1.2$ V and $V_{DS} = -5$ V) and (right) OFF-state drain leakage current (I_{OFF}) (at $V_{GS} = 0$ V and $V_{DS} = -5$ V) for different devices. Device B with maximum R_{ON} has minimum I_{ON} and I_{OFF}.

slightly improves for devices with higher R_{ON}, because output ac conductance G_{ds} is less for higher R_{ON}.

It is worth studying gate capacitance (C_{GG}) and gate-to-drain overlap capacitance (C_{GD}) versus drain voltage curves at $V_{GS} = -1.2$ V, for different values of p-well doping [Fig. 13(a) and (b)]. The peaking of C_{GG} and C_{GD} values at different V_{DS} values for different devices and the magnitude of the peak values are determined by the spreading of hole charge under gate-to-p-well overlap region in response to the applied small-signal voltage at gate and drain, respectively. Lower p-well doping shifts capacitance peaking to higher drain voltages. The maximum C_{GD} becomes slightly higher for device D with higher p-well doping. The peak C_{GG} (C_{GD}) increases (decreases) monotonically from device D with minimum R_{ON} to device B with maximum R_{ON}. To compare RF performance, both intrinsic cutoff frequency (f_T) (frequency at unity current gain point) and maximum oscillation frequency (f_{MAX}) (frequency at which Mason's unilateral power gain is unity) are extracted from small-signal ac device simulations [8] of STI-DePMOS devices for a fixed V_{DS} bias of $V_{DS} = -5$ V and a variable V_{GS} bias with $|V_{GS}| > |V_T|$. Each device shows a peak in f_T and f_{MAX} for $|V_{GS}| > |V_T|$, and these peak values are compared in Fig. 13(c). Difference in the relative ratio of peak f_T and f_{MAX} for different devices is due to differences in their G_m, C_{GG}, and C_{GD} characteristics in the saturation region. Both peak f_T and f_{MAX} degrade for device B with higher R_{ON} because of its reduced peak G_m and higher C_{GG} relative to the reference device. Highest peak f_T and f_{MAX} occur for device D with minimum R_{ON} because of its maximum G_m and lowest C_{GG}. In addition, Fig. 13(c) shows that device A with maximum V_{BD}/R_{ON} has the highest figure of merit for mixed-signal performance parameter of $V_{BD} \times$ peak-f_T.

B. Digital Performance

In addition to analog and RF applications, DeMOS devices are used as high-voltage switches in I/O buffers, voltage level shifters, dc-to-dc converters, and other mixed-signal circuits. Figs. 14–16 compare the digital performance of different STI-DePMOS devices.

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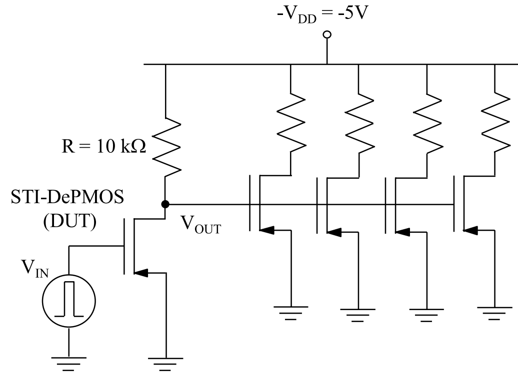

Fig. 15. Schematic of a fanout-of-4 (FO4) inverter used to compute FO4 delay. Source, body, and substrate terminals are grounded.

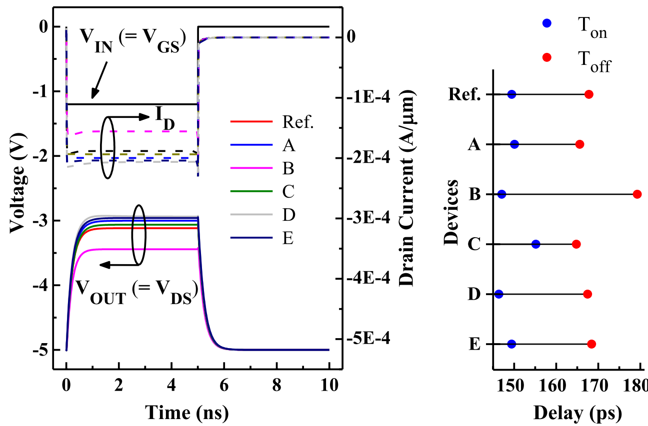

Fig. 16. Left: input gate voltage V_{IN} ($=V_{GS}$), output drain voltage V_{OUT} ($=V_{DS}$) (left y-axis), and output drain current (I_D) (right y-axis) waveforms of different devices under fanout-of-4 inverter test circuit. Right: comparison of turn-ON and turn-OFF propagation (FO4) delays (T_{ON} and T_{OFF}) of FO4 inverter with different devices.

Fig. 14 shows a slightly improved OFF-state leakage current (I_{OFF}) at $V_{GS} = 0$ V and $V_{DS} = -5$ V for the modified devices A–E, which is due to their higher V_{BD}. In addition, the ON-state drive current (I_{ON}) at $V_{GS} = -1.2$ V and $V_{DS} = -5$ V, and I_{OFF} are minimum for device B with maximum R_{ON}. To compare the switching (transient) performance of the devices with different doping profiles, they are biased in a fanout-of-4 inverter test circuit with $R = 10$ kΩ (Fig. 15). A square pulse of 10-ns width, 10-ps rise/fall time, and -1.2 V amplitude is applied to the gate of the device-under-test (DUT). Output drain voltage (V_{DS}) and drain current (I_D) waveforms of the DUT are shown in Fig. 16. Turn-ON and turn-OFF propagation delays (T_{ON}, T_{OFF}) are calculated as differences between 50% time points in gate and drain voltage transitions during turn-ON and turn-OFF events, respectively. The different values of T_{ON} and T_{OFF} for different devices (Fig. 16) occur due to their different I_{ON} values (Fig. 14) and capacitance characteristics (Fig. 13), which reflect the alterations in the p-well doping concentration profiles. As shown in Fig. 16, the turn-ON delay (T_{ON}) (which depends on the formation of inversion channel in n-well) is relatively low for devices B and D, despite their differences in R_{ON}. This is because of lower I_{DSAT} and V_{DSAT} and slower charging rate for device B compared with device D. The turn-OFF delay (T_{OFF}) (which depends on removal of hole charge from channel and drift regions) is relatively high for device B because of its low I_{ON} and high $C_{GG,peak}$.

TABLE II

SUMMARY OF DIFFERENT WELL DOPING PROFILES AND IMPACT ON PERFORMANCE OF STI-DePMOS DEVICES

Device	P-Well Conditions	Deep-N-Well Conditions	Device Performance
A	$R_{sh,PW}$ -	W_{DNW} ↑, $R_{sh,DNW}$ ↓	V_{BD} ↑, R_{ON} ↓
C	$R_{sh,PW}$ -	W_{DNW} ↑, $R_{sh,DNW}$ ↓	Analog/digital
D	$R_{sh,PW}$ ↓	W_{DNW} ↓, $R_{sh,DNW}$ ↓	FOM improve
E	$R_{sh,PW}$ ↓	W_{DNW} ↑, $R_{sh,DNW}$ ↓	
B	$R_{sh,PW}$ ↑	W_{DNW} ↑↑, $R_{sh,DNW}$ ↓↓	V_{BD} ↑, R_{ON} ↑ Analog/digital FOM degrade
F	$R_{sh,PW}$ ↓	W_{DNW} ↑, $R_{sh,DNW}$ -	V_{BD} ↓, R_{ON} ↓
G	$R_{sh,PW}$ ↑	W_{DNW} ↓, $R_{sh,DNW}$ ↑	V_{BD} ↓, R_{ON} ↑

The width W_{DNW} of deep-*n*-well layer is difference between junction depths X_{J3} and X_{J2} (shown in Fig. 3(a)). The symbol ↑ means increase, ↑↑ greater increase, ↓ decrease, ↓↓ greater decrease and - means no significant change. Analog and digital performance figure-of-merits (FOM) are compared for devices *A*-*E* with higher breakdown voltage, and not for devices *F*-*G*.

TABLE III

PERCENTAGE CHANGES IN FIGURE OF MERITS OF MODIFIED STI-DeNMOS DEVICES COMPARED WITH THE REFERENCE DEVICE

Figure-of-merit	Percentage change (%) for type *A*	Percentage change (%) for type *D*
V_{BD} (V_{DS} at $V_{GS} = 0$ V, $I_D = 0.1$ nA/µm)	-4 ↓	-10.6 ↓
R_{ON} (at $V_{DS} = 0.1$ V)	+5.5 ↑	13.6 ↑
V_{BD}/R_{ON}	-9 ↓	-21.3 ↓
V_T (at $V_{DS} = 0.1$ V)	-0.1 ↓	-0.9 ↓
Peak G_m (at $V_{DS} = 5$ V)	-2.8 ↓	-6.1 ↓
G_m/I_D (at $V_{DS} = 5$ V and $V_{GS} - V_T = 0.1$ V)	+1.3 ↑	-3.1 ↓
G_m/G_{DS} (dB) (at $V_{DS} =$ 5 V, $V_{GS} - V_T = 0.1$V)	+6.4 ↑	11.9 ↑
Peak f_T (at $V_{DS} = 5$ V)	-6.5 ↓	-10.1 ↓
Peak f_{MAX} (at V_{DS}=5V)	-27 ↓	-10 ↓
I_{ON} (at $V_{DS} = 5$ V)	-6 ↓	-10.3 ↓
I_{OFF} (at $V_{DS} = 5$ V)	-6.5 ↓	-15.9 ↓
Turn-on-delay (T_{on})	+2.2 ↑	+1.92 ↑
Turn-off-delay (T_{off})	+0.34 ↑	-1.35 ↓

Reference STI-DeNMOS is simulated with the reference process flow, whereas modified STI-DeNMOS devices with doping profile of types *A* and *D* as used for *p*-well and deep-*n*-well in STI-DePMOS devices (in Section III). For delay calculations, same FO4 inverter test circuit (Fig. 15) with voltages of inverted polarity is used (source, body and substrate terminals are grounded).

Table II highlights the variation of sheet resistance of p-well ($R_{sh,PW}$) and deep-n-well ($R_{sh,DNW}$) and the width of deep-n-well (W_{DNW}) for the devices investigated in this paper (Section III). Table II also shows the impact of these variations on the device performance with respect to the reference device.

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V. Impact on Performance of STI-DeNMOS Device

In Section III, it was shown that the STI-DePMOS devices A and D have the highest $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ ratio and minimum R_{ON}, respectively, compared with other devices (Fig. 5). Since the same process steps are also used for p-well (body) and deep-n-well in STI-DeNMOS in a triple-well CMOS technology [Fig. 1(a)], we investigate the impact of using the well doping profile of STI-DePMOS devices A and D on breakdown and mixed-signal performance of STI-DeNMOS, keeping the doping profile in n-well (drift region of STI-DeNMOS) unchanged. Table III shows that V_{BD}, R_{ON}, $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ ratio, I_{ON}, peak G_m, G_m/I_D, peak f_T and f_{MAX}, and propagation delays slightly degrade, whereas I_{OFF} and G_m/G_{ds} improve for the modified devices. The percentage changes in the performance parameters are results of variation in 2-D doping profiles at n-well/p-well junction J_1 in the modified STI-DeNMOS devices that affects the distributions of fields, current density, and carrier density in OFF- and ON-states. Though the best doping profiles (among the profiles investigated in Section III) for STI-DePMOS device affect the performance of STI-DeNMOS devices, the improvement in the performance and SOA of STI-DePMOS device (type A) far outweighs the marginal degradation in the performance of the modified STI-DeNMOS devices.

VI. Conclusion

We have found different ways to tune the OFF-state breakdown voltage and ON-state resistance in STI-DePMOS devices that are implemented in the triple-well CMOS process technology. By increasing the average doping concentration (by enough amount) in the deep-n-well layer, we could avoid the punch-through-induced vertical breakdown, thereby removing the two-stage breakdown behavior. In addition, by slightly increasing the average doping concentration in the deep-n-well layer, we could shift the onset of the first-stage breakdown to a higher drain voltage, thereby offering higher breakdown voltage than the reference device (Section II). Based on the detailed TCAD analyses, we concluded that the best device with the maximum $V_{\mathrm{BD}}/R_{\mathrm{ON}}$ ratio can be designed by moderately increasing the width and average doping concentration of the deep-n-well layer. This design generates a peak II hot spot at the lateral n-well/p-well junction, as for the conventional avalanche breakdown in STI-DeNMOS, and hence, it achieves a wider SOA for high-voltage operation. For high-voltage, high-speed, mixed-signal circuits, such as voltage level shifters, dc-to-dc converters, and envelope tracking power amplifiers using I/O devices, mixed-signal performance must also be optimized. Mixed-signal device performance could be improved for devices with relatively higher average doping concentration in the p-well, which have lower ON-state resistance and parasitic capacitances. In order to allow both n- and p-type STI-DeMOS devices made using the triple-well CMOS technology to enjoy maximum SOA and offer high mixed-signal performance, TCAD-based process technology optimization must be performed. The work in this paper gives valuable insights into ways to achieve these goals.

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