On the Geometrically Dependent Quasi-Saturation and g_m Reduction in Advanced DeMOS Transistors

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***Abstract*— This paper reveals an early quasi-saturation (QS) effect attributed to the geometrical parameters in shallow trench isolation-type drain-extended MOS (STI-DeMOS) transistors in advanced CMOS technologies. The quasi-saturation effect leads to serious g_m reduction in STI-DeMOS. This paper investigates the nonlinear resistive behavior of the drain-extended region and its impact on the particular behavior of the STI-DeMOS transistor. In difference to vertical DMOS or lateral DMOS structures, STI-DeMOS exhibits three distinct regions of the drain extension. A complete understanding of the physics in these regions and their impact on the QS behavior are developed in this paper. An optimization strategy is shown for an improved g_m device in a state-of-the-art 28-nm CMOS technology node.**

***Index Terms*— Drain length (DL), g_m reduction, overlap region, quasi-saturation (QS), shallow trench isolation-type drain-extended MOS (STI-DeMOS).**

I. Introduction

THE compatibility of drain-extended MOS (DeMOS)-type high-voltage (HV) devices in advanced CMOS processes facilitates low-cost manufacturing for system-on-chip and peripheral I/Os. The recent interest in DeMOS devices is toward analog and RF applications [1], [2]. However, at high drain current of DeMOS devices, lowering of the transconductance (g_m) limits the capabilities of the DeMOS devices for such applications [1]. For example, the g_m reduction affects the linearity performance of RF power amplifier by increasing the third-order harmonic distortion. It also hampers the power efficiency of an RF power amplifier as well as an audio power amplifier. Such g_m reduction behavior is often attributed to quasi-saturation (QS) effect in HV devices [3]. Therefore, understanding of the quasi-saturation effect and strategies to mitigate it is now of profound importance.

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The quasi-saturation effect, in simplified terms, is the saturation of drain current with V_{GS}, at higher gate bias without any channel pinchoff. This effect depends on the amount of potential drop in the drift region (Fig. 1), which in turns depends on various parameters related to the geometry and drift region doping profile of the HV devices. Therefore, a meticulous design strategy is needed to reduce the quasi-saturation effect in the case of a shallow trench isolation-type DeMOS (STI-DeMOS) device, due to its architectural difference from other HV devices, such as lateral DMOS (LDMOS) and vertical DMOS (VDMOS). The STI-DeMOS device has shown higher breakdown voltage compared with lightly doped drain MOS and better reliability compared with non-STI-DeMOS [1]. The difference in STI-DeMOS device as compared with other HV devices comes from an unusual current path, due to its retrograde doping profile and STI in the drift region. Hence, understanding of how this type of architecture is affecting the quasi-saturation behavior is necessary for an optimal design.

For VDMOS devices, it has been established that carrier accumulation in the drift region near the channel edge and carrier velocity saturation in the drift region occur when a critical current density is exceeded [4]. This leads to the observed quasi-saturation. In another study of quasi-saturation in VDMOS [5], the cell spacing is considered as a design parameter solely based on the characteristics of the drift region near to the channel. Other works with extensive discussion on quasi-saturation, VDMOS, and LDMOS [6]–[10] discussed the modeling aspects of quasi-saturation considering the carrier accumulation only near the channel edge in the drift region.

This paper shows that the quasi-saturation in STI-DeMOS is due to a more complex behavior occurring both in the gate overlap region near to the channel edge and the drain contact region. This is not the case for classical LDMOS or VDMOS devices. Only an accurate modeling of both drain and overlap regions (Fig. 1) and the consideration of the deep n-well region in between provide the correct picture of quasi-saturation.

This paper is organized as follows. Section II discusses the fabricated test structures, experimental setup, and technology computer-aided design (TCAD) simulation methodology. Section III investigates the cause of quasi-saturation effect and the design parameters needed to eliminate it in the case of

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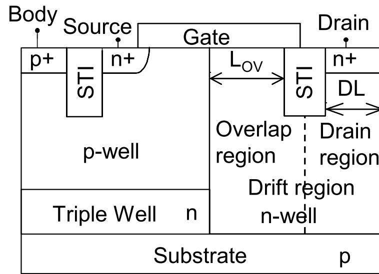

Fig. 1. STI-DeMOS device as realized in 28-nm CMOS process. The conventional device has DL = DL_{ref} and $L_{OV} = L_{OV,ref}$.

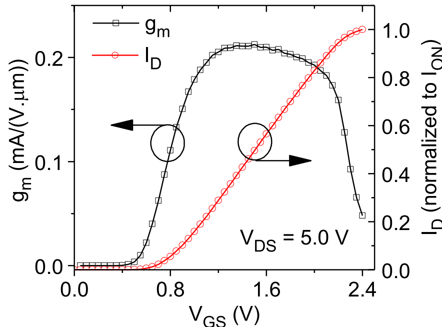

Fig. 2. Measured g_m–V_{GS} and I_D–V_{GS} behaviors for an STI-DeMOS device with DL = 1× at V_{DS} = 5 V.

STI-DeMOS transistor. Section IV validates two methods to minimize the g_m reduction with measurement results. Section V provides the conclusion.

II. Test Structure, Experimental Setup, and Simulation Setup

The state-of-the-art 28-nm technology STI-DeMOS fabricated test structures (Fig. 1) with different drain lengths (DLs) and gate-drift region overlap lengths (L_{OV}) are used in this investigation. All the devices have an oxide thickness (T_{OX}) of ~3 nm, and their gate terminates over the STI present inside the drift region. The typical values of DL and L_{OV} in sub-100-nm technologies are in the range of a few tens of nanometers to several hundreds of nanometers and 100–500 nm, respectively. The typical ON-current (I_{ON}) remains within 0.2–0.5 mA/μm.

Keithley 4200-SCS characterization system is used for the device-level characterizations. DC current–voltage (I–V) measurements are performed at room temperature. Note that the pulsed dc measurement is not considered in this paper due to the moderate current level of the devices under test at 5 V drain biasing. All the measurements are performed for three numbers of dies to obtain consistent results. Fig. 2 shows the measured g_m and I_D variation versus V_{GS} with our experimental setup for one of the devices.

Device TCAD tools [11] are used for investigating various device design parameters. The STI-DeMOS devices under investigation are built up by process simulation. In the device simulation, TCAD models are included to capture physical phenomena, such as carrier velocity saturation at high electric field, mobility reduction due to doping concentration variation, carrier–carrier scattering, and carrier recombination and generation.

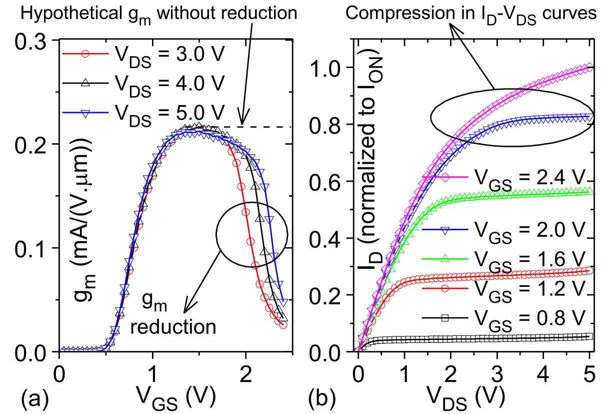

Fig. 3. (a) Measured g_m reduction with V_{GS} variation in STI-DeMOS transistor. (b) Compression in I_D–V_{DS} curves at higher V_{GS} (manifestation of QS) (measured results).

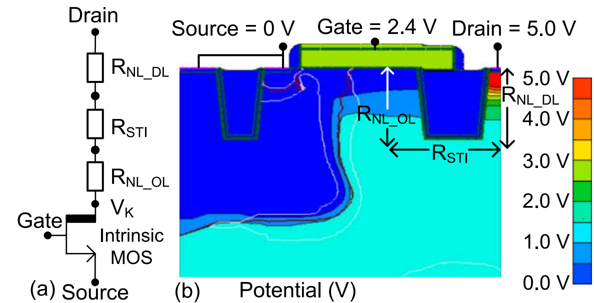

Fig. 4. (a) Simple resistive model of the drift region. (b) Potential contour plot of the conventional STI-DeMOS device when biased in the QS regime (simulation results).

III. Quasi-Saturation Effect: Cause and Minimization in an STI-DeMOS Transistor

For STI-DeMOS device, the measurement results show that g_m significantly reduces at higher V_{GS} (more than 2 V) [Fig. 3(a)]. As shown in Fig. 3(b), the g_m reduction can also be observed by the compression of I_D–V_{DS} curves as V_{GS} increases. For lower V_{GS} (less than 2 V), the drain current saturation is due to the channel pinchoff. This section focuses on the causes of quasi-saturation effect in STI-DeMOS devices and device engineering needed to address the same based on TCAD simulations.

A. Resistive Model From Quasi-Saturation Perspective

We modeled the STI-DeMOS device with an intrinsic MOS and three series resistors based on its architecture [Fig. 4(a)]. The intrinsic MOS behaves similar to a standard MOS transistor. Its drain bias is specified by the potential at the inner drain of the STI-DeMOS and is denoted by V_K in Fig. 4(a). The series resistors R_{NL_OL}, R_{NL_DL}, and R_{STI} represent the nonlinear resistance of the overlap region, the drain region, and portion under the STI of the STI-DeMOS device, respectively (Fig. 1). Modeling of the drain region as a resistor (R_{NL_DL}) is based on the observation that a considerable portion of the potential drop occurs in this region, as is evident from Fig. 4(b). This effect of drain contact region has not been observed in the classical LDMOS devices.

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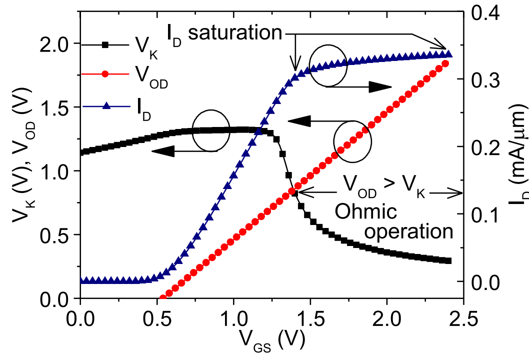

Fig. 5. V_K, V_{OD}, and I_D variations with V_{GS} for a drain bias of 5 V. The drain current saturates when the overdrive voltage ($V_{\text{OD}} = V_{\text{GS}} - V_{\text{TH}}$) is greater than the intrinsic MOS's drain voltage (V_K), indicating an ohmic operation. V_{OD} is shown only for the positive values (simulation results).

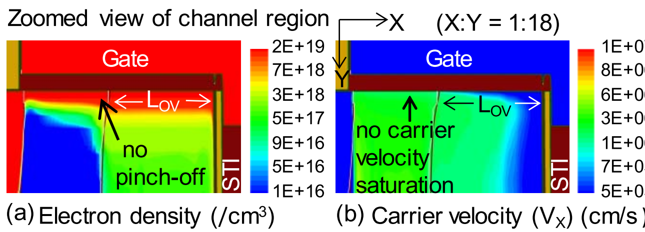

Fig. 6. Physical parameter contour plots of the conventional STI-DeMOS at $V_{\text{GS}} = 2.4$ V and $V_{\text{DS}} = 5$ V. (a) Electron density in the channel. (b) Carrier velocity (absolute value in the x-direction) in the channel (zoomed-in view of the channel is shown; y scale is zoomed 18 times more than x scale to show the entire channel) (simulation results).

B. Intrinsic MOS Operation and Quasi-Saturation Behavior

In general, for a fixed drain bias, the increase in V_{GS} increases the drain current. This causes a potential drop in the drift region, which in turn reduces V_K. This eventually drives the intrinsic MOS to the ohmic operating region. Once in the ohmic region, the drain current of MOS transistor will depend on the internal drain voltage (V_K) which is low, and hence, the sensitivity of the drain current to V_{GS} reduces. This translates to a saturation of the drain current.

Fig. 5 shows the variation of V_K with V_{GS}. When the gate overdrive (V_{OD}) for the intrinsic MOS is greater than V_K, the STI-DeMOS I_D saturates. It is worthwhile to mention that the saturation-like behavior is not due to the MOS channel pinchoff effect.

The drain current saturation in the HV device is different from that in the low-voltage standard MOS. In the standard MOS, the pinchoff of the channel leads to the drain current saturation. On the other hand, the HV STI-DeMOS shows no sign of the channel pinchoff during quasi-saturation. A zoomed-in view of the channel region in an STI-DeMOS device is shown in Fig. 6. There is no indication of pinchoff effect or velocity saturation in the channel.

C. Characteristics of the Drain Region Resistance R_{NL_DL}, the Overlap Region Resistance R_{NL_OL}, and Under the STI Region Resistance R_{STI}

The drift region n-well of the STI-DeMOS device has a retrograde doping profile to obtain a high breakdown voltage [1]. Due to this, n^{++}–n–n^+ and n^+–n–n^+ structures are formed in both drain and overlap regions, respectively [Fig. 7(a)]. We observed high electric fields in the drain region at n^{++}–n–n^+ structure of STI-DeMOS device [Fig. 7(b)]. A nonlinear I–V relation of $R_{\text{NL_DL}}$ is observed from Fig. 8, which indicates that the potential drop in this region is not a simple ohmic drop. A further investigation shows that the high electric field in the n^{++}–n–n^+ structure of the drain region is associated with carrier velocity saturation and space charge accumulation [Figs. 7(b) and 9]. The carriers are observed to be accumulated in the lowly doped n-region. These are usually observed in the drift region near the channel edge for the classical HV devices. A large fall in potential in Fig. 9 indicates a large potential drop in the lowly doped n-region.

The physical phenomenon in $R_{\text{NL_DL}}$ has resemblance with the phenomena occurring in the drift region as explained in [4]. The maximum current (henceforth called critical current) through the drift region at the boundary of carrier velocity saturation is given by [4]

$$I_C = qAnV_{\text{sat}} \quad (1)$$

where q is the electronic charge, A is the area, n is the carrier concentration ($=N_d$), and V_{sat} is the saturation velocity of

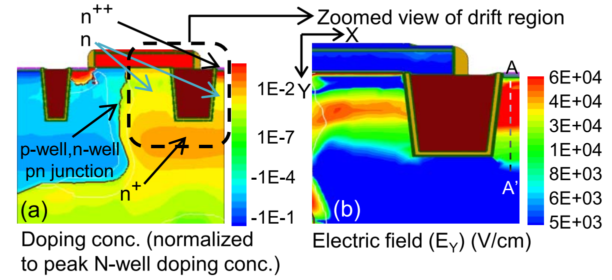

Fig. 7. (a) n^{++}–n–n^+ high–low homojunctions that define the resistances $R_{\text{NL_OL}}$ and $R_{\text{NL_DL}}$, respectively. (b) Zoomed-in view of the drift region showing electric field (absolute value in y-direction) plot when the conventional STI-DeMOS device is biased at the QS regime, i.e., $V_{\text{GS}} = 2.4$ V and $V_{\text{DS}} = 5$ V (simulation results).

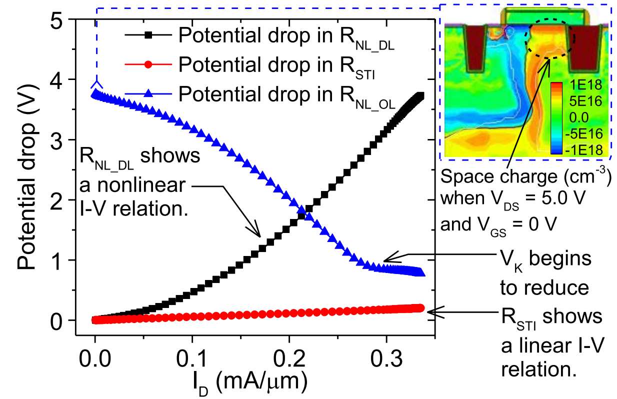

Fig. 8. I–V relation for the drain region resistance $R_{\text{NL_DL}}$, under the STI region resistance R_{STI} and the overlap resistance $R_{\text{NL_OL}}$ for V_{GS} variation from 0 to 2.4 V at $V_{\text{DS}} = 5$ V. An initial potential drop in $R_{\text{NL_OL}}$ is due to the depletion space charge formed under the gate in the overlap region for a high (5 V) drain bias, which diminishes as the current flows through it when V_{GS} increases (simulation results).

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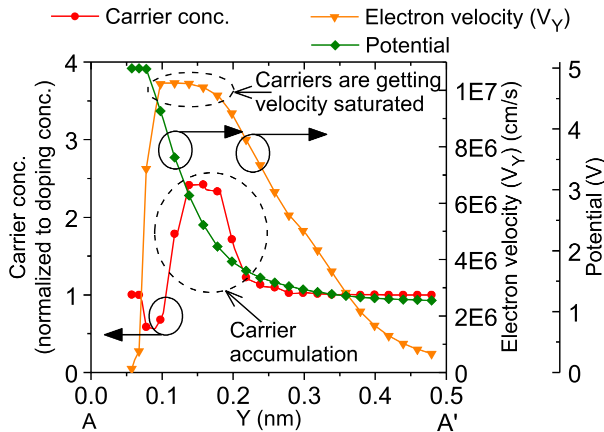

Fig. 9. Vertical cross section across the drain region [A–A′ in Fig. 7(b)] showing carrier accumulation and high potential drop when carrier velocity gets saturated. The device is biased at the QS regime, i.e., $V_{GS} = 2.4$ V and $V_{DS} = 5$ V (simulation results).

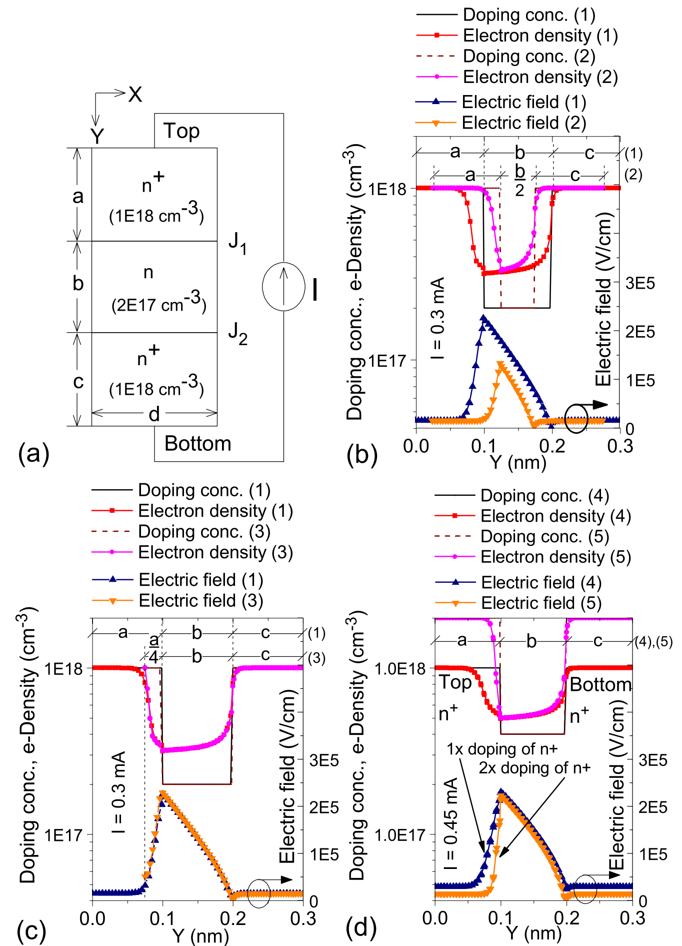

Fig. 10. (a) Idealized n^+–n–n^+ structure. Doping concentration, electron density, and electric field across a vertical cross section taken in the middle of n^+–n–n^+ structure. (b) n-region depth variation. (c) n^+-region depth variation. (d) n^+-region doping variation. The number in the parenthesis of the legend indicates the experiment number. This needs to be read in conjunction with Table I (simulation results).

the carriers. The carrier velocity gets saturated for a higher applied bias when $I > I_C$, and n becomes greater than N_d. Thus, for an n^{++}–n–n^+ structure, at higher applied bias when the drain current exceeds the critical current limit, the n-region gets flooded with excess carriers. These excess carriers give rise to a high electric field and, hence, a higher potential drop in this region. This potential drop is additional to the ohmic potential drop.

We observed that, though the physical phenomena in the case of R_{NL_OL} is similar to that of R_{NL_DL}, these phenomena can be observed prominently when overlap length, L_{OV}, is scaled aggressively to reduce the transistor footprint. For an identical length of L_{OV} and DL, R_{NL_OL} will show a higher potential drop than R_{NL_DL} due to two reasons. First, the effective length of overlap region is smaller due to the p-well–n-well p-n junction on its left. Second, the lowly doped portion of the overlap region has a lower doping as compared with the lowly doped portion of the drain region. The dopants in the overlap region diffuse to its left during thermal annealing, whereas dopant diffusion in the drain region is blocked by the STI. Thus, the critical current is lower in the overlap region than in the drain region, populating more number of carriers and, hence, dropping more potential there.

We found that R_{STI} is ohmic and depends on the sheet resistance of the drift region under the STI and, hence, is a function of STI width. Its linear I–V relation is shown in Fig. 8.

The onset of the quasi-saturation with different values of V_{DS} can be observed from the I_D–V_{GS} or g_m–V_{GS} plot. Fig. 3(a) shows that the higher the V_{DS}, the higher is the V_{GS} at which the fall of g_m curve occurs. Since quasi-saturation is caused by the near V_{DS} potential drop in the drift region, for higher V_{DS}, higher amount of potential is needed to be dropped in the drift region. This needs higher drain current. Hence, the onset of quasi-saturation for higher V_{DS} occurs at higher V_{GS}. At lower V_{DS}, even the ohmic drop in the drift region can cause V_K to fall below the overdrive voltage, and the drain current saturates.

D. Selection of Device Geometry Parameters Significant to Quasi-Saturation—Understanding Through an Idealized n^+–n–n^+ Structure

An idealized n^+–n–n^+ structure [Fig. 10(a)] is considered, its geometrical and doping parameters are varied, and their effect on the I–V relationship is analyzed in a condition similar to that in the overlap as well as the drain region during quasi-saturation. Doping of n^+- and n-regions, depths of these regions [i.e., a and b in Fig. 10(a)], and width d of the n^+–n–n^+ structure are varied. The conditions for lowest potential drop are obtained across the entire structure for a current more than the critical current. We found that the crucial parameters needed to be optimized to reduce the potential drop are: 1) the n-region depth; 2) the n-region doping; 3) the top n^+-region doping; and 4) the width of the n^+–n–n^+ structure. The details of the simulation experiment and explanation of I–V behavior, based on which the crucial parameters are selected, are given in the following Sections III-D-1 and III-D-2.

1) Details of Simulation Experiment With the n^+–n–n^+ Structure: A carefully chosen set of experiments are

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TABLE I
POTENTIAL DROP ACROSS THE ENTIRE IDEALIZED STRUCTURE AND CALCULATED I_C FOR A SET OF EXPERIMENTS (SIMULATION)

Expt. #	Experiments	I_C (mA)	Potential drop (V)
1.	n^+ - n - n^+ (1E18-2E17-1E18); a=b=c	0.2	1.3
2.	n^+ - n - n^+ (1E18-2E17-1E18); a=c, b/2	0.2	0.4
3.	n^+ - n - n^+ (1E18-2E17-1E18); b=c, a/4	0.2	1.3
4.	n^+ - n - n^+ (1E18-4E17-1E18); a=b=c	0.4	1.6
5.	n^+ - n - n^+ (2E18-4E17-2E18); a=b=c	0.4	1.2
6.	n^+ - n - n^+ (1E18-2E17-1E18); a=b=c, 2×d	0.4	0.6

performed with different dopings and dimensions. A current source is used to provide the bias, and the resulting potential drops across the entire structure are shown in Table I. The ohmic potential drops are subtracted in order to consider the potential drops only due to high electric fields in Table I. The potential drops are considered at current biases that are reasonably higher than the respective critical currents and are mentioned for each experiment in Fig. 10. For the same bias current, the lowest potential drop across this structure is the most desired situation in an analogy to the reducing potential drop in the drain region or overlap region for attenuating the quasi-saturation.

2) I–V Behavior Explanation With Geometrical and Doping Parameter Variation: Table I shows the list of performed simulation experiments on the n^+–n–n^+ structure under test. Expt. 1 and Expt. 2 are designed to study the effect of reducing the n-region depth, i.e., b. In Expt. 2, the potential drop across the entire structure is lower compared with Expt. 1 (Table I) for two reasons. First, for $I > I_C$, due to the lower depth $b/2$, the electric field extends to a smaller region as compared with Expt. 1. In addition, the peak electric field is also less in Expt. 2 [Fig. 10(b)]. Hence, the potential drop is less. Second, the high-low junction causes the carriers to diffuse from highly doped region to lowly doped region. Keeping the depth of the lowly doped region small enough, high carrier density ($n > N_d$) is observed in the entire n-region. Thus, it has higher critical current than the calculated one ($I_C > qAnV_{\text{sat}}$ as $n > N_d$), resulting in a lower potential drop.

The effect of reducing the top n^+-region depth, i.e., a, is evaluated in Expt. 3. The n^+–n–n^+ structure has a reverse biased junction (J_1) and forward biased junction (J_2) [Fig. 10(a)]. Hence, for $I > I_C$, the top n^+-region is depleted, and the n-region is accumulated with carriers. For a shorter depth ($a/4$) of the top n^+-region, the depletion region extends to the entire depth ($a/4$), and the electric field terminates at the n^+ boundary [Fig. 10(c)]. A less potential drop is expected in Expt. 3 as compared with Expt. 1. However, except for some unreasonably high bias, this effect is not apparent. The potential drop in both Expt. 1 and Expt. 3 is the same (Table I).

The effect of increasing the doping of top and bottom n^+-region is assessed in Expt. 4 and Expt. 5. In Expt. 5, both the n^+-regions have twice the doping concentration compared with Expt. 4. For $I > I_C$, the depletion in the top n^+-region (J_1 being reverse biased) extends to a less depth in Expt. 5 as compared with Expt. 4 [Fig. 10(d)]. Hence, less potential drop is observed in Expt. 5 (Table I). Bottom n^+-region's doping has no significant effect on the potential drop as J_2 is forward biased.

TABLE II
OPTIMIZATION PARAMETERS FOR STI-DeMOS DEVICE TO REDUCE QS

Sr. No.	Parameters	Short notation
1.	Length of the drain region	DL
2.	Length of overlap region	L_{OV}
3.	Depth of lowly doped portion (n-region) in both drain and overlap regions	n_H
4.	Doping concentration of lowly doped portion (n-region) in both DL and overlap regions	n_{dop}
5.	Doping concentration of the n^+-region in the overlap region	n^+_{dop}

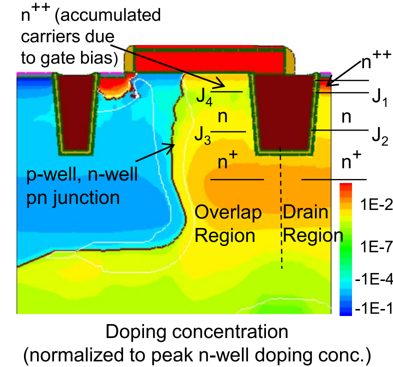

Fig. 11. n^{++}–n–n^+ structure in drain and overlap regions. Under usual operating condition, junctions J_1 and J_3 are reverse biased and J_2 and J_4 are forward biased (simulation results).

The effect of increasing the width d is evaluated in Expt. 6. Doubling d, the critical current in Expt. 6 becomes twice compared with Expt. 1 (both experiments have identical doping profile). Hence, the potential drop is lower in Expt. 6 compared with Expt. 1 (Table I). This is valid for any bias condition, though the results are shown for $I = 0.45$ mA in Expt. 6 and $I = 0.3$ mA in Expt. 1. Forcing $I = 0.45$ mA is impractical for Expt. 1.

In the next section III-E, the crucial parameters obtained from the above discussion are extended to the STI-DeMOS device parameters, and the design guidelines are elucidated.

E. Effect of Device Geometry on the Quasi-Saturation of STI-DeMOS Device

From the understanding of n^+–n–n^+ structure, we suggest a set of parameters for the optimization of DeMOS device, as shown in Table II.

With the applied drain bias, J_1 and J_3 are reverse biased (Fig. 11). Thus, the doping concentration of n^{++}-region in the drain region (n^{++}_{dop}) and n^+-region in the overlap region (n^+_{dop}) are also the optimization parameters. However, n^{++}-region, being the drain contact is heavily doped and is unaltered. The other two junctions J_2 and J_4 are forward biased with applied drain bias.

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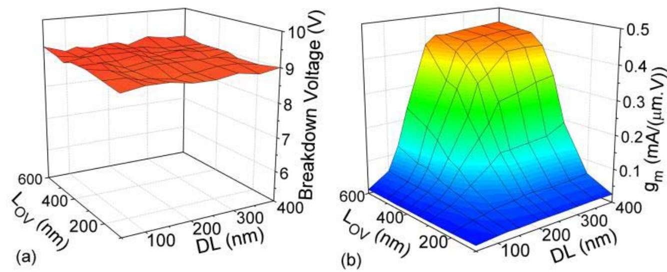

Fig. 12. (a) Breakdown voltage and (b) g_m (calculated at $V_{DS} = 5$ V and $V_{GS} = 2.4$ V) variation for DL and L_{OV} matrix with channel length = 200 nm (simulation results).

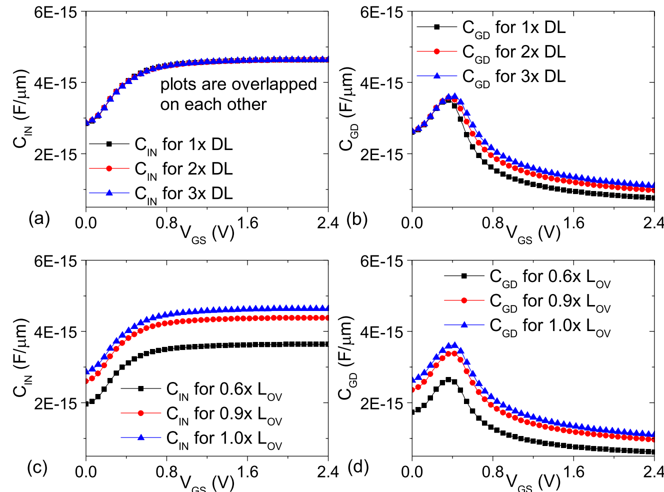

Fig. 13. STI-DeMOS device capacitances. (a) Input capacitance (C_{IN}) and (b) Gate–drain overlap capacitance (C_{GD}) for a set of DL variation (for 1 × L_{OV}); (c) Input capacitance (C_{IN}) and (d) Gate–drain overlap capacitance (C_{GD}) for a set of (L_{OV}) variation (for 3× DL) with drain and source terminals grounded (simulation results).

The DL is always designed to a lowest possible value by the device designer to reduce the transistor footprint. However, this has serious impact on g_m of the device. Increasing the DL and overlap length also reduces the quasi-saturation, but does not affect the breakdown, as shown in Fig. 12(a). This is also demonstrated with measurement results in the next section IV-C. The breakdown voltage for STI-DeMOS device depends on the electric fields at the p-well/substrate and n-well junctions, which are not affected by the increase in DL and/or L_{OV}. The g_m attains a maximum value with DL and L_{OV} when they are optimized, as shown in Fig. 12(b). Fig. 12(b) also indicates that there are optimum values of DL and L_{OV}, beyond which increasing the DL and L_{OV} only leads to higher transistor area without any g_m improvement.

The dynamic performance of the device is considered during the optimization of DL and L_{OV} for g_m improvement. Fig. 13 shows the variation of the input capacitance (C_{IN}) and gate–drain overlap capacitance (C_{GD}) with respect to the design parameters. These capacitors are considered, since they affect the cutoff frequency and switching speed of the transistor. The value of C_{IN} does not vary with DL, whereas C_{GD} slightly increases with DL in a nonlinear fashion. The increase of C_{IN} and C_{GD} with L_{OV} is as anticipated due to the increase in the gate area.

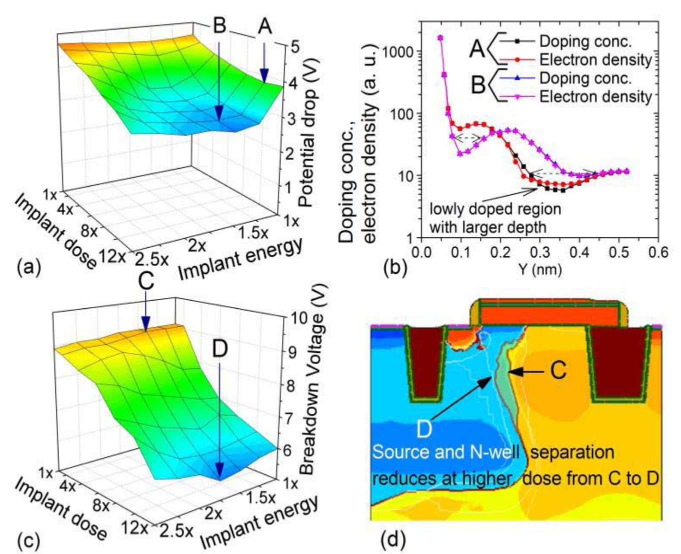

Fig. 14. Doping profile optimization of a conventional STI-DeMOS device. (a) Potential drop in the drift region (calculated at $V_{DS} = 5$ V and $V_{GS} = 2.4$ V) for a matrix of implant dose and energy. (b) Doping concentration and electron density variation in the drain region—the low implant energy as compared with the moderate implant energy. (c) V_{BD} variation in the drift region, for a matrix of n-well implant energy and dose. (d) Shifting of n-well toward the source at higher implant dose (simulation results). A lower potential drop and a higher breakdown voltage are the optimization goal.

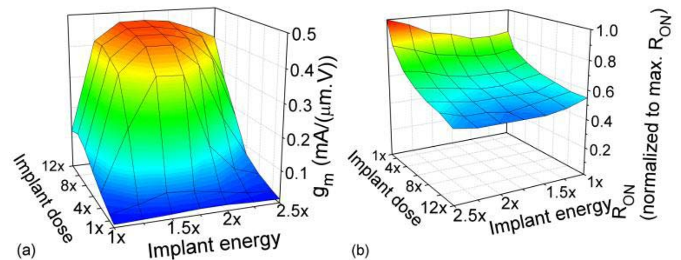

Fig. 15. (a) g_m (calculated at $V_{DS} = 5$ V and $V_{GS} = 2.4$ V) and (b) R_{ON} variations during doping profile optimization of the conventional STI-DeMOS device (simulation results).

The parameters n_H, n_{dop}, and n^+_{dop} are optimized by choosing proper dose and implant energy for the n-well. An increase in the implant dose: 1) reduces n_H; 2) increases n_{dop}; and 3) increases n^+_{dop}. As explained in Section III-D, this leads to a reduction of the carrier accumulation population, which in turn reduces the electric field and potential drop across the n^+–n–n^+ structure [Fig. 14(a)]. A decrease in the implant energy: 1) reduces the n_H and 2) increases n_{dop}. This reduces the potential drop in a similar way as in the case of increase in implant dose. However, for very low values of implant energy (less than 1.25×), an n^+-region is created below the drain n^{++}-region, and a lowly doped region with a larger depth is created in the drain region [Fig. 14(b)]. This drops a considerable amount of potential. Such behavior is insignificant for low implant doses (less than 4×).

The effect on the breakdown voltage of the STI-DeMOS device for doping profile optimization is shown in Fig. 14(c).

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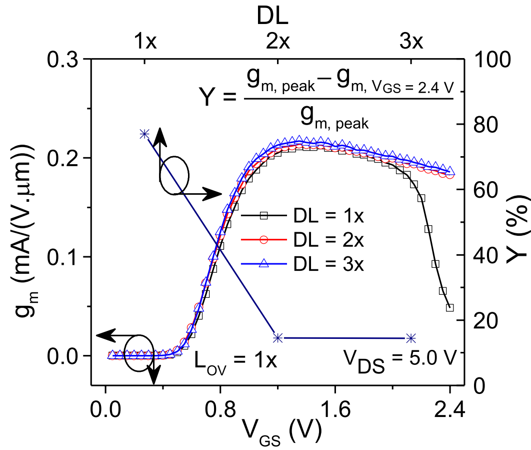

Fig. 16. Measured g_m–V_{GS} curves for a set of DL variation showing g_m improvement with the increasing DL. The percentage reduction of g_m from its peak value (Y) indicates the severity of g_m variation with DL values below 2×.

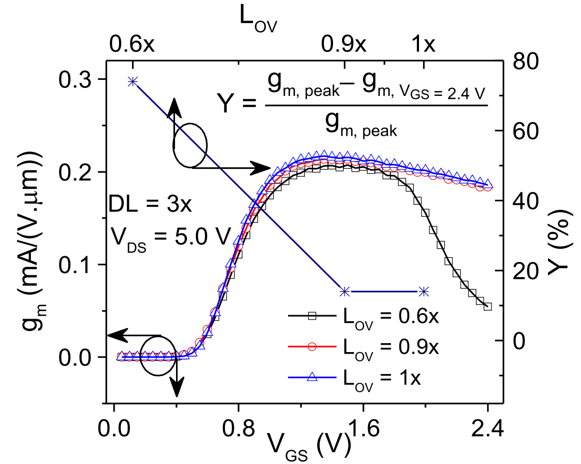

Fig. 17. Measured g_m–V_{GS} curves for a set of L_{OV} variation showing g_m improvement with the increase in L_{OV}. The percentage reduction of g_m from its peak value (Y) indicates the severity of g_m variation with L_{OV}.

At higher implant doses, the breakdown voltage of the device is severely affected. The breakdown voltage worsens both for lower implant energy and for a higher implant dose. These combinations bring the source and drain (n-well) depletion regions very close, which leads to a large source to drain leakage current reducing the breakdown voltage of the device [Fig. 14(d)]. The g_m and R_{ON} variations with doping profile optimization are shown in Fig. 15. A higher g_m and a lower R_{ON} are consistent with the lower potential drop in the drift region.

IV. Measurement Results

In the STI-DeMOS device, the drain region being served as a simple drain contact, the DL is scaled to a minimum value in order to save area. However, minimum DL has the lowest critical current that leads to a serious g_m reduction due to quasi-saturation. In this section, we show a validation of the previous TCAD optimizations with the help of experimental evidence.

A. Through Optimization of DL

We characterize the STI-DeMOS devices with three DL variations. The g_m–V_{GS} plots and the percentage of g_m reductions from its peak values are shown in Fig. 16. As shown in Fig. 16, the measured g_m reduces sharply by 77% from its peak value to g_m at V_{GS} = 2.4 V due to heavy quasi-saturation effect for 1× DL. As DL increases from 1× value, the g_m reduction weakens and becomes mere 14.5% for 2× DL. For DL values between 2× and 3×, the percentage of reduction in g_m remains ∼14%. The area penalty at 2× DL is only 4.6%.

B. Through Optimization of L_{OV}

For aggressively reduced L_{OV}, the quasi-saturation effect also becomes a function of L_{OV}. A substantial improvement in g_m reduction is observed (Fig. 17) when L_{OV} changes from 0.6× to 0.9×. Thereafter, the percentage g_m reduction remains at ∼14%. The area penalty at 0.9× L_{OV} is just 7.5%.

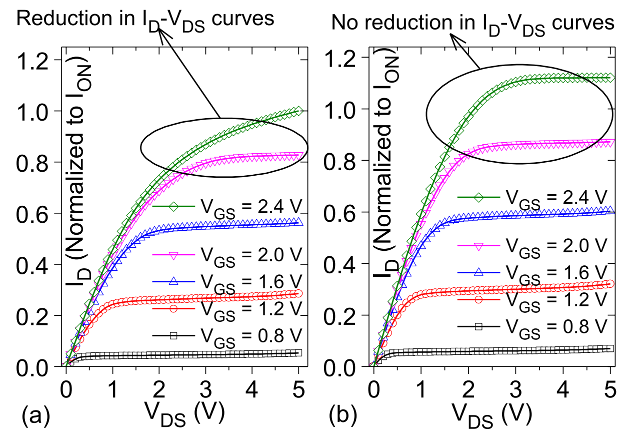

Fig. 18. Measured I_D–V_{DS} curves for STI-DeMOS device. (a) DL = 1× and L_{OV} = 1×. (b) DL = 3× and L_{OV} = 1× (improved g_m device).

The g_m improvement of the device can also be seen in the output characteristics of the device. A comparison of I_D–V_{DS} curves in Fig. 18 shows no reduction in the currents at higher V_{GS} for the improved g_m device.

C. Impact of Optimization on Figure of Merit of DeMOS

Since the junction breakdown V_{BD} is an important consideration in HV device optimization, its variation with DL and L_{OV} optimization is shown in Fig. 19. It is observed that V_{BD} is not affected by either DL or L_{OV}.

Device performance tradeoffs, such as linear drain current ($I_{D,\text{lin}}$) and R_{ON}, are shown in Fig. 20 for DL and L_{OV} optimizations. $I_{D,\text{LIN}}$ and R_{ON} are obtained at 100 mV of drain bias. The improvement in $I_{D,\text{LIN}}$ and R_{ON} is due to the reduction of ohmic resistances because of a widening of the current path with the increase in L_{OV} and DL. A figure of merit (FoM) that captures the best values of I_{ON}, R_{ON}, and V_{BD} for analog and RF application is shown in Fig. 21. With the optimization of DL and L_{OV}, the reduction of quasi-saturation boosts the ON-current. This leads to a higher FoM.

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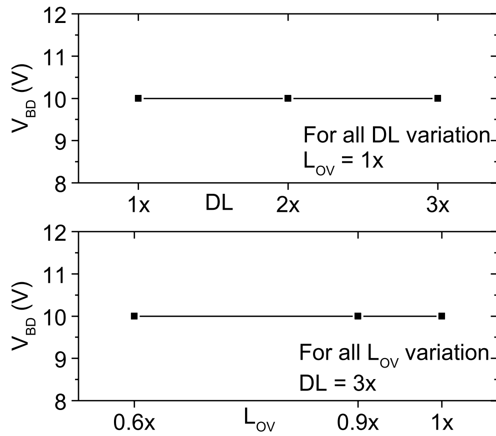

Fig. 19. Measured V_{BD} values for a set of DL and L_{OV} variations. The V_{BD} is unaffected by DL and L_{OV} variations.

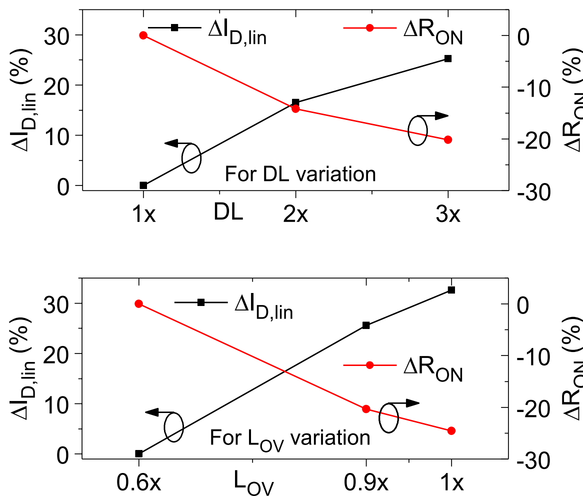

Fig. 20. Measured $I_{D,\mathrm{lin}}$ and R_{ON} for a set of DL and L_{OV} variations.

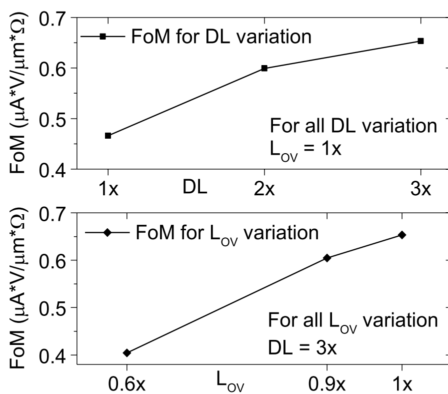

Fig. 21. Measured FoM ($=I^*_{\mathrm{ON}} V_{\mathrm{BD}}/R_{\mathrm{ON}}$) for a set of DL and L_{OV} values.

V. Conclusion

This paper demonstrates for the first time the nature and the root cause of the quasi-saturation and transconductance reduction in an STI-DeMOS device. The quasi-saturation effect is caused by ohmic operation of the intrinsic MOS channel due to near V_{DS} potential drop in the drift region. This is caused by carrier accumulation in the drift region accompanied with the carrier velocity saturation and high electric field. While this might be expected for the gate overlap region in analogy to similar devices, such as LDMOS, the STI-DeMOS shows a stronger impact on the quasi-saturation by another high electric field region underneath the drain contact. By optimizing the geometric parameters that are affecting the quasi-saturation, a three times higher transconductance could be achieved for high gate voltages in a 28-nm CMOS technology. This is required to drive the device in high-power mode for a limited time. By developing a comprehensive understanding of the physics of the drain extension region of a DeMOS, this paper provides the basis for an accurate modeling of DeMOS devices in advanced CMOS nodes.

References

[1] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part I: Mixed-signal performance of various high-voltage drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[2] M. Acar, M. P. van der Heijden, and D. M. W. Leenaerts, "0.75 Watt and 5 Watt drivers in standard 65 nm CMOS technology for high power RF applications," in *Proc. IEEE RFIC Symp.*, Montreal, QC, Canada, Jun. 2012, pp. 283–286.

[3] M. M. De Souza, P. Fioravanti, G. Cao, and D. Hinchley, "Design for reliability: The RF power LDMOSFET," *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 1, pp. 162–174, Mar. 2007.

[4] M. N. Darwish, "Study of the quasi-saturation effect in VDMOS transistors," *IEEE Trans. Electron Devices*, vol. 33, no. 11, pp. 1710–1716, Nov. 1986.

[5] J. Evans and G. Amaratunga, "The behavior of very high current density power MOSFETs," *IEEE Trans. Electron Devices*, vol. 44, no. 7, pp. 1148–1153, Jul. 1997.

[6] K. H. Lou, C. M. Liu, and J. B. Kuo, "An analytical quasi-saturation model for vertical DMOS power transistors," *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 676–679, Mar. 1993.

[7] C. Anghel *et al.*, "Physical modelling strategy for (quasi-) saturation effects in lateral DMOS transistor based on the concept of intrinsic drain voltage," in *Proc. Int. Semiconductor Conf.*, vol. 2. Oct. 2001, pp. 417–420.

[8] A. C. T. Aarts and W. J. Kloosterman, "Compact modeling of high-voltage LDMOS devices including quasi-saturation," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 897–902, Apr. 2006.

[9] L. Wang *et al.*, "Physical description of quasi-saturation and impact-ionization effects in high-voltage drain-extended MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 492–498, Mar. 2009.

[10] W. Wang, B. Tudor, X. Xi, W. Liu, and F. J. Lee, "An accurate and robust compact model for high-voltage MOS IC simulation," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 662–669, Feb. 2013.

[11] *Sentaurus Device User Guide, Version C-2009.06*, Synopsys Inc., Mountain View, CA, USA, 2009.

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