On the Improved High-Frequency Linearity of Drain Extended MOS Devices

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***Abstract*— Based upon two-tone measurements, 5dB improvement in the linearity behavior of drain extended MOS (DeMOS) device is reported by novel drain engineering. The presented modification significantly improves the device saturation characteristic, ON resistance and transconductance without affecting the breakdown behavior. Formation of IMD sweet-spot by device design is shown and verified using DeMOS devices fabricated in state-of-the-art 28nm CMOS technology. Detailed analysis towards the achieved improvement is also given.**

***Index Terms*— DeMOS, drain extended MOS device, IMD, LDMOS, Linearity, RF Power Amplifier.**

I. Introduction

RECENT growth in wireless consumer market is pushing semiconductor industry towards CMOS compatible high voltage devices for RF power applications [1]. Drain extended MOS (DeMOS) device is a potential candidate for RF power applications in advance CMOS nodes [2]. These devices sustain high voltages because of the reduced surface field (RESURF) action in the drain extension region. These devices are often designed for high power switching applications for the power management of advance system on chips (SoC) [3], [4]. However, modern wireless systems put strong restrictions on the device linearity for RF power amplifier (PA) applications. One of the reasons why commercial SoCs often do not have integrated RF PA is unacceptable linearity of DeMOS devices in advance CMOS nodes.

Linearity of a device is characterized by intermodulation distortion (IMD) measurements through two-tone test. IMD behavior of high-voltage devices and its relation to device characteristics has been analyzed by various researchers [5], [6]. However, the understanding towards device design for improved linearity has been fairly limited. In this letter, for the first time, we demonstrate that the length of drain contact can be used as a device design parameter to improve the device linearity. The design strategy is further validated through two-tone linearity measurements on fabricated RF PA in 28nm CMOS technology.

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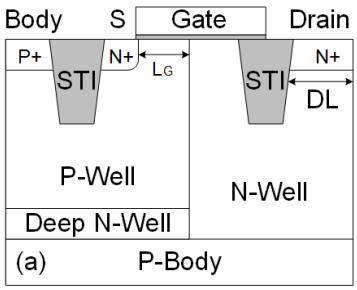

Fig. 1. Cross-section of the STI type DeNMOS device.

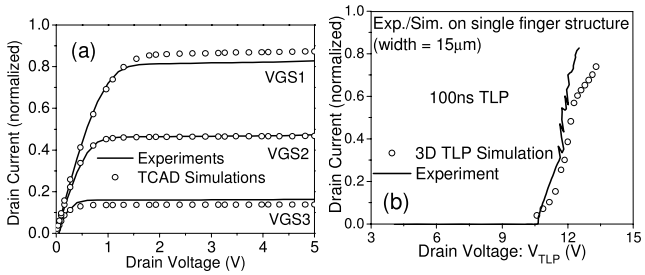

Fig. 2. (a) Mobility model calibration with quantum corrections (b) Calibration of avalanche generation and high-field velocity saturation models for high-voltage and high-current operation. Reprinted from A. Gupta et al. [10].

II. Drain Extended MOS Device Design

Recently, STI type DeMOS is shown as a potential candidate for RF PA applications [7]. This device is fully compatible with a standard CMOS fabrication process. Fig. 1 shows cross section of the conventional DeNMOS device which has a normalized drain diffusion length (DL) of minimum design rule (1×). A well calibrated Technology-CAD (TCAD) model was developed for detailed physical insight. Process and device models were calibrated using the experimental data and shown in Fig. 2. Deep well implant profiles were calibrated against secondary ion mass spectroscopy (SIMS) data. Further details on the TCAD calibration can be found in our earlier work [6]. Device I_D-V_G is plotted in Fig. 3 at V_{DS} = 5V. DL of this drain contact is generally similar to the source and body contacts in the conventional device. However, we found that

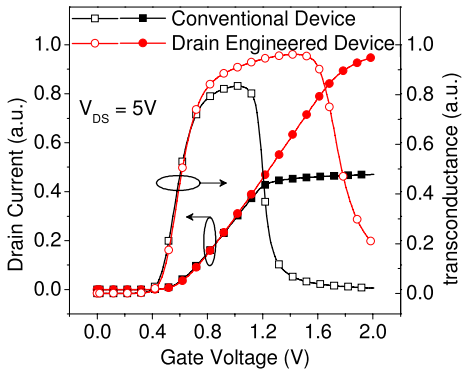

Fig. 3. Simulated I_D-V_G and g_m characteristics for conventional and drain-engineered device at $V_{DS} = 5V$.

DL needs to be carefully designed for RF applications. At high current conditions, conventional device suffers from significant space-charge modulation under drain contact region, which in turn increases the peak electric field and degrades carrier mobility. This leads to multiple quasi-saturation effects and ESD reliability issues as discussed in [7]. Because of these quasi-saturation effects, conventional device shows early compression in I_D-V_G characteristic. To mitigate this early space-charge formation, DL of drain contact was extended to 5× which leads to a drain-engineered device with improved I_D-V_G saturation and g_m characteristic as shown in Fig. 3. On-resistance (R_{ON}) of the device was measured at $V_{DS} = 0.1V$ and $V_{GS} = 2V$. Due to improved carrier mobility in case of DL= 5×, R_{ON} improves by 40%. This is discussed in detail in our earlier work [7]. Because of the retrograde doping profile used for well implants, breakdown occurs at P-Well and N-Well interface. Junction profile at this interface remains unaffected by change in the DL and hence it does not degrade the breakdown voltage (V_{BD}) of the device.

This drain engineering offers a unique insight into linearity behavior of these high-voltage devices. It is known that RF linearity depends on the combined effect of non-linear gate capacitance (C_{gg}) and third-order transconductance (g_{m3}) and it is very difficult to predict the behavior of individual terms at large-signal levels. By drain engineering, I_D-V_G characteristic at the saturation is improved without affecting C_{gg} and active channel region of the device. Therefore, the impact of only g_{m3} on the linearity can be analyzed.

Fig. 4 shows g_{m3} characteristics for conventional and drain-engineered devices. Device is biased slightly above threshold voltage (V_T) as shown in the figure to operate in class-AB mode which provides better linearity with acceptable RF gain and efficiency [6]. For small-signal conditions (ν_{g1}), contribution of g_{m3} (instantaneous area under g_{m3} which is centered at bias point) is negative as shown in Fig. 5. As the input power level increases, the gate signal traverses the expanding non-linearity of turn-on region (Fig. 4). Negative contribution gets cancelled by positive contribution of g_{m3} which makes a small-signal null in g_{m3} contribution (Fig. 5) since non-linearity due to g_{m3} depends on the area under g_{m3} curve as ν_g varies with time. This effect occurs at relatively low values of power levels and is not always observed. As the input power increases further, g_{m3} contribution remains positive until the signal reaches ν_{g2}.

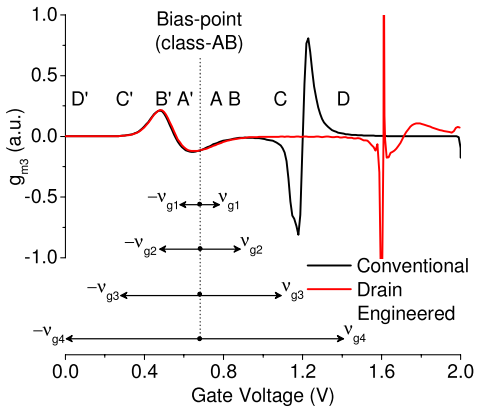

Fig. 4. Simulated third order transconductance (g_{m3}) characteristic of conventional and drain-engineered devices. Figure also shows the bias point at class-AB mode of operation along with superimposed input signals (ν_g).

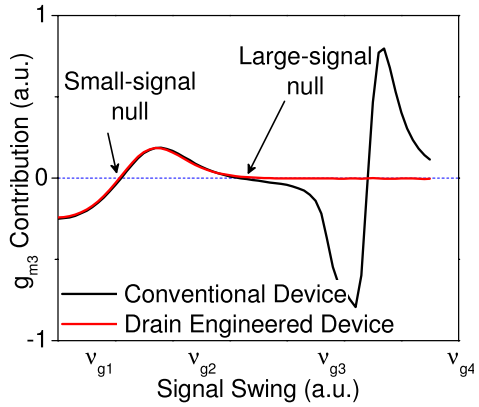

Fig. 5. Simulated gm3 contribution as a function of applied signal swing for conventional and drain-engineered devices. This is area under the gm3 curve when the starting point is centered at class-AB bias.

As the signal level increases further from ν_{g2} to ν_{g3}, strong compressive non-linearity dominates the g_{m3} contribution in case of conventional device. This causes an abrupt change of sign from positive to negative with high absolute peak value. Hence, a large-signal null in g_{m3} contribution is produced at high signal levels close to the output power compression point (Fig. 5). This abrupt nature of large-signal null in case of conventional device significantly limits the gate voltage range for which null in the g_{m3} contribution can be achieved. It is worth mentioning here that both positive and negative g_{m3} contributions result in non-linearity of the device. Only null in the g_{m3} contribution provides a linear behavior of the device.

In case of the drain-engineered device, when signal level increases from ν_{g2} to ν_{g3}, net positive g_{m3} contribution gets cancelled by small negative value over a wider range of gate voltage. This provides a null in the g_{m3} contribution over a wider range of signal swing as shown in Fig. 5. Therefore, the improved device can produce more significant large-signal null over a larger input power range compared to the conventional device.

III. On the Improved Linearity

A complete fabricated RF PA circuit (Fig. 6(a)) was used as a vehicle to study the IMD behavior of both the devices [7].

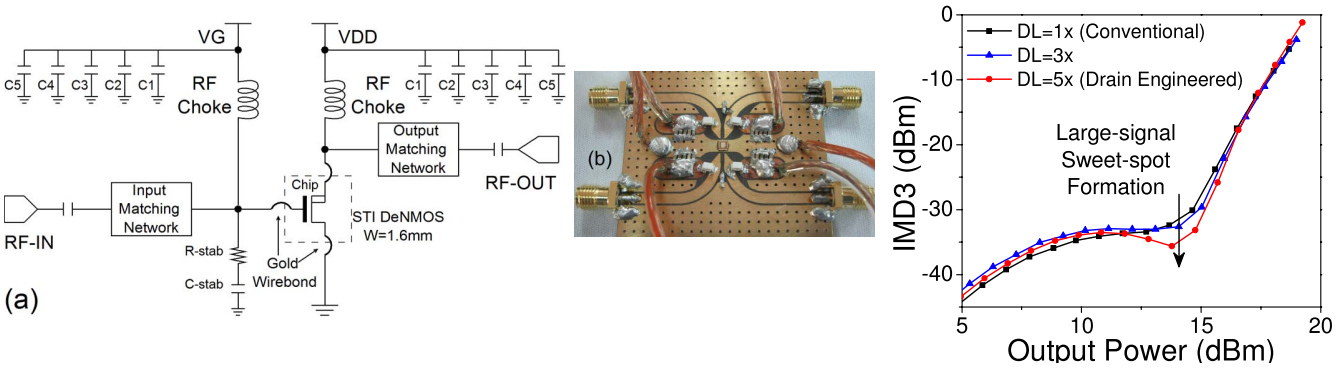

Fig. 6. (a) Circuit schematic and (b) photograph of the board level implementation of RF PA used for two-tone linearity measurements [7]. (c) Experimental IMD3 for conventional and drain-engineered devices. Measurements show a deeper and wider sweet-spot formation for drain-engineered device.

Three devices (DL = 1×, DL = 3× and DL = 5×) were fabricated in 28nm standard CMOS process with a total gate width of 1.6mm resulting in three RF PA circuits. Fig. 6(b) shows the photograph of complete fabricated RF PA on low loss laminate. Two-tone measurements were performed at center frequency of 1GHz with a tone spacing of 1MHz. For comparison, all three devices were biased at $V_{DS} = 5V$ and $V_{GS} = 0.65V$ for a class-AB mode of operation.

It is known that a null in the g_{m3} causes a minimum (sweet-spot) in the IMD3 characteristic [8]. Fig. 6(c) shows measured IMD3 (high) on RF PA in deep class-AB mode of operation. We observed that IMD3 (low) behavior is same as IMD3 (high) without any noticeable difference. For the conventional device, IMD3 power remains constant throughout the sweet-spot but does not produce a minimum. As predicted in the g_{m3} analysis for conventional device, sharp transition of positive to negative g_{m3} contribution does not produce noticeable minima in IMD3 characteristic. However, in case of drain-engineered device, g_{m3} contribution is null and hence, IMD3 distortion is less for a wider range of signal swing. Hence, it creates more pronounced local minima in the sweet-spot with ∼ 5dB (3×) lower IMD3 power compared to the conventional device. Difference in IMD3 at low output power can be correlated to 1.5dB gain improvement of the drain engineered device [7]. Various linearization techniques such as analog pre-distortion are reported to utilize IMD sweet-spot for PAs [9]. Highly linear systems can be achieved by utilizing these IMD sweet-spots efficiently.

IV. Conclusion

It is shown that drain-engineered DeMOS device achieves better and wider sweet-spot creation in IMD characteristic with ∼3× less harmonic power as compared to the conventional DeMOS device. Devices were fabricated in 28nm standard CMOS process to show the validity of the design strategy in deeply scaled technologies.

References

[1] R. Kumar et al, "A fully integrated 2 × 2 b/g and 1 × 2 a-band MIMO WLAN SoC in 45 nm CMOS for multi-radio IC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 328–329.

[2] T. Johansson and J. Fritzin, "A review of watt-level CMOS RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 1, pp. 111–124, Jan. 2014.

[3] A. Tombak, D. C. Dening, M. S. Carroll, J. Costa, and E. Spears, "High-efficiency cellular power amplifiers based on a modified LDMOS process on bulk silicon and silicon-on-insulator substrates with integrated power management circuitry," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1862–1869, Jun. 2012.

[4] T. Chang, H. L. Kao, Y. J. Chen, S. L. Liu, S. P. McAlister, and A. Chin, "A CMOS-compatible, high RF power, asymmetric-LDD MOSFET with excellent linearity," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[5] C. Fager, J. C. Pedro, N. B. De Carvalho, and H. Zirath, "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 12, pp. 2834–2842, Dec. 2002.

[6] C.-H. Choi, Z. Yu, and R. W. Dutton, "Impact of poly-gate depletion on MOS RF linearity," *IEEE Electron Device Lett.*, vol. 24, no. 5, pp. 330–332, May 2003.

[7] A. Gupta *et al.*, "Drain extended MOS device design for integrated RF PA in 28 nm CMOS with optimized FoM and ESD robustness," in *IEDM Tech. Dig.*, Dec. 2014, pp. 3.5.1–3.5.4.

[8] C. Y. Chen, O. Tornblad, and R. W. Dutton, "Linearity analysis of lateral channel doping in RF power MOSFETs," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3389–3394, Dec. 2009.

[9] Y.-S. Lee, M.-W. Lee, S.-W. Jung, and Y.-H. Jeong, "Analog predistortion power amplifier using IMD sweet spots for WCDMA applications," in *Proc. Asia–Pacific Microw. Conf.*, Dec. 2007, pp. 1–4.

[10] A. Gupta, M. Shrivastava, M. S. Baghini, D. K. Sharma, H. Gossner, and V. R. Rao, "Part I: High-voltage MOS device design for improved static and RF performance," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3168–3175, Oct. 2015.