ESD Behavior of Tunnel FET Devices

Nagothu Karmel Kranthi and Mayank Shrivastava, *Senior Member, IEEE*

***Abstract*—For the first time, we present the electrostatic discharge (ESD) behavior of grounded gate tunnel FET (ggTFET) with detailed physical insight into the device operation, 3-D filamentation and failure under ESD stress conditions. Current as well as time evolution of the junction breakdown, device turn-ON, voltage snapback, and finally the unique failure mechanism is studied using both 2-D and 3-D technology computer aided design simulations. The interaction between the band-to-band tunneling, avalanche multiplication, and thermal carrier generation leading to voltage snapback and failure is presented in detail. In addition, electro-thermal instability initiated filamentation and snapback discovered in the ggTFET is explained. The impact of various technology and device design parameters on the ESD behavior and robustness of TFETs is discussed. This has helped developing guidelines to design ESD robust TFETs for efficient protection concepts. Finally, the charge device model behavior of ggTFET device is discussed.**

***Index Terms*—Band-to-band tunneling (BTBT), electrostatic discharge (ESD), tunnel FET.**

I. INTRODUCTION

THE aggressive scaling of the CMOS technology required a novel transistor concept beyond FinFETs in sub-10-nm technologies. Thermionic injection being the road block for reduction in subthreshold swing (SS), a novel concept, which works on tunnel-based injection rather than thermionic injection was the way forward. This lead to the invention of tunnel FET (TFET), which has potential to offer steep turn ON by gate-controlled carrier tunneling from valance band to the conduction band (CB) and minimize SS.

Over the last decade, TFETs have gone through tremendous explorations, example SiGe source, spacer engineering, highly doped abrupt source profiles, double gate architectures, and Band gap engineering using III–V materials [1]–[3] and vertical tunneling [4], [5]. Trap-assisted tunneling (TAT) at the source–channel interface and challenges in the formation of abrupt source–channel junction are still major concerns to achieve theoretical limits of SS and higher ON current in TFETs. In the recent time, efforts have been made by different groups to understand long term reliability of TFET devices [6], [7]; however, insights into the electrostatic discharge (ESD) behavior of TFET devices, which is a major reliability concern in sub-22-nm node technologies [8], [9], are

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The authors are with the Advance Nanoelectronic Device and Circuit Research Group, Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: mayank@dese.iisc.ernet.in).

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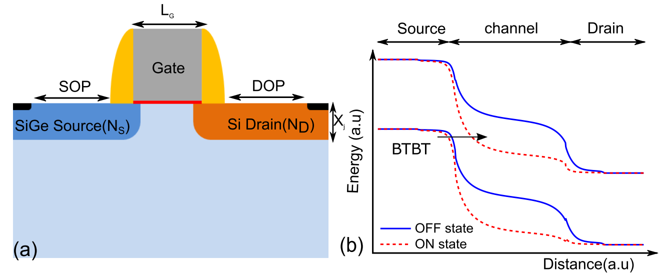

Fig. 1. (a) Cross sectional view of the Point TFET used in this paper. (b) Energy band profile of TFET device depicting both OFF-state (V_{GS} = 0V and V_{DS} = 0.5V) and ON-state (V_{GS} = 0.5V and V_{DS} = 0.5V) operation. The device parameters used for ESD explorations are: $N_D = 5 \times 10^{19}$ /cm^3, $N_S = 1{\times}10^{20}$ /cm^3, Germanium mole fraction (x) = 0.3, effective oxide thickness (EOT) = 0.6 nm, Junction depth X_j = 10 nm, and source side spacer dielectric constant (K_{sp}) = 3.9. L_G, *SOP*, and *DOP* are selected according to TCAD experiments.

still missing in the literature. A detailed physical insight into the ESD behavior of such novel devices at an early stage not only reduces the design time, but it also allows development of robust ESD protection concepts. While keeping in mind that the TFET is being considered as a strong contender to replace FinFETs in sub-10-nm node CMOS technologies, this paper attempts to understand the high-current ESD physics of the TFET devices using complex 3-D technology computer aided design (TCAD) simulations.

This paper is arranged as follows: Section II provides a basic understanding of TFET operation with insights into the various physical models and the calibration strategy used for the ESD TCAD simulations. Section III explains the detailed operation of the TFET device under ESD condition with physical insights. Section IV reveals the electrothermal instability-initiated filamentation and destructive snapback discovered in grounded gate TFET (ggTFET); whereas the impact of various technology parameters on the ESD behavior of ggTFET with technology guidelines are given in Section V. Finally, the charge device model (CDM), behavior of TFET devices is presented in Section VI before concluding this paper in Section VII.

II. TFET TECHNOLOGY AND COMPUTATIONAL FRAMEWORK

A. How Tunnel FET Works?

Tunneling is purely a quantum mechanical phenomenon. Fig. 1(a) shows the cross-sectional view of a point TFET device used in this paper for ESD investigations. Note that the silicide blocking of source and drain regions [drain side silicide blocking length (DOP) and source side silicide blocking length (SOP)] is only deployed for ESD explorations. Fig. 1(b)

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shows that the energy band diagram along the transport direction in the channel region, both under OFF and ON states.

In the OFF state, minority carriers (electrons) in the valence band (VB) of the P^+ source experiences no band overlap with the CB of the channel region, as shown in Fig. 1(b). This hinders the electron tunneling from the VB of the source region to the CB of the channel. The band overlap between source side VB and channel region's CB can be tuned with the application of applied gate field, which increases the band bending and reduces the tunneling distance when vertical gate field is increased. As soon as the overlap is achieved, the availability of unfilled energy states at lower energies in the channel makes the electrons from the VB of source to tunnel into the CB of channel and contributes to the transistor current. The probability of tunneling depends on electric field across the tunnel junction (E), carrier effective mass (m), the source band gap (E_g) as depicted in the equation [10]

$$T_{BTBT} = exp\left(-\frac{4\sqrt{2m^* E_g^3}}{3q\hbar E}\right). \quad (1)$$

It is worth highlighting that a rigorous design of experiment was used in this paper to realize a TFET device for ESD investigations. While maximizing I_{on}/I_{off}, the design of experiments involved source doping, source side band-gap engineering, and source/drain spacer design. The optimum device parameters used in this paper for ESD explorations are listed in Fig. 1.

B. TCAD Framework and Model Calibration

Computation of tunneling field effect phenomena, which involves complex nonlocal band-to-band tunneling (BTBT), is not trivial to capture along with 3-D high-field and high-current effects. Therefore, it worth highlighting that a rigorous modeling approach has been followed in this paper. To capture BTBT phenomenon, a non-local BTBT model is used, which considers Wentzel–Kramers–Brillouin) approximation with two-band dispersion relation while accounting for the electron–hole wave-vector throughout the tunneling path to solve for the total tunneling probability [11]. The modeling approach, adopted from [11], is explained in great detail in [12].

It is worth highlighting that the nonlocal BTBT approach captures tunneling at all the junctions and interfaces of the device. The device setup is first calibrated for the drift diffusion transport with nonlocal BTBT. Mobility and BTBT models were calibrated against experimental data reported in [13]. Since silicon–germanium is being used as source material in TFET device used for ESD explorations, tunneling models were calibrated against a SiGe TFET as well. For calibration, device design, doping profiles, and device dimensions were borrowed from [13]. TAT was reported to be a major concern, which limits the subthreshold characteristics of TFET devices. TAT is dominant in the presence of high electric field at the tunneling interfaces. In this paper, TAT was captured by using Shockley–Read–Hall (SRH) recombination model. The key BTBT model parameters after calibration with and without quantum confinement effect, as used in this paper, are summarized in Table I. As shown in Fig. 2, a good match between the experimental data and the simulated characteristic was obtained with less than 1% error.

TABLE I

Calibrated Barrier Tunneling Model Parameters. Here m_{te} Is the Electron Tunneling Mass, m_{th} Is the Hole Tunneling Mass, τ_{max} Is the Maximum SRH Recombination Time, and $\hbar\omega$ Is the Effective Phonon Energy

Parameter	Default	Calibrated w/o QC	Calibrated $w/$ QC
m_{te}	m_0	0.185*m_0	0.12*m_0
m_{th}	m_0	0.275*m_0	0.23*m_0
τ_{max}	1x10^{-5} s	2x10^{-5} s	4x10^{-6} s
$\hbar\omega$	0.068 eV	0.063 eV	0.046 eV

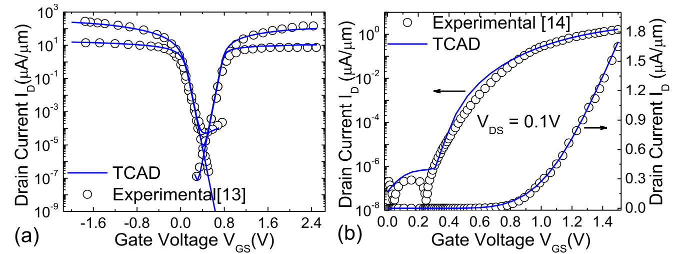

Fig. 2. TCAD calibration for TFET simulations. Calibration of (a) mobility models using device published in [13] and (b) tunneling models using device published in [14]. This depicts a good match between experiments and simulations.

Finally, high current and high-field effects, for example high-field mobility degradation for electrons and holes, auger recombination, avalanche generation, and electrothermal transport models were considered precisely to capture device behavior under ESD conditions. Details of 3-D ESD simulation setup and modeling approach used in this paper have been borrowed from [15].

III. ESD Behavior of TFETs

For all ESD/transmission line pulsing (TLP) simulations reported in this section and in Section IV, the drain terminal of the TFET was stressed using a current pulse of 10-ns rise time (RT) and 100-ns pulsewidth (PW) while keeping the human body model (HBM) like ESD event in mind. The quasi-statistic characteristics is obtained by averaging the transient data from 60 to 90 ns. Gate and source terminals were grounded in all the cases. The definition of thermal boundary condition is very crucial for ESD simulations [15]. Improper thermal boundary conditions can produce significant deviation in the results. Hence, a heat sink at different physical boundaries of the device was kept at spacing higher than the respective thermal diffusion length calculated for 100 ns.

Fig. 3(a) shows TLP I–V characteristics of ggTFET device with different regions of operation while including and excluding the barrier tunneling effect. In this paper, the terms barrier tunneling and BTBT are used in the same context,

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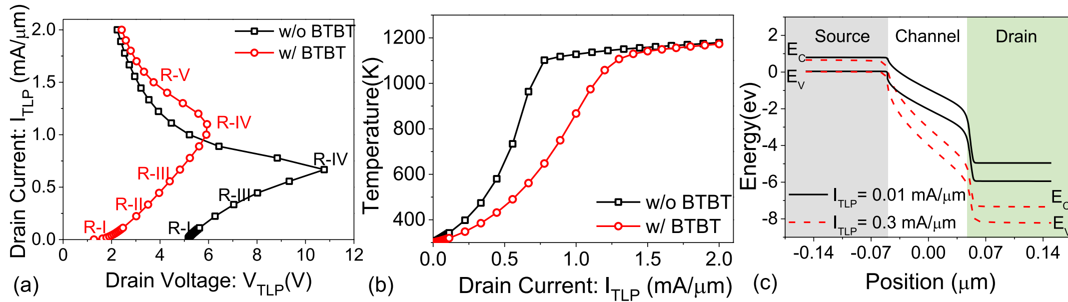

Fig. 3. (a) TLP *I–V* characteristics of ggTFET with and without barrier tunneling effect. (b) Maximum temperature across the device as a function of TLP current with and without barrier tunneling effect. (c) Energy band profile along the carrier transport direction and 3 nm below the gate–channel interface, both before and after device turn-ON.

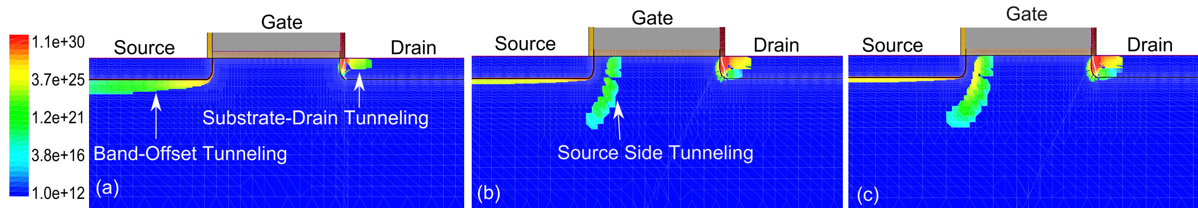

Fig. 4. Electron Barrier tunneling ($cm^{-3}s^{-1}$) at (a) very low injection currents (0.01 mA/μm), i.e., close to source–drain breakdown, (b) at the onset of device turn-ON (0.1 mA/μm), which depicts source side tunneling and (c) after the complete turn-ON (0.3 mA/μm) depicting a stronger source side tunneling.

i.e., interband tunneling. At lower injection currents the junction breakdown dominates (R–I), the excess carrier generated through this process triggers the device and lowers the ON-resistance ($R - II$ and $R - III$). This leads to self-heating across the device together with avalanche and BTBT generation, which causes the device to snap back to lower holding voltages (R–IV) and finally device sees failure, attributed to very high and localized self-heating (R–V). The device operation in these regions is explained in detailed below with physical insight into the ESD behavior of the device.

A. Junction Breakdown

As soon as ggTFET is stressed under ESD condition potential at the drain terminal increases to support the injected current. As the ESD stress is increased further, electric field in the reverse-biased drain–substrate junction increases to its critical value, which triggers the avalanche generation at the drain end. Drain–substrate junction breakdown is the major source of current at very low stress levels (1 μA/μm). When stressed further, the positive drain potential further lowers the energy bands in the drain–channel region besides generating excess carriers due to avalanche generation. This is depicted in Fig. 3(c). In the OFF state and at injection currents of the order 1 μA/μm, no significant band bending is observed and hence the current through the device is supported through reverse p-i-n leakage current. However, at a injection current of 0.1 mA/μm, BTBT-assisted avalanche generation can be observed. Fig. 3(c) shows significant band bending at the drain side at moderate currents. When the CB energy at the drain side becomes lower than the channel region's VB energy, the valance electrons from the channel region tunnel into the drain region while leaving behind the holes in the channel. Fig. 3(a) shows a significant contribution of BTBT in the breakdown regime. Holes are then drifted towards the source. This contributes to the total drain current at low injection levels as shown in Fig. 5(a), which shows the current density near BTBT-assisted avalanche breakdown, for an ESD stress of 0.01 mA/μm. To validate our argument and prove tunneling-assisted avalanche generation, we have simulated the same ggTFET device while excluding barrier tunneling effect. It shows that the breakdown voltage is increased by 2.5 times, if the barrier tunneling is not considered. This can be explained as the following. The tunnel carriers act as the minority carriers for avalanche multiplication process. If the BTBT is not taken into account, the number of carriers available for avalanche generation is lowered. This requires higher avalanche/field strength to turn-ON the device and, hence, higher breakdown voltage.

B. BTBT-Assisted Avalanche Generation: Device Turn-ON

The BTBT-assisted avalanche generation at the drain–substrate junction generates electron–hole pairs. The excess electrons are collected at the drain, whereas the excess holes drift towards the source region. Excess holes in the p-type substrate increases the local substrate potential, which causes a significant energy band bending and electric field at the source–channel interface. The band diagram in Fig. 3(c) shows a significant band overlap at the source–channel junction, which also reduces the tunneling distance from source to channel. This leads to BTBT from source to channel as shown in Fig. 4(b). Moreover, BTBT-assisted carrier injection from source to channel further aids to impact ionization at drain, which triggers an additional current path as shown in Fig. 5(b). As the injected current increases, the number

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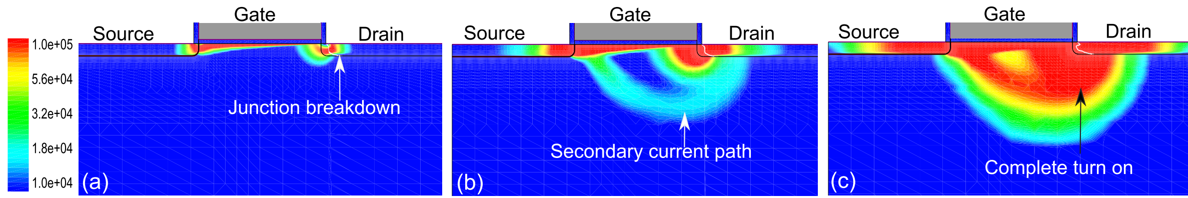

Fig. 5. Conduction current density (A cm^{-2}) at (a) very low injection currents (0.01 mA/μm), where the current is dominated by the drain-to-substrate junction breakdown, (b) medium injection level (0.1 mA/μm) at which formation of a second current path can be seen, and (c) at higher injection current (0.3 mA/μm) when the device is completely turned-ON.

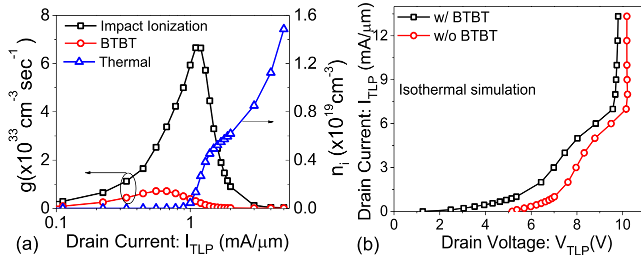

Fig. 6. (a) Comparison of carrier generation rate (cm^{-3}s^{-1}) due to impact ionization and barrier tunneling with induced excess carrier density (cm^{-3}) due to self-heating, as a function of TLP current. Though the generation rates for BTBT and avalanche actions are accessible in units of cm^{-3}s^{-1}, the excess carrier generation due to lattice heating is only captured in terms of change in effective intrinsic density in units of cm^{-3}, which makes the comparison relative in nature. (b) ggTFET TLP I–V characteristics under isothermal condition with and without barrier tunneling effect.

of holes collected at the source/accumulated in the substrate region increases. This increases the band bending and hence BTBT at the source–channel interface [Fig. 4(b)], which enhances avalanche generation at the drain. This positive feedback action completely turns-ON the device (R-III) as shown in Fig. 5(c). It can be noticed from Fig. 5(b) that the second current path is slightly deeper compared with the first current path. This is explained as follows: the excess holes before getting collected at the source contact diffuse through the substrate, which in-turn increases the substrate potential. This triggers BTBT along the source—substrate junction, however, away from the channel, which in-turn forms another path for current to flow from drain to source.

C. Snapback

Fig. 6(a) compares the excess carrier generation due to impact ionization, barrier tunneling, and self-heating as a function of stress current. It shows that impact ionization and barrier tunneling dominates the thermal generation at junction breakdown and device turn-ON regions, which is submerged by thermal generation at currents close to the onset of snapback. Moreover, as discussed before, BTBT dominates impact ionization at current near 0.2 mA/μm. Interestingly excess carrier generation due to impact ionization and barrier tunneling vanishes at currents close to snapback. This is attributed to reduced drain potential after snapback. Fig. 6(b) shows TLP I–V characteristics of ggTFET device without accounting for self-heating across the device (isothermal). Under isothermal simulation, device depicts no snapback state, independent of whether barrier tunneling was considered or not. Earlier, Fig. 3(a) had shown the presence of snapback state when self-heating was considered, independent of barrier tunneling effect. The ESD current conduction through ggTFET device can be summarized as follows. Interaction between the avalanche, BTBT leads to device turn-ON and current conduction from source to drain. This leads to self-heating and hot spot formation at the drain side. As the maximum temperature in the hot spot reaches to a critical temperature, where the thermal carrier generation dominates the avalanche and BTBT processes, the regions between source and drain gets flooded with excess carriers. This 3(a) mitigates the BTBT generation and 3(b) leads to snapback state. This explanation together with Figs. 3 and 6concludes that the snapback in the ggTFET device is purely attributed to thermal generation, which is independent of mechanism involved in turn-ON of the device.

Furthermore, Fig. 3(b) shows peak lattice temperature versus stress current. It is worth highlighting that the critical temperature (T_c), which leads to voltage snapback remains the same in both the cases, i.e., with and without BTBT. However, the stress level at which the device snaps back is different under both the scenarios. The device with BTBT reaches to its critical J.E at much higher injected current when compared with simulation results when BTBT was not considered. This is attributed to difference in the peak electric field at the drain substrate junction. As soon as device turns-ON, the ON-resistance of the device continues to increase when BTBT is not considered, unlike the case with BTBT. This can be attributed to the fact that BTBT increases the impact ionization rate by providing excess minority carriers for impact ionization, whereas lattice heating mitigates impact ionization process due to increased electron–phonon scattering. This trade off is compared in Fig. 6(a). The impact ionization rate first increases with the stress current due to increase in BTBT. The same, however, falls at higher currents because of increased lattice heating. On the other hand, BTBT rate falls at higher current due to the presence of deep snapback and low holding voltage state present at higher current.

D. Failure

2-D TCAD simulations help very little in understanding the ESD failure mechanism. 3-D simulations were performed to understand the dynamics of filament formation and resulting change in failure current when compared with the case when no change across the width plane was enforced (2-D simulations). TFET being a newer technology and this paper being the first work on the ggTFET,

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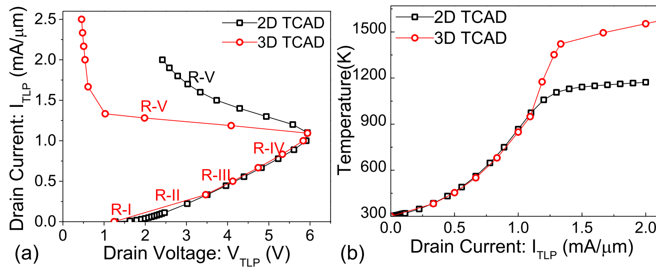

Fig. 7. (a) Comparison of TLP *I–V* characteristics of ggTFET device extracted using 2-D and 3-D TCAD simulations. The difference in the characteristics after the snapback is attributed to strong filament formation. (b) Maximum temperature across the device as a function of ESD current extracted using both 2-D and 3-D TCAD approaches.

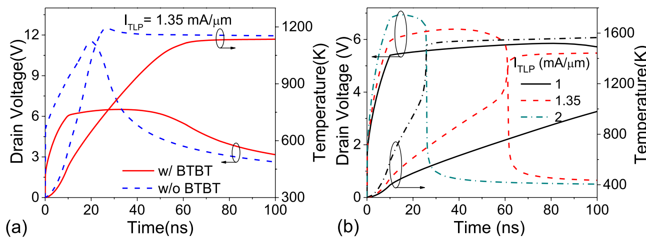

Fig. 8. (a) Sub-100-nm time response of ggTFET under ESD stress conditions, with and without considering barrier tunneling extracted using 2-D TCAD. (b) Drain voltage and maximum lattice temperature as a function of time for different stress currents extracted using 3-D TCAD simulations. Figure shows onset of filament formation and deep voltage snapback in a fully silicided ggTFET.

ESD behavior using both 2-D and 3-D approaches are explored to evaluate and understand the failure and filamentation mechanism. The 3-D TCAD approch used in this paper was presented in [16] and [17]. Fig. 7(a) shows that the 3-D simulation results deviate from the 2-D simulations after the onset of snapback. Moreover, 3-D simulations predict much deeper snapback of ggTFET devices and immediate fail after snapback. This is attributed to filament formation because of an electrothermal instability after snapback, which leads to a sharp increase in temperature as depicted in the inset of Fig. 7(b). Fig 7(b) also shows that for ggTFET device depth of snapback is directly related to self-heating across the device. Hence, the device can be believed to fail as soon as it achieves a snapback state. The 3-D behavior of ggTFET under ESD condition and physics of filament formation are discussed in detail in Section-IV.

IV. Origin of Electrothermal Instability and Filament Formation

Fig. 8 shows the transient response of the fully silicided device against HBM-like ESD stress. Contrary to the gradual snapback state present when 3-D [Fig. 8(a)], a sudden collapse in the drain voltage and sharp rise in the temperature can be seen after the onset of voltage snapback when 3-D effects are captured [Fig. 8(b)]. The transient analysis of the device under ESD stress gives deeper insights related to the time evolution of various aspects related to device turn-ON and failure. Figs. 8(b) and 9 shows that the junction breakdown occurs within 2 ns, device turn-ON takes place within 8 ns and failure after 60 ns under high-current injection conditions (I_{TLP} = 1.35 mA/μm). It is worth highlighting, as shown in Fig. 8(a), that the characteristics and time response differ when BTBT is not included. This again validates the role of barrier tunneling in the carrier transport through ggTFET under ESD condition. When the barrier tunneling is not accounted for, a sharp rise in voltage can be seen before snapback. However with BTBT such a sharp increase in voltage to support lower current injection is not witnessed. This validates higher sensitivity and role of barrier tunneling in avalanche generation. Finally, it is also observed that, the time to thermal snapback decreases with increasing stress level. This is attributed to snapback being a function of intrinsic carrier generation, which itself is a function of self-heating.

Fig. 7 shows differences in *I–V* characteristics when 3-D effects were captured compared with its 2-D counterpart. It shows that the device behavior differs in region *R*–V, which is attributed to strong filament formation after thermal snapback. A detailed analysis of 3-D TCAD results, as shown in Figs. 10 and 11 reveals the physics of filament in ggTFET devices, which is summarized as follows.

1) Onset of Thermal Snapback: At the stress current level greater than 1 mA, attributed to self-heating, when 1) thermal generation of excess carriers dominate BTBT and avalanche generation and 2) source to drain current under ESD condition is predominantly because of thermal generation of electron–hole pairs, a lower source-to-drain field is required to sustain conduction. This results in an onset of voltage snapback, which leads to nonuniform self-heating along the device width.

2) Nonuniform Self Heating and Electron–Hole Pair Generation: In addition to above-mentioned, the device edges experience higher self-heating when compared with the center of the device because of difference in the thermal resistance experienced by device center and edge regions. This causes a nonuniform temperature profile along the device width despite uniform current flow. Fig. 10(a) and (b) shows lattice temperature at the onset of thermal snapback and just after the filament formation, respectively. The nonuniform temperature along the width causes nonuniform electron–hole pair generation, which leads to nonuniform hole concentration and hence potential in the substrate along the width. Fig. 10(c) and (d) shows hole distribution before and after electrothermal instability.

3) Nonuniform BTBT: The electron tunneling at the source–channel junction is uniform along the width when the device is stressed below 1 mA (Fig. 7). As the BTBT at this junction is a function of energy band profile, nonuniform substrate potential, results in nonuniform band bending and BTBT. This increases the source side injection at one of the device edge leading to nonuniform conduction and filament formation. Fig. 11(a) and (b) shows the electron tunneling before and after the filament formation, respectively. Strong uniform BTBT at both drain–channel and source–channel junctions is observed before the filament formation, whereas nonuniform BTBT at source side and weak BTBT at drain side are observed after the formation of filament. A weak BTBT at drain side is attributed to voltage snapback. Note that at lower and medium currents, avalanche-assisted BTBT at drain is the major driving force for the carrier generation to support

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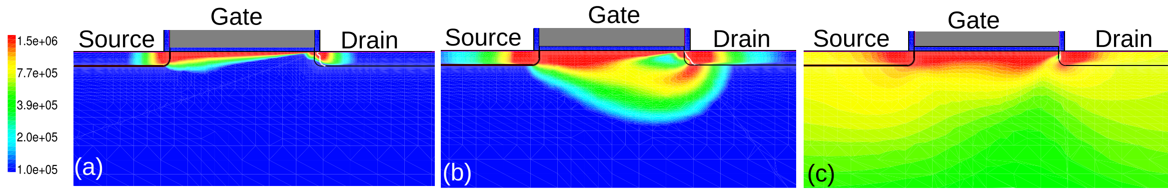

Fig. 9. Conduction current density (A cm^{-2}) at (a) 2 ns, (b) 8 ns, and (c) 90 ns depicting avalanche breakdown, device turn-ON and onset of snapback, respectively, under highcurrent (I_{TLP} = 1.35 mA) injection condition.

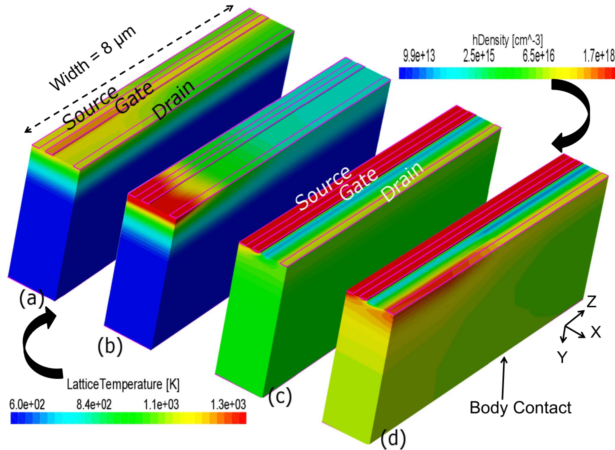

Fig. 10. (a) and (b) Lattice temperature (K) and (c) and (d) hole density (cm^{-3}) at the onset of filament formation [(a) and (c)] and after filamentation [(b) and (d)].

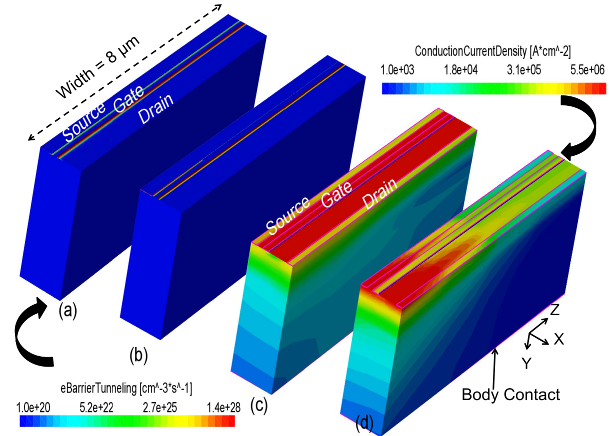

Fig. 11. (a) and (b) Electron barrier tunneling rate (cm^{-3}s^{-1}) and (c) and (d) conduction current density (A cm^{-2}) at the onset of voltage snapback [(a) and (a)] and after the filament formation [(b) and (d)].

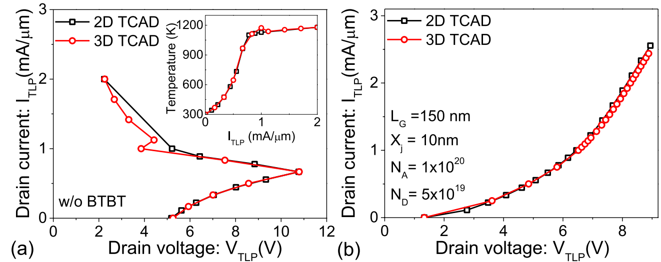

Fig. 12. 2-D versus. 3-D TLP characteristics of ggTFET device when (a) barrier tunneling is not captured and (b) lattice heating was not captured.

carrier transport before snapback. Due to the dominance of avalanche assisted BTBT over thermal carrier generation, the non-uniformity in temperature doesn't cause any instability before R-IV.

4) Strong Filament Formation: Step 1 to 3 act as positive feedback to each other, which leads to formation of a strong filament in less than a nanosecond. It is worth highlighting that no filament formation, i.e., uniform conduction was observed when BTBT was not considered in 3-D simulations (Fig. 12). This validates that nonuniform thermal generation sets the conditions for onset of filament formation, however nonuniform BTBT is the primary reason for strong filament formation.

Fig. 12(a) shows no difference in the snapback behavior extracted using 2-D and 3-D TCAD simulations when BTBT was not considered. This validates that filament formation is due to nonuniform BTBT. Similarly, Fig. 12(b) shows missing snapback in both 2-D and 3-D simulations, which validates that snapback is attributed to thermal carrier generation and electrothermal nature of the filament. In summary, these experiments validate our argument that the positive feedback between BTBT and nonuniform temperature along the width is the cause of filament formation and failure in ggTFET device stress under ESD condition.

V. Technology and Design Guidelines

Understanding the impact of various device design and technology parameters on the ESD behavior of a new device technology is crucial at the early stage of technology development. This helps in developing robust ESD protection concepts for the newer device technology. The impact of silicide blocking length, drain doping, germanium mole fraction, and junction depth on avalanche breakdown, device turn ON, onset of snapback and failure is discussed in this section using 3-D TCAD simulations.

A. Silicide Blocking

Current ballasting using silicide blocking has been widely reported to improve the ESD performance of ggNMOS devices [18]. Silicide blocking offers negligible resistance in the prefailure regime and limits the current crowding in the width direction at the onset of failure. Fig. 13(a) shows 100-ns TLP I–V characteristics of the ggTFET for DOP. The SOP kept at 100 nm throughout the analysis if not mentioned otherwise. Fig. 13(a) shows that the breakdown voltage is not affected by the silicide blocking in ggTFET, however, as soon as the device turns-ON silicide blocking increases the ON resistance of the device. Such an increase in ON resistance unique and often not observed in the ggNMOS devices. This is attributed to reduced barrier tunneling rate

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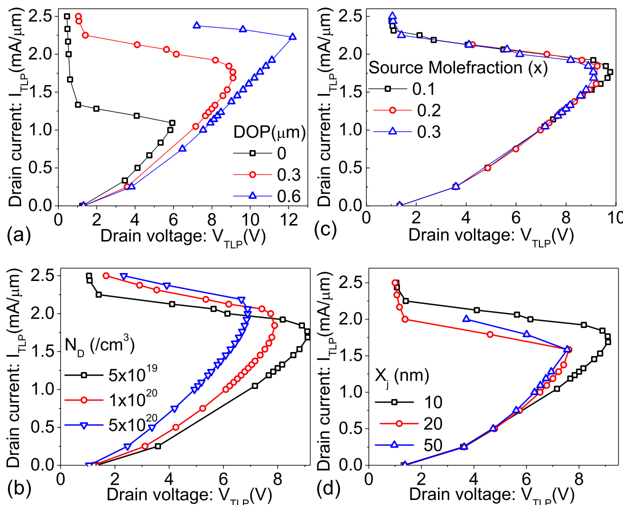

Fig. 13. (a) Impact of drain side silicide blocking on TLP characteristic of ggTFET. SOP was 100 nm. (b) TLP characteristics with varied drain doping (N_D). Increasing drain doping enhances the drain side tunneling (Xj = 10 nm, EOT = 0.6 nm, L_G = 100 nm, N_S = 1×10^{20}, DOP = 300 nm, and SOP = 100 nm). (c) Impact of germanium percentage (x) in $Si_{1-x}Ge_x$ source on the TLP characteristics of ggTFET device. (d) TLP I–V characteristics of ggTFET device for different S/D junction depths.

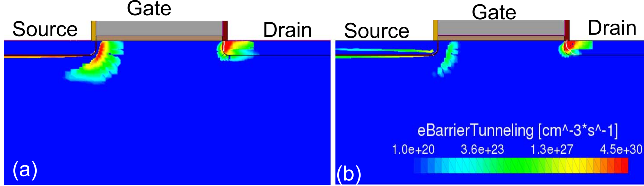

Fig. 14. Electron tunneling (cm^{-3}s^{-1}) for (a) fully silicided device and (b) silicide blocked device with DOP = 300 nm, extracted at fixed drain potential (V_{TLP} = 5V). The reduction in electron tunneling at source–channel junction with increased silicide blocking length (DOP) can be clearly noticed.

at the source–substrate junction for higher DOP, as shown in Fig. 14. As DOP increases the current flows deeper into the substrate, which reduces the effective hole density collected under the gate. This shifts the CB level in the channel region to higher energy, which reduces the valance band to CB overlap and lowers BTBT. The reduced tunneling rate leads to the requirement of higher avalanche strength, therefore higher fields, to support a given injection current. Furthermore, as DOP is increased, self-heating across the device is mitigated, which is attributed to lowering of overall current density for a given injected current. This increases the failure current and voltage required for thermal snapback, as clearly shown in Fig. 13(a).

B. Drain Engineering

Asymmetric source/drain doping profile is often used for improving the I_{on}/I_{off} and SS in TFET [10], [19]. Higher source doping offers improved I_{on}, whereas a moderate drain region doping lowers I_{off} and improves the subthreshold operation by lowering OFF-state BTBT at drain side, which mitigates the pMOS operation in the n-channel device. This mandates investigation of ggTFET's ESD behavior as a function of drain region doping (N_D). Fig. 13(b) depicts the TLP I–V characteristics of ggTFET for different drain doping while keeping DOP fixed (300 nm). It shows that lowering drain doping increases the breakdown voltage, which is attributed to significantly mitigated BTBT at the drain side when drain doping is reduced. This, in conjunction with reduced surface fields, lowers the BTBT-assisted avalanche generation. On the other hand, mitigated BTBT-assisted avalanche generation adversely affects the turn-ON of the device, which increases the ON-resistance of the device. As shown in Fig. 13(b), a device with lower drain doping requires higher drain potential to support a given injected current, which has caused higher ON resistance. This on one hand increases device's ruggedness or failure voltage while maintaining improved subthreshold characteristics, on the other hand it lowers the failure current, which is due to higher self-heating at lower currents. It is worth highlighting that while both higher silicide blocking length and lower drain doping increases the ON-resistance, silicide blocking improves the thermal performance and hence failure current, whereas lower drain doping leads to higher self-heating and reduces the failure current.

C. Source Engineering

Lower band gap materials for TFET source have been found to be very attractive as it lowers the tunneling barrier height and width, which increases source-to-channel tunneling probability and results in higher drive current. For Si TFETs, $Si_{1-x}Ge_x$ is the common choice of source material [13], [20]. Fig. 13(c) shows the TLP characteristics of ggTFET device with SiGe source with different Ge percentage (x) values. As the breakdown voltage of ggTFET and turn-ON at moderate currents does not depends on the source band gap, which has no influence on impact ionization and BTBT at the drain substrate junction, x has no influence on breakdown voltage and the ON resistance of the device. As soon as device achieves snapback state, at higher current levels, reduced source band gap by increasing x increases the electron tunneling from the source to channel/substrate. This lowers the snapback voltage while keeping the failure current the same.

D. Junction Depth

In ggNMOS devices, increase in the junction depth improves current spreading under high-current injection condition, attributed to better emitter efficiency of the lateral bipolar, which improves the ESD robustness of the device. Fig. 13(d) shows the impact of junction depth (X_j) on the ESD behavior of ggTFET devices. Unlike ggNMOS, junction depth beyond $X_j = 20nm$ plays no role under high-current injection condition. It shows that the ON-resistance, which is directly related to tunneling efficiency from source to substrate/channel, increases for $X_j < 20nm$. Increasing junction depth increases the tunneling cross section at the source–substrate interface, which in-turn increases the tunneling current and hence lowers the ON-resistance. On the other hand, increasing junction depth was found to lower the BTBT generation rate. This is attributed to relaxed hole distributed across a wider region, which lowers the substrate potential and band bending. This in-turn reduces the

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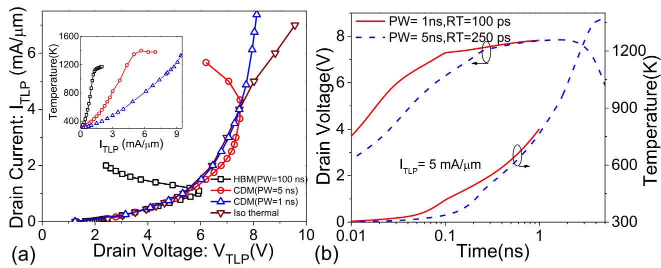

Fig. 15. (a) TLP *I*–*V* characteristics of ggTFET extracted under HBM, CDM, and isothermal conditions. (b) Transient CDM behavior of ggTFET for pulse duration of 1 ns (RT = 100 ps) and 5 ns (RT = 250 ps).

tunneling current. For junction depth < 20-nm increase in tunneling cross-sectional area dominates and current continue to increase with increasing junction depth, however, at junction depth > 20 nm, these two competing effects counter balance each other, which limits the current to increase further.

VI. CDM Behavior

Fig. 15 shows the ggTFET behavior under very fast TLP (CDM-like ESD stress) conditions. For these simulations RT of 100/250 ps and the PW of 1/5 ns was considered. The quasi-static characteristics was obtained by averaging the voltage and current data from 60% to 90% interval. For physical comparison, TLP I–V characteristic extracted from isothermal simulation is also given. Fig. 15 clearly shows lower self-heating under CDM conditions, which delays the thermal snapback and allows the vf-TLP characteristics to follow isothermal characteristics. The device stressed under CDM condition has six times higher It2 when compared woth the same under HBM condition. However, Vt2 is 20% higher when compared with HBM like stress condition.

VII. Conclusion

The ESD behavior of grounded gate point TFET device is presented in detail for the first time. The device turn-ON was attributed to BTBT-assisted avalanche generation, whereas BTBT in conjunction with avalanche and thermal carrier generation was found to cause deep voltage snapback. At currents beyond snapback region, thermal generation was found to dominate the avalanche and band-to-band contribution, which leads to thermal failure. Nonuniform thermal generation leads to nonuniform BTBT in TFET devices, which causes filament formation and failure. Nonuniform thermal generation sets the conditions for the onset of filament formation, however, nonuniform BTBT is the primary reason for strong filament formation. Finally, the device design guideline presented in this paper depicts the importance of silicide blocking, source engineering, and junction depth. It was found that silicide blocking mitigates the BTBT-assisted electrothermal instability, which increases threshold for voltage snapback and failure current by increasing silicide blocking length. This improves the ESD robustness of ggTFET devices. The CDM behavior of ggTFET device was found to be similar to isothermal response. The failure current under CDM condition was six times higher compared with the same under HBM condition at a cost of 20% increase in failure/holding voltage.

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Nagothu Karmel Kranthi received the M.Tech. degree from the National Institute of Technology, Calicut, India, in 2014. He is currently pursuing the Ph.D. degree in advanced nanoelectronic devices, Circuit Research Group, Indian Institute of Science, Bangalore, India.

He was with ST microelectronics, Noida, India, as a Graduate Trainee from 2013 to 2014, where he was involved in ESD related issues in 28 nm FDSOI technology.

Mayank Shrivastava (S'09–M'10–SM'16) received the Ph.D. degree from the IIT Bombay, Mumbai, India, in 2010.

He is currently an Assistant Professor with the Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, India. He joined Indian Institute of Science as an Assistant professor in 2013, where he has established the Advance Nanoelectronic Device and Circuit Research Group.

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