

A Comprehensive Computational Modeling Approach for AlGaIn/GaN HEMTs

Vipin Joshi, Ankit Soni, Shree Prakash Tiwari, *Senior Member, IEEE*, and
Mayank Shrivastava, *Senior Member, IEEE*

Abstract—This paper for the first time presents a comprehensive computational modeling approach for AlGaIn/GaN high electron mobility transistors. Impact of the polarization charge at different material interfaces on the energy band profile as well as parasitic charge across the epitaxial stack is modeled and studied. Furthermore, impact of surface and bulk traps on two-dimensional electron gas, device characteristics, and gate leakage is accounted in this paper. For the first time, surface states modeled as donor type traps were correlated with gate leakage. Moreover, a new approach to accurately model the forward gate leakage in Schottky gate devices is proposed. Finally, impact of lattice and carrier heating is studied, while highlighting the relevance of carrier heating, lattice heating, and bulk traps over the device characteristics. In addition to this, modeling strategy for other critical aspects like parasitic charges, quantum effects, S/D Schottky contacts, and high field effects is presented.

Index Terms—AlGaIn/GaN, computational modeling, HEMT, hot electrons, surface traps, 2-DEG.

I. INTRODUCTION

WIDE band gap semiconductor based power devices like AlGaIn/GaN HEMTs have emerged as the most viable alternative of Silicon based power devices. Extensive research is being carried out to improve performance and reliability of these devices since past few decades. As the demand for more efficient and robust designs are on a rise, it has become essential to adopt a well-developed design and analysis methodology. Silicon based power devices have greatly benefited from computational modeling based design approach. Si power devices have established their ground in terms of physics based prediction

Manuscript received August 24, 2016; accepted October 2, 2016. Date of publication October 6, 2016; date of current version November 8, 2016. This work at Indian Institute of Science, Bangalore, India, was supported by the Department of Electronics and Information Technology, Government of India, under National Mission on Power Electronic Technology Project NaMPETPh-II/SP13/Ex05 and Department of Science and Technology, Government of India, under Technology Systems Development Programme's (TSDP) project DST/TSG/AMT/2015/294. The review of this paper was arranged by Associate Editor M. Fischetti. Vipin Joshi and Ankit Soni contributed equally to this work.

V. Joshi is with Department of Electrical Engineering at Indian Institute of Technology Jodhpur, Jodhpur 342001, India. He is also associated with Advanced Nanoelectronic Device and Circuit Research Laboratory, Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore, as an intern (e-mail: pg201382005@iitj.ac.in).

A. Soni and M. Shrivastava are with the Advanced Nanoelectronic Device and Circuit Research Laboratory, Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore 560012, India (e-mail: sankit@ese.iisc.ernet.in; mayank@ese.iisc.ernet.in).

S. P. Tiwari is with the Department of Electrical Engineering, Indian Institute of Technology Jodhpur, Jodhpur 342001, India (e-mail: sptiwari@iitj.ac.in).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TNANO.2016.2615645

of device behavior and are widely accepted by semiconductor industry, as the approach can accurately predict behavior and physics of complex device designs. It further extensively aids in device-circuit co-design and design for reliability during the development phase. The application of computational modeling in complex semiconductor technology development is not new, for example, this has greatly assisted in enablement and performance improvement of FinFET technology [1]–[3]. Similarly, high power devices like LDMOS were also designed and investigated using a similar approach, which helped in higher robustness and performance [4], [5]. On the other hand, HEMT being relatively emergent technology lags behind in terms of availability of a reliable and consistent computational modeling strategy. This hinders progress and limits technology development to rely only on hardware results. Moreover, the presence of unique polarization effects combined with presence of traps, hot electrons and self heating make prediction of accurate device behavior for HEMTs a challenging task. Few efforts have been made in the past to compute HEMTs [6]–[18], but none of the reports encapsulate all the required aspects and physics, which is critically important to precisely predict device characteristics under all complex boundary conditions. Earlier works [6]–[9] have extensively discussed effect of traps on drain/gate lag effect [6], drain current dispersion [7], high field performance of device [8], gate leakage and breakdown characteristics of the device [9]. The simulation studies in [10] and [11] have presented effect of gate connected [10] and source connected [11] field plates on the breakdown voltage of the device, which was further extended by Saito *et al.* to breakdown voltage vs. on-resistance (V_{br} - R_{on}) trade-off [11]. Bahat-Treidel *et al.* have confined their simulation studies [12] only to the effect of AlGaIn back barrier layer on the Energy band diagrams and punch through voltage enhancement in AlGaIn/GaN HEMTs. In [13], Palacios *et al.* have done a comprehensive study on the source of increase in dynamic source resistance of AlGaIn/GaN HEMT devices. Effect of field plate structures on Dynamic-ON resistance of the device has been analyzed by Saito *et al.* in [14]; however, the simulation studies were limited only to electric field calculations. Longobardi *et al.* have presented a study on effect of donor traps on sheet charge density and AlGaIn/GaN HEMT device characteristics [15]; however, the study is limited to surface traps only. Wang *et al.* have discussed hot electron and self heating effects in Double Channel HEMTs [16], however, the discussion does not consider surface states and traps at other locations which affect GaN HEMT performance. Simulation studies on the modeling of Fe and C doping in GaN as traps, which explain the impact of these dopants on the current collapse behavior of HEMT devices

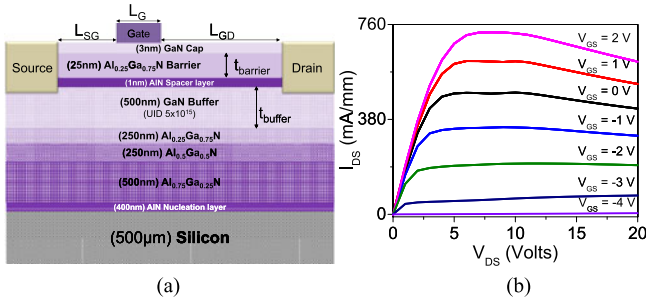


Fig. 1. (a) Cross-sectional view of the realized HEMT device and (b) Measured $I_{DS} - V_{DS}$ characteristics of the HEMT device.

is presented in [17], [18]. However these studies are confined to impact of traps on current collapse and don't consider effect of hot electrons and surface states which, as will be explained later, are also necessary to model the DC behavior of the device. While these simulation studies give reasonable insight on individual aspects of AlGaN/GaN HEMTs; they fail to encapsulate all physical aspects to accurately capture the device characteristics. This work examines all the aspects of AlGaN/GaN HEMT device operation and captures critical aspects like polarization charge, quantum effects, surface traps, bulk traps, contacts, gate stack, gate leakage, carrier dynamics, carrier tunneling, hot electrons, high field effects, and self heating behavior. Based on this a computational modeling strategy has been established, which enables physics based prediction of experimental trends and characteristics of newer designs. The numerical computations are done using Sentaurus TCAD [19]. The paper is arranged as follows. Section II presents details of HEMT device and measured characteristics used in this work. Section III & IV collectively address challenges associated with modeling of various physical aspects, proposed modeling approach and impact of various physical parameters. In particular, Section III discusses origin of charge carriers and effect of traps on device characteristics; whereas Section IV emphasizes on challenges related to carrier dynamics, which were not considered in earlier works. Finally, this work is concluded in Section V.

II. HEMT DEVICE AND EXPERIMENTAL RESULTS

Fig. 1(a) depicts the stack details and schematic view of the Normally-ON AlGaN/GaN HEMT device considered in this work to develop a computational modeling strategy. The AlGaN/GaN stack is grown over a Silicon substrate, using MOCVD, with AlN nucleation layer. Al_xGa_{1-x}N transition layers were grown on the top of AlN nucleation layer before growing GaN buffer, which mitigates the dislocation density and the lattice mismatch between GaN buffer and substrate. AlGaN barrier is separated from GaN buffer by a 1 nm thick AlN layer which has been reported to provide better $n_s \cdot \mu$ product [20]. Finally, AlGaN barrier is covered by a 3-nm GaN cap. Ohmic contacts were developed using rapid thermal annealing of Ti/Al/Ni/Au (20/120/30/50 nm) stack at 870 °C for 30 seconds. A Schottky gate was used, which consists of Ni/Au (20/130 nm) metal stack. The source to drain distance (L_{sd}) and gate length (L_g) are 4 μm and 1 μm, respectively. The

measured $I_{DS} - V_{DS}$ characteristics of the device are as shown in Fig. 1(b). The Hall mobility of the device is 1931 cm²/V·s and the extracted sheet density (n_s) is 10¹³ cm⁻².

III. COMPUTATIONAL MODELING CHALLENGES: ELECTROSTATICS

A. Polarization and 2-Dimensional Electron Gas

An absence of inversion symmetry in III-N compounds gives rise to polarization field and associated charges. Growth of Al-GaN/GaN epitaxial layers in [0001] direction, allows stacking of these polarization charges in a way that creates favorable environment for electrons to accumulate in the GaN layer at Al-GaN/GaN interface, forming a sheet type charge region known as 2-Dimensional Electron Gas (2-DEG). While earlier works have attempted to model polarization charge [6]–[8], [10], [13]–[15], [17], these works limit the polarization effect inside the AlGaN layer by adding a +σ charge at the AlGaN/GaN interface and an equivalent -σ charge at the AlGaN top surface. While this approach is sufficient to model current, it neglects polarization charge at any other material interfaces, which is essential to capture all aspects of device physics, parasitic effects and to predict characteristics of double channel HEMTs. The method used in this work takes care of the polarization charge at all the III-N interfaces and accounts for parasitic charges as well. Polarization charges can be computed numerically as suggested by Ambacher *et al.* in [21], which approximates the charge induced due to discontinuity in the polarization vector at material interfaces. In principle there is no discontinuity in the x and y plane, therefore one can ignore the spontaneous polarization in x and y plane (this however may not be valid for 3D HEMT devices). The polarization along the z plane is given as $P_z = P_z^{SP} + P_{strain}$, where, $P_{strain} = 2d_{31} \cdot S \cdot (c_{11} + c_{12} - 2c_{13}^2/c_{33})$, c_{ij} are stiffness constant, d_{31} is piezoelectric coefficient and P^{SP} denotes the spontaneous polarization vector. Quantities c_{ij} & d_{ij} are calculated over the plane perpendicular to axis i and are oriented in the j direction. S is strain in a given layer, which is given as $S = (1 - R) \cdot (a_0 - a) / a$, where R is the strain relaxation parameter, a_0 and a are the lattice constants of strained and unstrained layers, respectively. Once the polarization vector is calculated, the polarization charge can be calculated as $q_{pol} = -A \cdot \nabla P$, where parameter A is a fitting constant. Once the polarization charge is calculated, it is straight forward to include this in the Poisson equation ($\Delta \epsilon \cdot \Delta \phi = -q(p - n + N_D - N_A + q_{pol})$) to capture electrostatic behavior of the device.

While polarization charge at the AlGaN/GaN interface is desirable for 2DEG channel, its presence at other interfaces significantly affects vertical field distribution and therefore energy band profile and parasitic charge distribution, as depicted in Fig. 2(a). The modified energy band profile results in parasitic hole density at other material interfaces (Fig. 2(c)) and varies the sheet charge density profile (Fig. 2(d)). Fig. 2(d) further shows an electron concentration in the barrier layer, which is attributed to the energy band profile with conduction band energy below the fermi-level in the barrier layer (Fig. 2(b)). This leads to formation of secondary channel in the device. These observations and findings clearly justify the importance of inclusion of

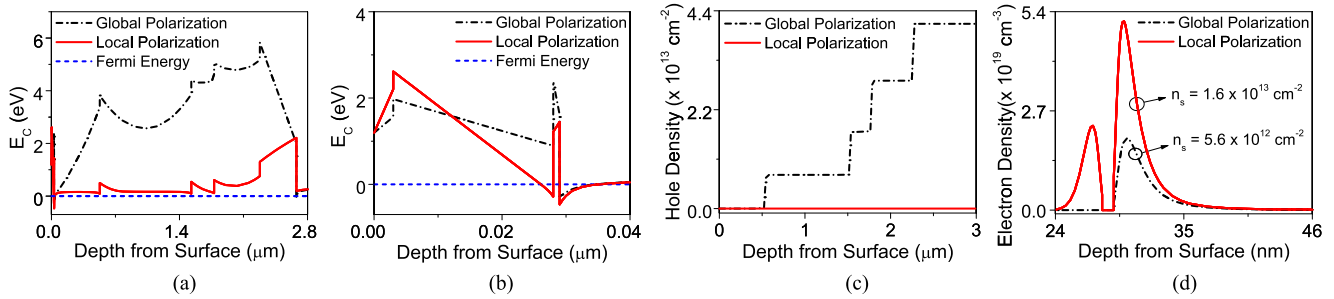


Fig. 2. Effect of polarization profile on (a) Energy band profile as a function of stack depth, (b) Energy band profile near the channel region, (c) Parasitic hole density and (d) sheet charge density profile. All the measurements are done at initial rest condition. While, Global polarization considers polarization charge for the whole device, localized polarization limits the polarization charge computation to the AlGa_N barrier layer only. The Hole density plot contains integrated values on Y-axis, thus each step shows presence of a corresponding hole density peak.

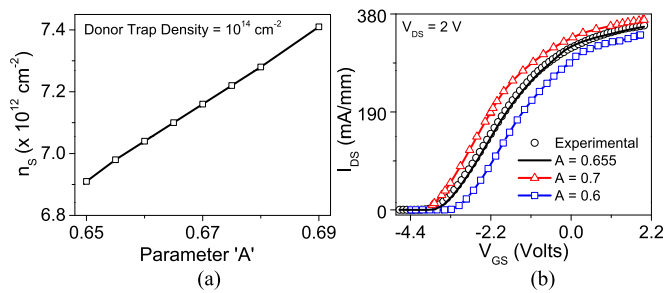


Fig. 3. Effect of linear fitting parameter A on (a) Sheet charge density, and (b) $I_{DS} - V_{GS}$ characteristics of the device.

polarization charge at all the material interfaces, which results in accurate and adaptive results - independent of III-N stack. This also becomes significantly important in analyzing effect of buffer traps on device characteristics under application of different transition/back-barrier layers, as the modified energy band profile will significantly affect the occupation state of these traps. As discussed above, Fig. 3 depicts impact of linear fitting parameter A ($q_{pol} = -A \cdot \nabla P$) on the device characteristics, in particular sheet carrier concentration and threshold voltage of the device.

It is well known that sheet carrier distribution and peak concentration are strong function of Al mole fraction (x) in Al _{x} Ga _{$1-x$} N barrier layer, degree of stress or stress relaxation at the AlGa_N/Ga_N interface (R) and barrier layer thickness (t_{AlGa_N}). Increasing Al mole fraction increases bandgap of the barrier layer as well as polarization at the interface. Moreover, at higher Al mole fractions ($x > 0.4$) strain relaxation typically occurs at the interface, which leads to reduced piezoelectric polarization and hence a reduced sheet density. In principle all these design and technology parameters map to the amount of stress at the AlGa_N/Ga_N interface, which directly affects the sheet carrier concentration and distribution. Hence, these trends can be incorporated in the model used above for P_{strain} and strain relaxation parameter ($S = (1 - R) \cdot (a_0 - a) / a$). The modeled and simulated trends are depicted in Fig. 4(a). Similarly, t_{AlGa_N} affects the polarization field in the AlGa_N layer and hence reducing t_{AlGa_N} reduces sheet charge density as per the relation $q_{pol} = -A \cdot \nabla P$. Fig. 4(b) outlines the modeled 2-DEG density (n_s) dependence on barrier thickness and gate recess. As depicted, a thinner barrier reduces n_s , attributed to

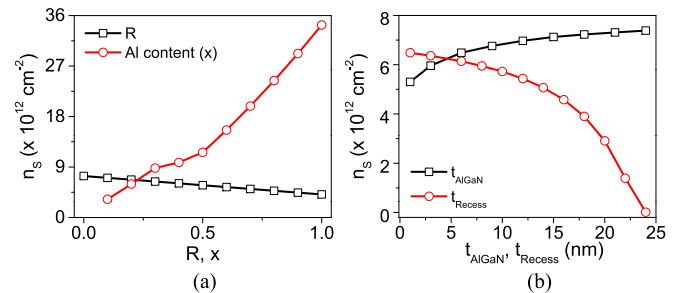


Fig. 4. Sheet charge density variation as a function of (a) Al mole fraction in barrier layer and degree of relaxation at AlGa_N/Ga_N interface, and (b) barrier layer thickness and gate-recess depth. The relaxation parameter calculations assume an Al mole fraction of 0.25 (Al_{0.25}Ga_{0.75}N). Gate recess depth calculations assume an AlGa_N layer thickness of 25 nm and the gate recess depth is calculated from the top of the structure, i.e., from the top of Ga_N cap layer. All the sheet charge density calculations are done along a cut line, through the epitaxial layers, located in the middle of the gate electrode.

higher polarization fields developed in the barrier layer, which depletes the channel. This is an important aspect to model in order to design stack for Normally-ON devices and design recess for Normally-OFF devices.

B. Quantum Effects

Since at the AlGa_N/Ga_N interface the conduction band energy changes abruptly and hence charge carriers are confined to a narrow quantum well (few nm), quantum confinement effects like energy band splitting and reduced density of states are expected to play a key role. It is worth highlighting that most of the simulation studies presented earlier [6]–[10], [12], [13] have neglected quantum confinement effects. Quantum confinement effects, as depicted in Fig. 5, lowers the peak 2DEG concentration; however shifts the peak away from the AlGa_N/Ga_N interface, which improves carrier mobility. Hence accounting quantum confinement is of high importance for accurate prediction on threshold voltage, transconductance and ON current of the device. While Schrödinger wave equation offers the most physically sophisticated and accurate model to account quantum effects, it is however numerically expensive to be solved for larger HEMT devices. In order to achieve accuracy comparable to that of Schrödinger equation and to have acceptable numerical cost, density gradient quantum correction model [22], [23] is deployed in this work, while using Schrödinger equation to

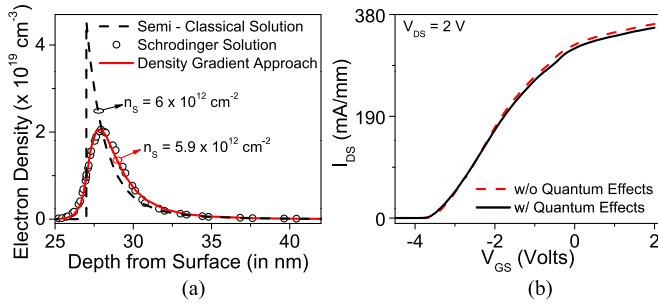


Fig. 5. Effect of Quantum confinement on (a) sheet charge density profile, and (b) $I_{DS} - V_{GS}$ characteristics of the device. The density gradient quantum profile is in good agreement with the Schrödinger solution, while the $I_{DS} - V_{GS}$ characteristics suggest no significant degradation in device characteristics in presence of quantum effects.

extract model parameters. It accounts for quantum effects by introducing a potential like term Λ_n into the classical density formula:

$$n = N_C F_{1/2} \left(\frac{E_{F,n} - E_C - \Lambda_n}{kT_n} \right) \quad (1)$$

where, N_C is the effective density of states, $F_{1/2}$ is Fermi integral of order 1/2, $E_{F,n}$ is the quasi-Fermi energy for electrons, E_C is the conduction band edge and kT_n represents thermal energy of electrons. Λ_n is computed as:

$$\Lambda_n = -\frac{\gamma \hbar^2}{6m_n} \cdot \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \quad (2)$$

where, $\hbar = h/2\pi$ is Planck's constant, m_n is the electron effective mass, n is electron density and γ is a fitting parameter. For the electron density profile calculated using this model to be in full agreement with solution of Schrödinger equation, as depicted in Fig. 5, γ was found to be 1.3 and 2.2 for GaN and AlN, respectively.

C. Surface States

Ibbetson *et al.* [24] suggested that polarization charges alone are not sufficient to explain 2DEG profile and proposed that surface states in presence of polarization field defines the 2DEG. On the other hand, Meneghesso *et al.* proposed (i) formation of a high density hole layer at the surface of the device to account for negative charge carriers in the channel and (ii) presence of surface states, which behave as traps to capture these hole [7]. Mitigation of RF dispersion [25], [26], drain and gate lag effects [6], [7] by surface passivation also support presence of surface traps [27], pertaining to Nitrogen vacancies. Simulation result, as depicted in Fig. 6(a), reveals a surge in drain current in the absence of surface states, which is attributed to hole current contributed by holes present at the surface. However, such a current surge does not exist in the experimental characteristics of the device, which suggests compensation of hole current or suppression of mobile hole charge by some means, which is depicted in Fig. 6(b). It shows that hole current is fully compensated by donor type surface states resulting in a negligible hole current, which supports the earlier theory [7]. In this work the donor

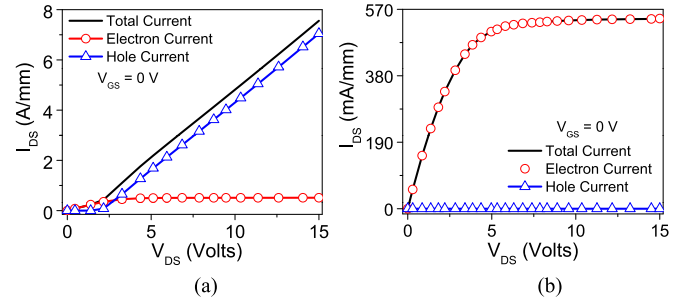


Fig. 6. $I_{DS} - V_{DS}$ characteristics of the device (a) without Traps and (b) with Donor type Traps (Density = $1 \times 10^{14} \text{ cm}^{-2}$, Energy = $E_C - 0.6 \text{ eV}$). The characteristics of the device without traps clearly show a dominant hole current while presence of surface traps suppress this hole current.

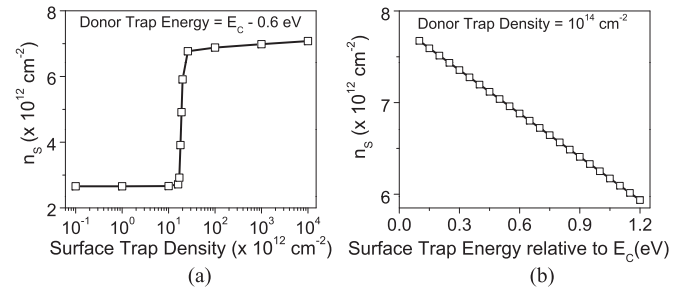


Fig. 7. Variations in sheet charge density as a function of surface donor type trap (a) Density, and (b) Energy.

type surface states are modeled as donor traps with trap density of $1 \times 10^{14} \text{ cm}^{-2}$ and an activation energy of $E_C - 0.6 \text{ eV}$.

The trends and observations presented above are further quantified in Fig. 7, which depicts impact of surface trap density and energy on 2DEG density. Ionized surface traps will behave as positive charge sheet and hence an equal increase in the 2DEG charge is expected to compensate the positive charge sheet at the surface. Fig. 7(a) shows that the 2DEG density increases with surface trap density and shows a abrupt increase in 2DEG density above a particular threshold of surface trap density. This is attributed to ionization of surface states, which results in an increased sheet charge density. However, above a certain value of surface trap density, the 2DEG density saturates, which can be attributed to Fermi level pinning and resulting saturation of ionized donor density at the surface [28]. Fig. 7(b) depicts that the 2-DEG density increases as traps become shallower, i.e. move close to Conduction band level, attributed to increased ionization of shallower traps. Surface traps and polarization charge both affect the sheet charge density; however, the polarization charge shows a greater control on the threshold voltage of the device. On the other hand, surface traps greatly influence the gate leakage characteristics, which will be modeled in the following sections.

D. Traps

Since HEMTs consist of several epitaxial layers, defects are expected to be present within individual layers as well as the interfaces. Depending on the physical location, some of these defects can behave as donor or acceptor type bulk as well as interface traps. While the spatial and energy distribution of such

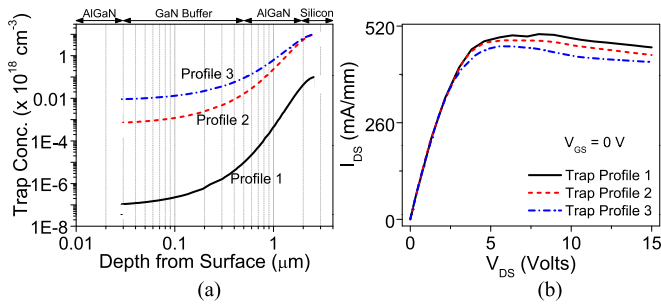


Fig. 8. (a) Gaussian trap profile used in buffer layer of the HEMT device. (b) $I_{DS} - V_{DS}$ characteristics of the device under influence of buffer traps. Acceptor type Buffer traps were used with Trap Energy as $E_C - 0.96$ eV. Buffer traps reduce the overall current but are not responsible for negative differential resistance phenomena.

traps and its relation with growth parameters is still not well understood, earlier works suggest presence of acceptor type traps in the bulk of GaN cap, GaN buffer and AlGaN barrier while donor type traps are expected to be present over the surface of GaN capping layer [8]. Traps present in the GaN buffer region and on the HEMT surface are considered to be dominant for the prediction of electrical characteristics of the device. While the role of surface traps has already been discussed in previous section, traps in the GaN buffer are modeled here.

A peculiar feature in the measured $I_{DS} - V_{DS}$ characteristics of GaN HEMTs at higher voltages was consistently observed, where the drain current in the saturation region falls gradually, when drain was stressed above a particular voltage ($V_{DS} > 10$ V in this case). This was commonly referred as negative differential resistance (NDR) in some of the earlier works and was often attributed to presence of bulk traps in GaN buffer. In order to analyze how bulk traps affect device characteristics, Gaussian like distribution was considered for acceptor type buffer traps with peak located near AlGaN/AlN interface and it spreads into the Channel region, as depicted in Fig. 8(a). As no compensation doping was present in the device discussed here, the intrinsic and defect generated traps are considered. These are believed to be maximum near the interface with nucleation region and should decrease with increase in buffer thickness, thus giving rise to a Gaussian like profile of Fig. 8. The effect of Acceptor type buffer traps with energy level at $E_C - 0.96$ eV, which is related to dislocations in GaN devices [27], on the device characteristics is shown in Fig. 8(b). It shows that increasing buffer trap concentration does not contribute to negative differential conductance, rather it reduces the saturation current of the device, which can be attributed to reduced carrier concentration in the channel region. For completeness, the trap energy was also varied from $E_C - 0.5$ eV to $E_C - 2.9$ eV, covering the energy level for C ($E_C - 2.5$ eV) [18] as well as Fe ($E_C - 0.5$ eV) [17]. The results (not shown here) suggest that irrespective of the trap energy, the trend was similar to that shown in Fig. 8. This suggests that the buffer traps affect the sheet charge density and saturation current of the device; however, doesn't contribute to NDR phenomena. Hence NDR depicted in the characteristics is truly due to self heating effects, as discussed in the next section. It is worth highlighting that effect of traps

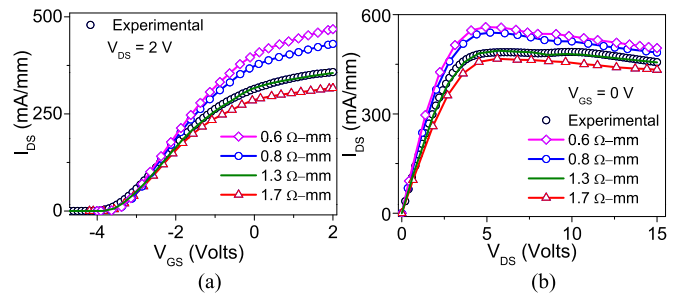


Fig. 9. Effect of Source/Drain contact resistance on (a) $I_{DS} - V_{GS}$ and (b) $I_{DS} - V_{DS}$ characteristics of the device. The simulation data is in complete agreement with experimentally extracted value of $1.3 \Omega\text{-mm}$

can be captured only if carrier heating is considered at the same time to account for trap occupation by hot electrons/holes. Details on carrier dynamics and how to account for hot electrons / hot holes is discussed in later section. In this work, unlike previous works, [16], for the first time we have modeled and studied effect of carrier heating in conjunction with bulk and surface traps.

E. S/D Contacts

Fig. 9 shows impact of S/D contact resistance on the HEMT device characteristics. It is worth highlighting that unlike ohmic contacts, change in contact resistance not only changes the HEMT device's linear region behavior, it affects the characteristics in the saturation region as well. Hence physics based modeling of contacts is very important to predict expected characteristics and its impact on device's circuit performance/figures of merit parameters. In this work, we have used well established metal stack (Ti/Al/Ni/Au) for realizing S/D contacts. In principle, attributed to post deposition higher temperature anneal, the metal layers diffuse deep down to the GaN buffer and make contact to 2-DEG. The Ti present at the bottom forms TiN after anneal, which is presumed to create N vacancies in GaN. The formation of TiN lowers the barrier height at the interface and large N vacancies enhance tunneling at metal-semiconductor interface [29]. In order to model this effect, S/D metal with work function equivalent to TiN (4.1 eV) was used with diffusion depth of 2nm below 2-DEG. In order to capture effect of donor vacancies, a thin n-type doping layer is used at the metal-semiconductor interface around the S/D contacts. Finally, to account for tunneling nature of carrier transport from S/D to channel, equations for Schottky interface were solved. A lumped resistance was then connected in series to this Schottky contact, which is depicted in Fig. 9.

IV. COMPUTATIONAL CHALLENGES & MODELING: CARRIER DYNAMICS AND TRANSPORT

Previous section discussed modeling of various electrostatic aspects of AlGaN/GaN HEMTs. This section extends the discussion to carrier dynamics and transport while considering aspects like mobility, high field effects, hot carriers, self heating etc.

A. Carrier Transport

Carrier transport in a semi-classical system is often modeled using carrier mobility, which is affected by a combination of various different scattering mechanisms, depending on the device structure and materials used. Acoustic phonon scattering, non-polar and polar optical phonon scattering, ionized impurity scattering, piezoelectric scattering, and alloy scattering are major scattering mechanisms for AlGaIn/GaN HEMTs [30]–[34]. Among these optical phonon scattering is noted to be the dominant scattering mechanism at room temperature [35], [36] in GaN HEMTs. In this work these scattering effects are accounted using the models and GaN transport parameters proposed by Arora *et al.* in [37] and Farahmand *et al.* [38], respectively. Model given below, as adopted from [38], reasonably approximates the low field mobility

$$\mu_0(T, N) = \mu_{\min} \left(\frac{T}{300} \right)^{\beta_1} + \frac{(\mu_{\max} - \mu_{\min}) \left(\frac{T}{300} \right)^{\beta_2}}{1 + \left[\frac{N}{N_{\text{ref}} \left(\frac{T}{300} \right)^{\beta_3}} \right]^{\alpha(T/300)^{\beta_4}}}. \quad (3)$$

Here T is lattice temperature, N is total doping density, N_{ref} is the reference concentration and account for mobility degradation at higher concentrations, α is an exponential factor that controls slope around $N = N_{\text{ref}}$, μ_{\min} & μ_{\max} are the minimum and maximum expected mobility values and $\beta_1, \beta_2, \beta_3$ & β_4 take into account the temperature dependence of minimum expected mobility, lattice scattering, ionized impurity scattering and concentration dependent mobility, respectively. In this work these parameters are adopted from [38], which were extracted using Monte Carlo simulations and offer good agreement with mobility measured.

As modeled above, at lower electric fields, accelerated electrons thermalize due to optical phonon scattering; however, as the electric field increases, the same is no longer dominant. At higher electric fields, in AlGaIn/GaN HEMTs, carrier velocity or mobility is governed by inter valley scattering [39], which causes electrons to transfer to higher energy conduction band valley once electrons gain sufficient energy. The transferred electrons have higher effective mass and hence reduced mobility and carrier velocity. This leads to a negative differential mobility at higher fields. Once all the states in the upper valley are occupied, the electrons can no longer jump to higher energy sub-band, which stops the electron transfer and results in a constant/saturated carrier velocity at very high fields. This behavior was modeled by Farahmand *et al.* [38], which is adopted in this work while using model parameters extracted from Monte Carlo simulations [38]:

$$\mu = \frac{\mu_0(T, N) + v_{\text{sat}} \frac{E^{n_1-1}}{E_C^{n_1}}}{1 + a \left(\frac{E}{E_C} \right)^{n_2} + \left(\frac{E}{E_C} \right)^{n_1}} \quad (4)$$

where μ_0 is the low field mobility approximated by eq. (3), v_{sat} & E_C are related to saturated velocity and critical field required for electron transfer, a, n_1 & n_2 are fitting parameters, extracted using Monte Carlo simulations. The device characteristics shown in Fig. 10 clearly highlight the relevance of high

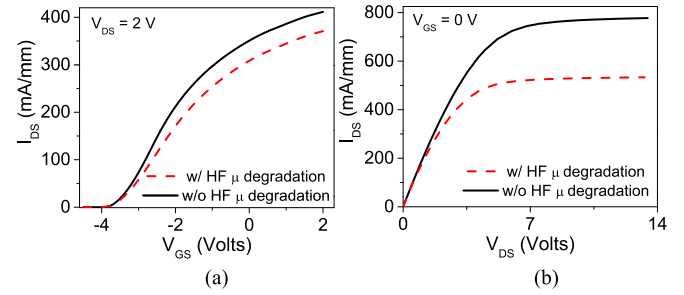


Fig. 10. Effect of high field mobility degradation on (a) $I_{DS} - V_{GS}$ and (b) $I_{DS} - V_{DS}$ characteristics of the device.

field effects. It shows drastic reduction of the drain current, in the presence of high field effects, which is attributed to reduced carrier velocity and hence mobility at higher fields. It is worth highlighting that normal electric field doesn't affect the carrier transport as the 2-DEG is slightly away from AlGaIn/GaN interface, attributed to quantum confinement. Finally, to account for velocity overshoot, carrier heating must be modeled, which is explained in later sub-sections.

B. Gate Stack Modeling

Beside HEMT's overall leakage characteristics, modeling gate leakage is equally important for device's reliability and to account for effects like RF dispersion as well as gate/drain lag. The focus of this paper is on Schottky gate as modeling leakage through Schottky gate is relatively non-trivial compared to MIS-HEMT. Earlier works suggest Fowler Nordheim (FN) tunneling with Poole-Frenkel emission to be responsible for leakage under reverse bias condition [40], while forward bias current is primarily due to thermionic emission. We for the first time have accounted gate to 2-DEG coupling, which we found to contribute to a significant fraction of gate current. To account tunneling effects, non-local tunneling is considered in this work. Nonlocal tunneling was earlier discussed by Jeong *et al.* [41], which has used WKB approximation for calculating tunneling probability. Nonlocal tunneling used in this work, as explained in [19] takes into account the tunneling current dependence on band edge profile along the entire tunneling path. Moreover, impact of surface states/traps is also modeled in this work, which can alter the surface potential and can provide additional leakage paths for the gate current. While earlier works have assumed presence of surface traps [6]–[8], [13], [42], however they were modeled using a fixed surface trap density and energy, without considering their impact on gate leakage. Another work [9] has considered effect of surface traps on the gate leakage, however, by modeling it as a fixed charge, which only alters the Schottky barrier height. These approaches neglect trapping/de-trapping phenomena expected due to presence of surface traps. This work for the first time examines effect of surface traps on gate leakage, as shown in Fig. 11. Fig. 11 suggests that gate leakage increases as the trap energy moves closer to conduction band and/or when trap density increases in general. The earlier increases the ionization probability, which enhances the tunneling. For devices realized in this work with a Schottky gate

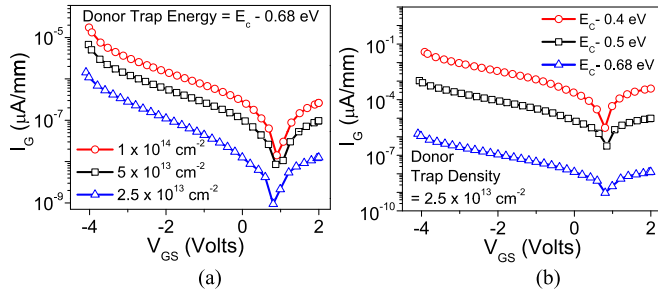


Fig. 11. Effect of Surface trap (a) density and (b) energy on the gate leakage characteristics of the device. The surface trap energy shown is with respect to the Conduction band energy (E_C).

workfunction of 5.15 eV, the estimated surface trap density was found to be $2.39 \times 10^{13} \text{ cm}^{-2}$ with energy $E_C - 0.15 \text{ eV}$. In Section III.C, trap density of 1×10^{14} with energy of $E_C - 0.6 \text{ eV}$ were assumed, which is related to N vacancy in GaN [27] and is more likely to be present. However, these deep traps are unable to explain gate leakage characteristics, which suggests the traps to be at an energy of $E_C - 0.15 \text{ eV}$ which is closely related to the energy of surface states ($E_C - 0.12 \text{ eV}$) in n-GaN [27]. It is worth highlighting that this change in trap density and energy does not cause any significant change in the DC characteristics of the device.

This gives an excellent agreement with the measured characteristics, except for $V_{GS} > 0.8$, which suggests presence of a different leakage path or mechanism. As gate is driven positive, the electrons should now be transported into the gate via tunneling or thermionic emission. Given that the cap layer is effectively depleted of any free carriers by surface states, the probability of such a transmission is very low, resulting in a lower current in the forward direction as compared to reverse current through gate. Certainly thermionic emission from GaN cap to metal gate is not sufficient to explain the high forward gate leakage current and therefore one needs to closely look into the device geometry and model it. A closer look reveals gate metal to 2-DEG coupling through the MESA region as the gate metal over GaN cap extends to gate pad, which is over the MESA region. This direct coupling reduces the built-in potential required for the side diode to conduct [43], which leads to an early forward leakage current. In order to capture this leakage component, mixed mode simulations were performed with a MESA diode parallel to HEMT's gate and source terminals. Fig. 12(a) shows that the extension proposed above for gate stack modeling offers an excellent match with experiments for complete range of gate voltage. It's worth highlighting that the extracted Schottky barrier height of the MESA diode was found to be 0.75 eV higher compared to HEMT's Schottky gate. This could be attributed to slanted MESA trench profile and trap states present at the gate/2-DEG interface.

C. Lattice and Carrier Heating: Impact on Carrier Transport

Attributed to very high power operation, GaN HEMTs are expected to experience observable lattice heating. If the heat energy is not properly removed from the system, it builds hot

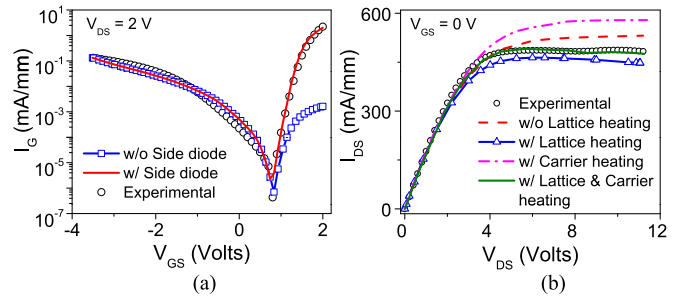


Fig. 12. (a) Computed gate leakage characteristics and (b) $I_{DS} - V_{DS}$ characteristics of the device. For both the computations a surface trap density of $2.39 \times 10^{13} \text{ cm}^{-2}$ at an energy of $E_C - 0.15 \text{ eV}$ is considered.

spot and can severely impact the device performance. This requires physics based modeling of lattice heating with appropriate thermal boundary conditions, which however was neglected in earlier works [6]–[10], [12], [13]. In this work lattice heating and its impact on carrier transport was accounted using the methodology proposed by Wachutka *et al.* [44], [45]. In addition to lattice heating, as the device operates under very high electric fields, hot carrier generation can't be avoided. The heated electrons on one hand leverage improved carrier transport because of velocity overshoot; however on the other hand, it can disturb the trap occupation dynamics as well as can create new traps. Any change in the occupation of surface and/or buffer traps is reflected in 2-DEG density, as discussed in the previous sections. While Wang *et al.* had considered hot electron effect in their work [16], its role in conjunction with surface and/or bulk buffer traps together with lattice heating, was never given importance before. In this work the carrier temperature (T_n) dependent carrier transport for electrons was accounted using transport model proposed by Stratton *et al.* [46] and Apanovich *et al.* [47]:

$$\vec{J}_n = \mu_n (n \nabla E_C + k T_n \nabla n - n k T_n \nabla \ln \gamma_n - 1.5 n k T_n \nabla \ln m_n)$$

Here $\gamma_n = (n/N_C) \exp(-\frac{E_{F,n} - E_C}{kT})$, N_C is the effective density of states, m_n and m_p are electron and hole effective masses, respectively. Finally, the effect of carrier energy on mobility is captured by replacing electric field (E) in eq. (4) by [47]:

$$E = \sqrt{\frac{\max(E_n - E_0, 0)}{\tau_{e,n} q \mu_n}} \quad (5)$$

where $E_0 = 3kT/2$ is the equilibrium thermal energy, $E_n = 3kT_n/2$ is the average electron energy, and $\tau_{e,n}$ is the energy relaxation time.

Fig. 12(b) shows incorporation of lattice and carrier heating significantly affects the device characteristics. If only carrier heating is accounted, simulations overestimate the current, when compared to iso-thermal case, which is attributed to over estimated carrier velocity or mobility. On the other hand, if only lattice heating is considered, simulations underestimate the drain current, which is attributed to significantly mobility degradation and missing energy exchange from phonon to electrons. Finally, figure depicts excellent agreement with experiments when lattice as well as carrier heating was accounted at the same time.

V. CONCLUSION

We found and demonstrated that the presence of unique polarization charges across various epitaxial interfaces significantly affects the energy band profile and attributes to the parasitic charges along with sheet charge density. This finding has justified the importance of inclusion of polarization charge at all the material interfaces unlike ignored in previous works. We have presented for the first time that the Surface states modeled as donor type traps, significantly affects the sheet charge density, device characteristics and gate leakage. Moreover, it was shown that gate leakage calibrated as presented in this work provides a good measure for determining the surface donor trap parameters. High forward gate leakage current through the Schottky gate was found to be contributed by side / MESA diode. The S/D contacts were modeled using a Schottky interface while accounting the barrier tunneling at the S/D contact. The impact of contact resistance on linear as well as saturation characteristics revealed the modeling of AlGaIn/GaN HEMT contacts using a fixed (ohmic) contact resistance gives misleading results. This work further highlights importance of physics based modeling, while accounting for barrier tunneling through the Schottky interface, of S/D contacts in GaN HEMTs. It was found that the negative differential resistance is only due to self heating in the device, and not attributed to surface or bulk traps. Finally, it was found that the lattice heating under estimates the current, whereas carrier heating overestimates it. Hence accounting lattice heating, carrier heating in conjunction with buffer and surface traps are necessary to accurately model device characteristics.

REFERENCES

- [1] M. Shrivastava, M. S. Baghini, A. B. Sachid, D. K. Sharma, and V. R. Rao, "A novel and robust approach for common mode feedback using IDDQ FinFET," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3274–3282, Nov. 2008.
- [2] M. Shrivastava, M. S. Baghini, D. K. Sharma, and V. R. Rao, "A novel bottom spacer FinFET structure for improved short-channel, power-delay, and thermal performance," *IEEE Trans. Electron Devices*, vol. 57, no. 6, pp. 1287–1294, Jun. 2010.
- [3] M. Shrivastava, H. Gossner, and V. Ramgopal Rao, "A novel drain-extended FinFET device for high-voltage high-speed applications," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1432–1434, Oct. 2012.
- [4] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part I: Mixed-signal performance of various high-voltage drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.
- [5] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part II: A novel scheme to optimize the mixed-signal performance and hot-carrier reliability of drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 458–465, Feb. 2010.
- [6] J. M. Tirado, J. L. Sánchez-Rojas, and J. Izpura, "Trapping effects in the transient response of AlGaIn/GaN HEMT devices," *IEEE Trans. Electron Devices*, vol. 54, no. 3, pp. 410–417, Mar. 2007.
- [7] G. Meneghesso *et al.*, "Surface-related drain current dispersion effects in AlGaIn-GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1554–1561, Nov. 2004.
- [8] M. Faqir, G. Verzellesi, G. Meneghesso, E. Zanoni, and F. Fantini, "Investigation of high-electric-field degradation effects in AlGaIn/GaNHEMTs," *IEEE Trans. Electron Devices*, vol. 55, no. 7, pp. 1592–1602, Jul. 2008.
- [9] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura, and T. Ogura, "Influence of surface defect charge at AlGaIn-GaN-HEMT upon Schottky gate leakage current and breakdown voltage," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 159–164, Feb. 2005.
- [10] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaIn/GaNhigh electron mobility transistors using a field plate," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1515–1521, Aug. 2001.
- [11] W. Saito *et al.*, "High breakdown voltage AlGaIn-GaN power-HEMT design and high current density switching behavior," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Jan. 2004.
- [12] E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl, and G. Tränkle, "Punchthrough-voltage enhancement of AlGaIn/GaN HEMTs using Al-GaN double-heterojunction confinement," *IEEE Trans. Electron Devices*, vol. 55, no. 12, pp. 3354–3359, Dec. 2008.
- [13] T. Palacios *et al.*, "Influence of the dynamic access resistance in the gm and FT linearity of AlGaIn/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 52, no. 10, pp. 2117–2123, Oct. 2005.
- [14] W. Saito *et al.*, "Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1825–1830, Aug. 2007.
- [15] G. Longobardi *et al.*, "Impact of donor traps on the 2DEG and electrical behavior of AlGaIn/GaN MISFETs," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 27–29, Jan. 2014.
- [16] X. D. Wang, W. D. Hu, X. S. Chen, and W. Lu, "The study of self-heating and hot-electron effects for AlGaIn/GaN double-channel HEMTs," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1393–1401, May 2012.
- [17] M. J. Uren, J. Moreke, and M. Kuball, "Buffer design to minimize current collapse in GaN/AlGaIn HFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 12, pp. 3327–3333, Dec. 2012.
- [18] G. Verzellesi *et al.*, "Influence of buffer carbon doping on pulse and AC behavior of insulated-gate field-plated power AlGaIn/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 443–445, Apr. 2014.
- [19] *User Manual, Version J-2014.09*, Synopsys TCAD Sentaurus, Synopsys, San Jose, CA, USA, 2014.
- [20] L. Shen *et al.*, "AlGaIn/AlN/GaNhigh-power microwave HEMT," *IEEE Electron Device Lett.*, vol. 22, no. 10, pp. 457–459, Oct. 2001.
- [21] O. Ambacher *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face Al-GaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, 1999. [Online]. Available: <http://scitation.aip.org/content/aip/journal/jap/85/6/10.1063/1.369664>
- [22] M. Ancona and G. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev. B*, vol. 39, no. 13, pp. 9536–9540, 1989.
- [23] M. Ancona and H. Tiersten, "Macroscopic physics of the silicon inversion layer," *Phys. Rev. B*, vol. 35, no. 15, pp. 7959–7965, 1987.
- [24] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaIn/GaN heterostructure field effect transistors," *Appl. Phys. Lett.*, vol. 77, no. 2, pp. 250–252, 2000. [Online]. Available: <http://scitation.aip.org/content/aip/journal/apl/77/2/10.1063/1.126940>
- [25] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaIn/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268–270, Jun. 2000.
- [26] J. W. Chung *et al.*, "Gate-recessed InAlN/GaN HEMTs on SiC substrate with passivation," *IEEE Electron Device Lett.*, vol. 30, no. 9, pp. 904–906, Sep. 2009.
- [27] D. Bisi *et al.*, "Deep-level characterization inGaN HEMTs-Part I: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013.
- [28] G. Longobardi *et al.*, "Impact of donor traps on the 2DEG and electrical behavior of AlGaIn/GaN MISFETs," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 27–29, Jan. 2014.
- [29] Z. Fan, S. N. Mohammad, W. Kim, Ö. Aktas, A. E. Botchkarev, and H. Morkoç, "Very low resistance multilayer Ohmic contact to n-GaN," *Appl. Phys. Lett.*, vol. 68, no. 12, pp. 1672–1674, 1996.
- [30] R. Tülek *et al.*, "Comparison of the transport properties of high quality AlGaIn/AlN/GaN and AlInN/AlN/GaN two-dimensional electron gas heterostructures," *J. Appl. Phys.*, vol. 105, no. 1, 2009, Art. no. 013707.
- [31] O. Celik, E. Tiras, S. Ardali, S. Lisesivdin, and E. Ozbay, "Determination of the LO phonon energy by using electronic and optical methods in AlGaIn/GaN," *Open Phys.*, vol. 10, no. 2, pp. 485–491, 2012.
- [32] D. Zanato, S. Gokden, N. Balkan, B. Ridley, and W. Schaff, "The effect of interface-roughness and dislocation scattering on low temperature mobility of 2D electron gas in GaN/AlGaIn," *Semicond. Sci. Technol.*, vol. 19, no. 3, pp. 427–432, 2004.
- [33] W. Knap *et al.*, "Influence of dislocation and ionized impurity scattering on the electron mobility in GaN/AlGaIn heterostructures," *J. Crystal Growth*, vol. 281, no. 1, pp. 194–201, 2005.

- [34] S. Lisesivdin, S. Acar, M. Kasap, S. Ozcelik, S. Gokden, and E. Ozbay, "Scattering analysis of 2DEG carrier extracted by QMSA in undoped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ heterostructures," *Semicond. Sci. Technol.*, vol. 22, no. 5, pp. 543–548, 2007.
- [35] L. Hsu and W. Walukiewicz, "Electron mobility in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures," *Phys. Rev. B*, vol. 56, no. 3, pp. 1520–1528, 1997.
- [36] T. Fang, R. Wang, H. Xing, S. Rajan, and D. Jena, "Effect of optical phonon scattering on the performance of GaN transistors," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 709–711, May 2012.
- [37] N. D. Arora, J. R. Hauser, and D. J. Roulston, "Electron and hole mobilities in silicon as a function of concentration and temperature," *IEEE Trans. Electron Devices*, vol. 29, no. 2, pp. 292–295, Feb. 1982.
- [38] M. Farahmand *et al.*, "Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: Binaries and ternaries," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 535–542, Mar. 2001.
- [39] F. Abou El-Ela and A. Mohamed, "Electron transport characteristics of wurtzite GaN," *ISRN Condensed Matter Phys.*, vol. 2013, 2013, Art. no. 654752.
- [40] S. Turuvekere, D. S. Rawal, A. DasGupta, and N. DasGupta, "Evidence of Fowler–Nordheim tunneling in gate leakage current of AlGaN/GaN HEMTs at room temperature," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4291–4294, Dec. 2014.
- [41] M. Jeong, P. M. Solomon, S. E. Laux, H. S. P. Wong, and D. Chidambarrao, "Comparison of raised and Schottky source/drain mosfets using a novel tunneling contact model," in *Proc. Tech. Digest., Int. Electron Devices Meet.*, 1998, Dec. 1998, pp. 733–736.
- [42] F. Medjdoub *et al.*, "Barrier-layer scaling of InAlN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 422–425, May 2008.
- [43] J. G. Lee, B. R. Park, C. H. Cho, K. S. Seo, and H. Y. Cha, "Low turn-on voltage AlGaIn/GaN-on-Si rectifier with gated ohmic anode," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 214–216, Feb. 2013.
- [44] G. Wachutka, "An extended thermodynamic model for the simultaneous simulation of the thermal and electrical behavior of semiconductor devices," in *Proc. 6th Int. NASECODE Conf.*, 1989, pp. 409–414.
- [45] G. K. Wachutka, "Rigorous thermodynamic treatment of heat generation and conduction in semiconductor device modeling," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 9, no. 11, pp. 1141–1149, Nov. 1990.
- [46] R. Stratton, "Diffusion of hot and cold Electrons in semiconductor barriers," *Phys. Rev.*, vol. 126, pp. 2002–2014, Jun. 1962. [Online]. Available: <http://link.aps.org/doi/10.1103/PhysRev.126.2002>
- [47] Y. Apanovich *et al.*, "Numerical simulation of submicrometer devices including coupled nonlocal transport and nonisothermal effects," *IEEE Trans. Electron Devices*, vol. 42, no. 5, pp. 890–898, May 1995.



Vipin Joshi received the M.Tech. degree in VLSI design from Malaviya National Institute of Technology, Jaipur, India. He is currently working toward the Ph.D. degree in electrical engineering from the Indian Institute of Technology Jodhpur, Jodhpur, India. His current research interests include simulation and modeling of GaN HEMTs and device-circuit codesign.



Ankit Soni received the B.Tech. degree in electronics and communication engineering from the National Institute of Technology, Hamirpur, Himachal Pradesh, India. Since 2015, he has been working toward the Ph.D. degree at the Indian Institute of Science, Bangalore, India. His research interests include computation modeling of GaN HEMT and design and fabrication of high power HEMTs.



Shree Prakash Tiwari (M'11–SM'16) received the Ph.D. degree in electrical engineering from Indian Institute of Technology (IIT) Bombay, Mumbai, India, in 2008. From 2008 to 2011, he was a Postdoctoral Fellow at the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA. In 2011, he joined IIT Jodhpur, Jodhpur, India, as an Assistant Professor of electrical engineering. His research interests include exploration of high performance transistor devices with organic and inorganic semiconductors, and flexible electronics.



Mayank Shrivastava (S'09–M'10–SM'16) received the Ph.D. degree from the Indian Institute of Technology (IIT) Bombay, Mumbai, India, in 2010. He is currently an Assistant Professor in the Department of Electronic Systems Engineering, Indian Institute of Science Bangalore, India. From April 2008 to October 2008 and May 2010 to July 2010, he held short term Visiting Positions in Infineon Technologies, Munich, Germany. Between 2010 and 2013, he was with Infineon Technologies, East Fishkill, NY, USA; Intel Mobile Communications, Hopewell Junction, NY, USA; and Intel Corporation, Mobile and Communications Group, Munich, Germany. In 2013, he joined the Indian Institute of Science as an Assistant professor, where he has established Advance Nanoelectronic Device and Circuit Research Group. He has more than 60 publications in international journals and conferences and 30 patents in the areas of electron devices and nanoelectronics. He received first Indian Section of American TR35 Award 2010 and the IEEE EDS Early Career Award for year 2015. In addition to this, he has received several other awards and honours including Excellence Award for his Ph.D. thesis in 2010, the Best Paper Award from Intel Asia Academic Forum 2008, and the Industrial Impact Award from IIT Bombay in 2008. To get more information about his current research interests, publications, and patents, visit: <http://www.dese.iisc.ernet.in/people/mayank/>