Drain Extended Tunnel FET—A Novel Power Transistor for RF and Switching Applications

Mayank Shrivastava, *Senior Member, IEEE*

***Abstract*— For the first time, a novel drain-extended tunnel FET (DeTFET) device is disclosed in this paper, while addressing the need for high-voltage/high-power devices for system-on-chip and automotive applications in beyond FinFET technology nodes. Operation of the proposed DeTFET device is presented with physics of band-to-band tunneling and associated carrier injection. Device's intrinsic (dc/switching), analog, and RF performance is compared with the state-of-the-art drain-extended nMOS (DeNMOS) device. The proposed device for 11 V breakdown voltage offers 15× better subthreshold slope, 8× lower off-state leakage, 2× higher on current, and absence of channel length modulation and drain induced barrier lowering, while keeping 2.5× lower threshold voltage. This results into significantly better on resistance for a range of gate voltages, higher transconductance, orders of magnitude higher intrinsic transistor gain, and better RF characteristics, when compared with the DeNMOS device. Finally, device design guidelines are presented and scalability, without affecting breakdown voltage, of the proposed device is compared with the DeNMOS device.**

***Index Terms*— Automotive, drain-extended MOS (DeMOS), FinFET, high power, high voltage, Laterally Diffused MOS (LDMOS), system-on-chip (SoC), tunnel FET.**

I. Introduction

FinFET technology has been predicted to become obsolete beyond 7-nm technology node, if not earlier [1], [2], and is potentially expected to be replaced by tunnel FETs [3]. Though the tunnel FET technology has shown a great potential to outperform FinFETs, it has yet not seen the required industrial maturity for commercialization. However, as there is no other technology option present, tunnel FETs have acquired the presence in the technology roadmap and is expected to be seen in semiconductor products after the year 2022 [4].

System-on-chip (SoC) design in FinFET and beyond FinFET nodes is an open question. Besides technological challenges, design rule limitations, and lack of advanced Electrostatic Discharge (ESD) protection concepts, absence of ultrahigh voltage (UHV) device concepts for 5–20 V operations is the key limiter [5]–[8]. Note that the SoC design requires the integration of logic, analog, RF, and high-voltage functionalities on the same chip. This mandates processing of core, analog, RF, and high voltage/high power devices in the same flow [5]. The other emerging application of tunnel FET like low-power technology is Internet of Things [9], which requires integration of SoC and sensors. In planar CMOS, LDMOS or drain extended MOS (DeMOS) devices are used for UHV applications, which caters to on-chip functionalities like high-voltage level shifters, line drivers, USB, RF power amplifier (PA), charge pump for camera flash, and dc–dc convertors [10], [11].

Requirement of LDMOS or DeMOS like UHV devices has been addressed for FinFETs up to a certain extent [12], [13]; however, the same for the tunnel FET technology was never addressed. It is also worth investigating how LDMOS or DeMOS devices would behave if thermionic injection of majority carriers is replaced by source-to-channel tunneling of minority carriers, which is the key enabler of the tunnel FET technology.

This paper presents a novel drain-extended tunnel FET (DeTFET) concept with a potential to replace drain-extended MOSFETs and similar high-voltage/high-power MOSFET designs. This paper is arranged as follows. Section II briefs about the computational setup, calibration approach, and DeMOS device for reference and comparisons. Section III discloses the proposed DeTFET device, its operation, and physics. Moreover, a comparison of device's switching, analog, and RF performances with the DeMOS device is also discussed in Section III. Device design and scaling details are presented in Section IV. Finally, the proposal and findings are concluded in Section V.

II. Model Calibration and TCAD Framework

Computation of a high-voltage device requires precise calibration of high field mobility and breakdown models. Furthermore, to accurately capture band-to-band tunneling (BTBT) phenomena—the operating principle of tunnel FETs—sophisticated calibration of BTBT and recombination models is required. This paper uses a well-calibrated setup for high-voltage devices, which has been greatly described in our earlier works [13]–[15]. To summarize, drift diffusion transport model was used while accounting for high field mobility degradation, surface scattering, impact ionization, SRH, and auger recombination. This setup was further extended with nonlocal BTBT model using two-band dispersion, quantum confinement (QC), thin layer mobility degradation, and bandgap widening, and field-enhanced trap-assisted tunneling

Manuscript received August 27, 2016; revised October 30, 2016; accepted November 17, 2016. Date of publication December 28, 2016; date of current version January 20, 2017. This work was is encouraged by the IMPRINT Program of the Government of India. The review of this paper was arranged by Editor B. Zhang.

The author is with the Advance Nanoelectronic Device and Circuit Research Laboratory, Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: mayank@dese.iisc.ernet.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2016.2636920

0018-9383 © 2016 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:26:22 UTC from IEEE Xplore. Restrictions apply.

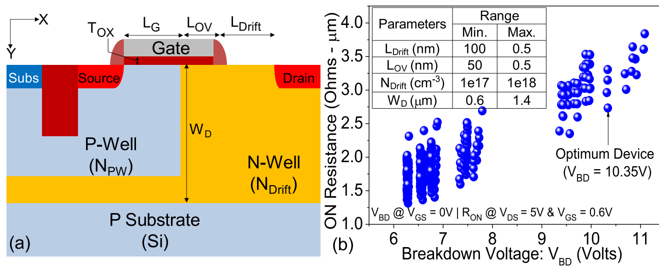

Fig. 1. (a) Schematic of the state-of-the-art CMOS DeMOS device—as used in this paper for comparison. (b) R_{ON} versus V_{BD} tradeoff extracted from a detailed DOE used to realize the best DeMOS device for one-to-one comparison. Inset: parameters used for the DOE. E_{OT}, N_{PW}, and L_G were 0.6 nm, 5×10^{17} cm^{-3}, and 200 nm, respectively, which were kept fixed for all simulations in the DOE. The optimum of the device was found for $L_{Drift} = 300$ nm, $L_{OV} = 100$ nm, $N_{Drift} = 1 \times 10^{17}$ cm^{-3}, and $W_D = 1\,\mu$m.

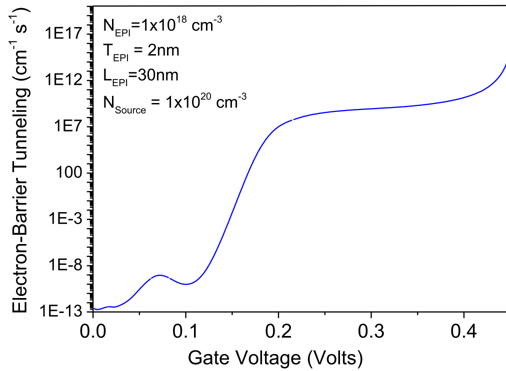

Fig. 2. Electron barrier tunneling versus gate voltage, integrated over the entire tunneling cross section.

models, which is explained in detail in our recent work [16]. Strain at Si–SiGe interface has not been considered in the device computations. Completeness of simulation setup/band splitting due to QC, its impact on BTBT, and threshold voltage shift can be validated by multiple branches in the electron barrier tunneling versus V_{GS} (integrated over the entire tunneling cross section), which is shown in Fig 2.

Strain at Si/SiGe interface strongly depends on Epi-growth conditions. It is established that strain at Si/SiGe improves the TFET performance. Due to the unavailability of precise growth conditions at this stage and hence the strain data, the idea was to do an underestimated prediction, and therefore skip strain at Si/SiGe. Computational studies in this paper were performed using the Synopsys Sentaurus TCAD tool.

For one to one comparison of the proposed device with the state-of-the-art DeMOS device, a non-STI DeMOS device, as depicted in Fig. 1(a), was realized through an extended design-of-experiment (DOE). DOE details are given in Fig. 1(b). It is worth highlighting that the effective oxide thickness (EOT) was considered to be 0.6 nm, keeping in mind sub-7-nm CMOS technology roadmap [3]. For non-STI device realization using the DOE method, ON-resistance (R_{ON}) versus breakdown voltage (V_{BD}) tradeoff was considered in order to maximize V_{BD} and minimize R_{ON}. Furthermore, devices with early quasi-saturation [17] were discarded to maximize transconductance (g_m) and output resistance ($1/g_{ds}$). Finally, ON-current (I_{ON}) was maximized, while keeping leakage current (I_{OFF}) below 10 pA/μA.

III. Proposed Drain Extended Tunnel FET

Fig. 3(a) shows the schematic of the proposed DeTFET device. For better understanding, the proposed device can be seen in three parts: drain-side region (right of cutline C–C'), source-side region (left of cutline B–B'), and channel region (between cutline B–B' and C–C'). The drain-side and channel regions of the proposed device remain the same as the drain-extended NMOS (DeNMOS) device [Fig. 1(a)]. However, the source-side region of the proposed device consists of p^+ SiGe source with an n-type Si Epi region sandwiched between the SiGe source and the gate-stack. This enables vertical or area tunneling of minority carriers from SiGe p+ source into n-Epi region under the influence of gate field. The concept of area tunneling is to enable tunneling along the gate electric field while enhancing the tunneling cross-sectional area, which is known since a few years as different terminologies, namely, vertical TFET, STBFET, binary TFET, bilayer TFET, line TFET, green TFET, and so on [16], [18], [19]. The effectiveness of p^+ SiGe source/Si-Epi heterostructure and the gate overlap over the n-type Si Epi region for enhancing BTBT has also been confirmed experimentally and reported in [20].

It is important to stress from the beginning that the idea of the proposed device is not to replace a tunnel FET like beyond FinFET technology devices for low-voltage operation. The key idea behind this invention is to enable tunnel-FET-like technology with high-voltage devices for the development of SoCs, which require high-voltage devices operating from 10 to 40 V. The other aspect of this invention is to change thermionic injection of carriers at the source side of power MOSFETs by BTBT-based carrier injection. The tunnel injection mechanism for power MOSFETs, which conventionally caters to 40–700 V applications, was never discussed in this section.

The proposed device enables area tunneling between SiGe source and Si Epi region, which breaks the barrier imposed by thermionic injection-based carrier transport from source to channel in the case of DeNMOS devices. This principle is shown in Fig. 3(b). Fig. 3(b) shows the conduction and valance band energies along cutline A–A' under ON- and OFF-states. Under OFF-state, the conduction band of n-Epi region is not aligned with the valance band of SiGe p+ source, restricting quantum mechanical tunneling from valance to conduction band, as shown in Fig. 4(c). However, the alignment is clearly evident under the influence of gate field (ON-state), which enables vertical tunneling, as shown in Fig. 4(a) and (b). Fig. 4 shows the barrier tunneling rate of e/h under OFF- and ON-states. It depicts that the barrier tunneling rate under ON-state is over ten orders of magnitude higher than the same under OFF-state. Moreover, the BTBT under ON-state occurs across the entire n-Epi region, sandwiched between SiGe source and gate oxide; unlike the point tunneling under OFF-state condition. Tunneling nature of carrier injection, from source to channel, along with: 1) over ten orders of magnitude difference between barrier tunneling rate under ON- and OFF-state and 2) shift from point tunneling (OFF-state) to area tunneling (ON-state) lead to an excellent ON- to OFF-current ratio with steep subthreshold slope/early turn-ON,

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:26:22 UTC from IEEE Xplore. Restrictions apply.

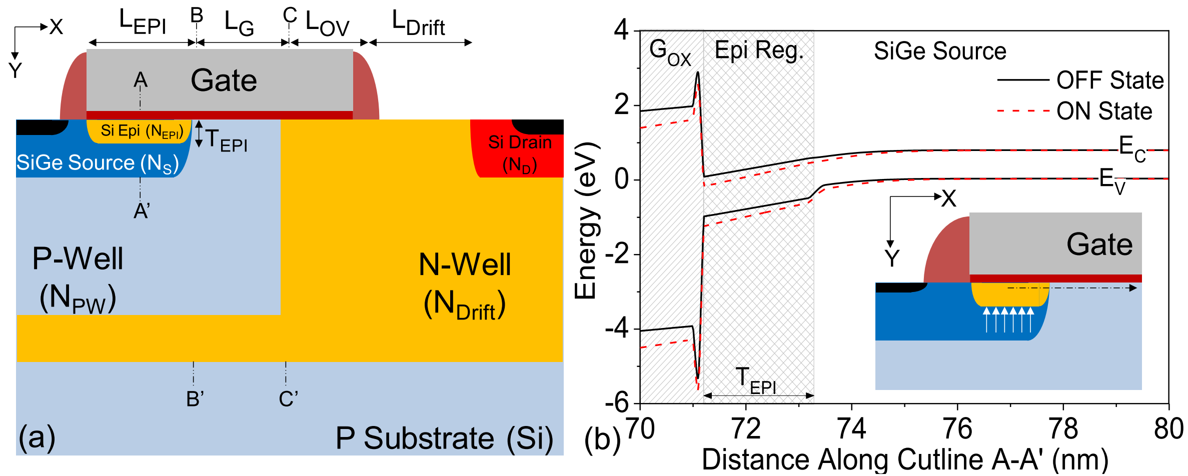

Fig. 3. (a) Schematic of the proposed DeTFET. (b) Conduction and valance band energies versus distance along the cut line A–A' [depicted in Fig. 2(a)] extracted under ON-and OFF-states. S/D doping, junction depth, and Ge% of SiGe source used in all simulations are 1×10^{20} cm^{-3}, 10 nm, and 30%, respectively [16]. DeTFET device, used for comparison with DeNMOS, further has following additional parameters: $L_{EPI} = 30$ nm, $T_{EPI} = 2$ nm, and Epi region doping (N_{EPI}) = 1e18 cm^{-3}. Moreover, the source-to-drain pitch of DeTFET is the same as the optimized DeNMOS device used for comparison.

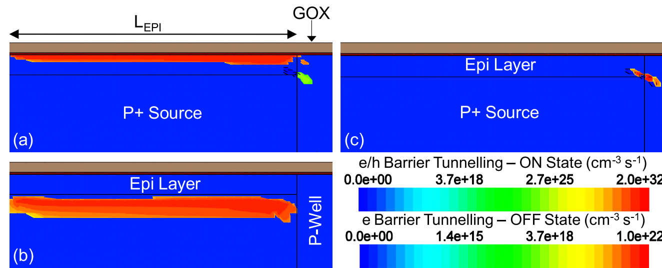

Fig. 4. (a) and (c) e-barrier tunneling rate and (b) h-barrier tunneling rate around SiGe source and Si Epi region in (a) and (b) ON-state and (c) OFF-state.

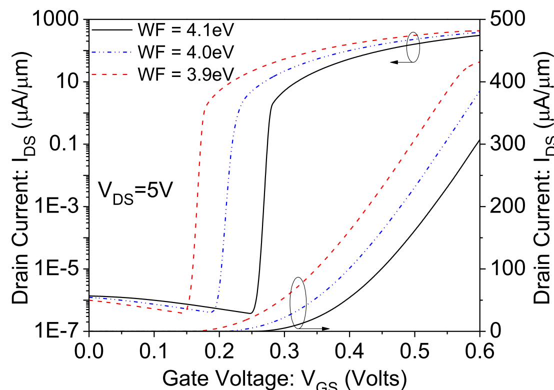

Fig. 5. Drain current versus gate voltage (I_D–V_G) characteristics of the proposed DeTFET device (Log and Linear scale) as a function of gate metal WF. Except a shift in the I_D–V_G characteristics, no other change was observed.

as depicted in Fig. 5. Fig. 5 shows I_D–V_G characteristics of the proposed DeTFET device for different gate metal work functions (WFs). Except a shift in the I_D–V_G characteristics, no other change was observed. For a WF of 3.9 eV, the proposed device is predicted to have OFF-current (I_{OFF}) less than 1 pA/μA, threshold voltage (V_T) = 0.15 V, subthreshold slope less than 5 mV/decade, and ON-current exceeding 300 μA/μm at $V_{GS} = 0.5$ V.

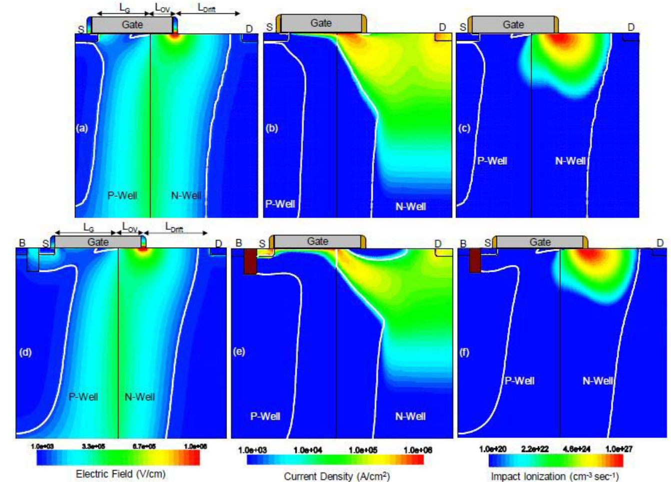

Fig. 6. Comparison of (a) and (d) electric field distribution under OFF-state, (b) and (e) conduction current density under ON-state, and (c) and (f) impact ionization at junction breakdown between DeTFET (a)–(c) and DeNMOS (d)–(f) devices.

It is worth highlighting that the device behavior associated with the drain-side region (right of cutline C–C') and the channel region (between cutline B–B' and C–C') of the proposed DeTFET device remains the same as DeNMOS device, as shown in Fig. 6, except 10% higher breakdown voltage of DeTFET device, which is attributed to the absence of subthreshold leakage and parasitic NPN. Fig. 6 compares electric field profile under OFF-state, current distribution in the drift region under ON-state, and impact ionization under OFF-state at the breakdown voltage. It is evident from Figs. 4 and 6 that the proposed device differs from the conventional device only in terms carrier injection from source to channel, which leads to a significant improvement in the device behavior, device's characteristics, and figure-of-merit (FOM) parameters, as shown in Figs. 7 and 8.

Fig. 7 compares the I_D–V_D and I_D–V_G characteristics of DeTFET and DeNMOS devices, which draws following observations.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:26:22 UTC from IEEE Xplore. Restrictions apply.

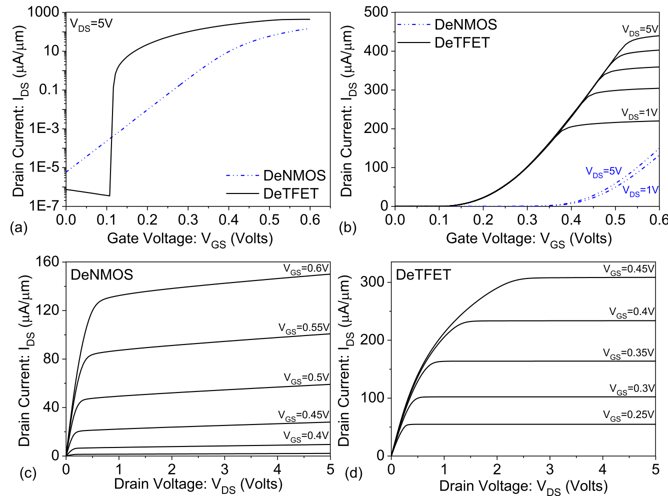

Fig. 7. Comparison of (a) and (b) I_D–V_G and (c) and (d) I_D–V_D characteristics of DeNMOS and DeTFET devices. I_D–V_G characteristics of DeNMOS and DeTFET on (a) log and (b) linear scales. I_D–V_D characteristics of (c) DeNMOS and (d) DeTFET.

1) ON-current and OFF-current of the proposed device are over 2× higher and 8× lower, respectively, than DeNMOS device.
2) Even for lower OFF-current, DeTFET offers a much smaller threshold voltage (0.15 V) and a significantly lower average SS (4mV/decade, extracted over six orders of current) when compared with DeNMOS device (0.35 V and 65 mV/decade, respectively), which is attributed to the tunneling nature of carrier injection from source to channel.
3) DeTFET device does not show threshold voltage shift as a function of drain voltage, unlike small shift present in DeNMOS device characteristics, which reveals the absence of drain-induced barrier lowering (DIBL) in DeTFET device.

This can help scaling the channel length further. First, output characteristics of the DeTFET in the saturation region is almost flat unlike DeNMOS device, which shows the absence of channel length modulation in the proposed device. This is attributed to the tunneling nature of current injection, which makes the carrier injection from source to drain almost independent of drain field. Second, higher output current swing in DeTFET for smaller range of input/gate voltage, compared with DeNMOS device.

The differences and advantages presented above attribute to the significantly reduced ON-resistance of DeTFET device, for a wide range of gate voltage, compared with DeNMOS device, [Fig. 8(a)]. Furthermore, DeTFET device offers 1.5× higher transconductance and orders of magnitude higher intrinsic transistor gain than the DeNMOS device, as shown in Fig. 8(b). Fig. 8(c) and (d) shows that the DeTFET device offers slightly better cutoff frequency (F_t), maximum oscillation frequency ($F_{\max}$), and RF power gain; however, the peak with respect to gate voltage occurs at much lower gate voltages. This implies that at a given frequency and for a given output RF power level, required input power for DeTFET-based RF PA would be significantly lower than the same

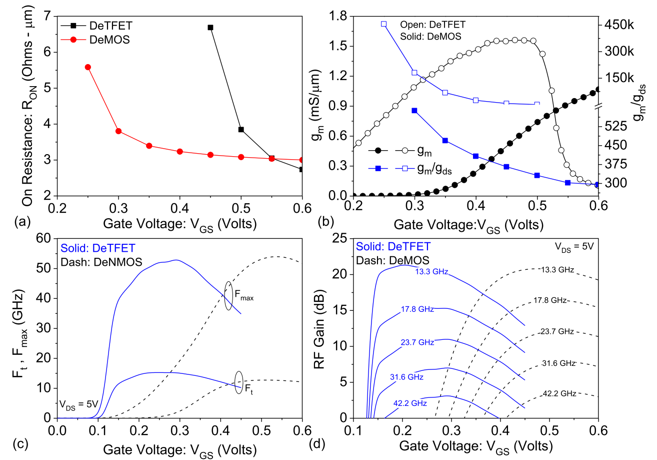

Fig. 8. Comparison of switching, analog, and RF FOM parameters of DeNMOS and DeTFET devices. (a) ON-resistance, (b) transconductance (g_m) and dc gain (g_m/g_{ds}), (c) F_t and $F_{\max}$, and (d) RF gain as a function of gate voltage for both DeNMOS and DeTFET devices.

designed using a DeNMOS device. Hence, one can expect proposed DeTFET-based RF PA to offer higher power added efficiency than the DeNMOS-based RF PA.

It is worth highlighting that the comparison above is done for a similar source-to-drain OFF-state leakage current, not for equal threshold voltage, which is a common practice while comparing TFET device with device having thermionic injection barrier [18], [19]. It is worth highlighting that an equal threshold voltage comparison will be a worst case for DeNMOS device, attributed to its significantly high leakage current and OFF-state power dissipation, in the case of comparable threshold voltage, which is not desirable for switching applications. For RF performance and ON-state comparison, only peak performance parameters (like peak g_m, maximum $F_t/F_{\max}$, and least R_{ON}) are compared, independent of gate voltage at which they were found to be maximum. Hence, the RF/analog performance comparison is independent of threshold voltage. Based on this, one can easily conclude that the proposed DeTFET device is superior in performance when compared with a DeNMOS device, independent of their respective threshold voltages.

IV. Device Design Guidelines and Scaling

This section presents device design guidelines while taking key design parameters into consideration. Moreover, scalability of channel length for DeTFET and DeNMOS is also compared here.

A. Device Design Guidelines

From a device design point of view, there are three unique regions of interest: 1) drain side, i.e., drift region; 2) channel; and 3) source side, i.e., barrier tunneling region. As discussed before, the drift region of the proposed device behaves the same way as the drift region of DeNMOS. Hence, the design guideline for the drain side/drift region can be borrowed from earlier works on DeNMOS [10], [11], [15], [17]. The channel length scaling is discussed in Section IV-B. As far as the source-side region is concerned, there are three critical design parameters, i.e., Epi

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:26:22 UTC from IEEE Xplore. Restrictions apply.

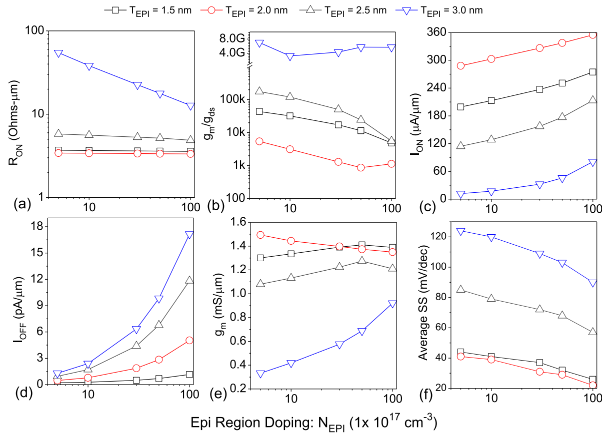

Fig. 9. Impact of Epi region doping and Epi thickness on the device FOM parameters. (a) ON-resistance. (b) Intrinsic transistor gain. (c) ON-current. (d) OFF-current. (e) Transconductance. (f) Average subthreshold slope (calculated over eight decades of current).

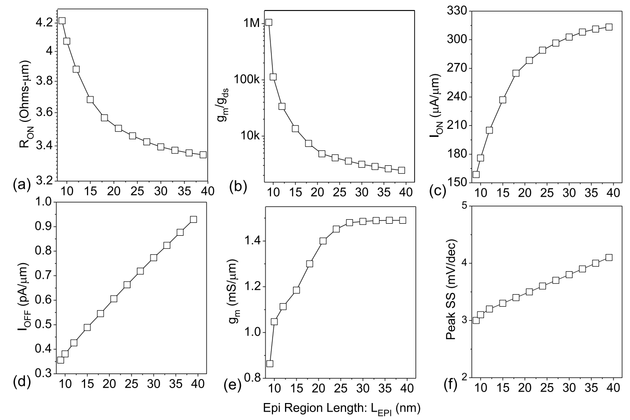

Fig. 11. Impact of Epi region length on the device FOM parameters. (a) ON-resistance. (b) Intrinsic transistor gain. (c) ON-current. (d) OFF-current. (e) Transconductance. (f) Subthreshold slope. Note that the trends are extracted for a fixed L_G.

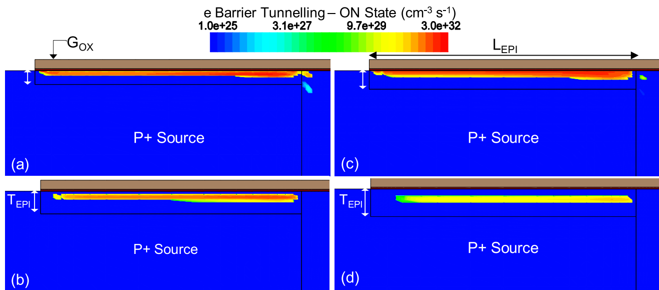

Fig. 10. e-barrier tunneling rate around SiGe source and Si Epi region in ON-state. (a) T_{EPI} = 1.5 nm. (b) T_{EPI} = 2 nm. (c) T_{EPI} = 2.5 nm. (d) T_{EPI} = 3 nm. The maximum tunneling rate was observed for T_{EPI} = 2 nm.

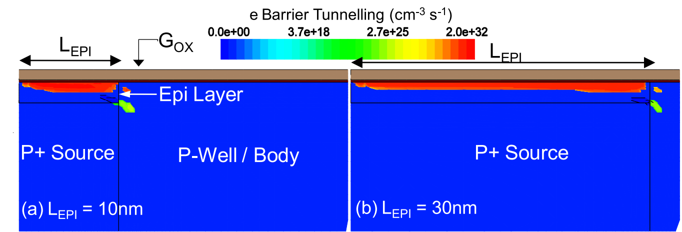

Fig. 12. e-barrier tunneling rate around SiGe source and Si Epi region in ON-state. (a) L_{EPI} = 10 nm. (b) L_{EPI} = 30 nm.

region doping (N_{EPI}), Epi thickness (T_{EPI}), and Epi region length (L_{EPI}). Fig. 9 shows the impact of Epi region doping and Epi thickness on the device FOM parameters. It can be clearly observed that R_{ON} falls as the Epi region doping was increased, which, however, is weak for lower Epi thicknesses and stronger for larger Epi thickness. On the other hand, R_{ON} increases as the Epi thickness was increased above or decreased below 2 nm. This is attributed to a maximum ON-current at T_{EPI} = 2 nm. Increasing N_{EPI} improves the BTBT, which in turn improves the ON-current and transconductance, at the cost of slightly increased S/D leakage current and reduced gain (g_m/g_{ds}). Increasing T_{EPI} above 2 nm reduces the ON-current and transconductance, which is attributed to increased tunneling barrier width. Moreover, reducing the T_{EPI} below 2 nm also reduces the ON-current and transconductance, which, however, is attributed to the reduced number of tunneling states (Fig. 10). Increasing T_{EPI} also suppresses gate control over the tunnel junction, which is evident from the increased I_{OFF} and SS with the increasing T_{EPI}. Fig. 11 shows the impact of Epi region length (L_{EPI}) on the device FOM parameters. Increasing L_{EPI} improves the BTBT cross-sectional area (Fig. 12), and hence increases number of carrier injected into the channel. This improves the ON-current, transconductance and reduces ON-resistance with increasing L_{EPI}, however, at the cost of lower g_m/g_{ds} and slightly higher I_{OFF} and SS.

It is worth highlighting that ON-current saturates to a fixed value at higher L_{EPI}. This is attributed to the maximum current through the device being limited by the channel, which is inversely proportional to the channel length. If the channel length is scaled, which increases the channel current limit, the ON-current as a function of L_{EPI} saturates at higher L_{EPI}. Moreover, source-side design parameters (T_{EPI}, L_{EPI}, and N_{EPI}) have no impact on drain-to-substrate breakdown voltage. It should be noted that SS in Fig. 9(f) is the average SS calculated over eight decades of drain current, whereas the same in Fig. 11(f) is peak SS, which is extracted at sub-nA current. Average SS over eight decades of current is a highly conservative approach, usually not followed in the literature, however, is realistic from switching applications point of view.

B. Channel Length Scaling

This section compares proposed DeTFET's dc, switching, and RF performance with conventional DeNMOS in relation to channel length scaling of these devices. Fig. 13(a) shows that the ON-resistance falls by 5% and 15% for DeTFET and DeNMOS, respectively, as the channel length was scaled down from 250 to 100 nm. This in the case of DeTFET is attributed to reduction in the channel resistance, whereas in the case of DeNMOS, it attributes to improve ON-current [Fig. 13(b)] and reduced channel resistance. It is worth highlighting that, since ON-current of DeTFET is limited by number of electrons tunnel from source to channel, ON-current in the case of DeTFET does not improve by channel length

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:26:22 UTC from IEEE Xplore. Restrictions apply.

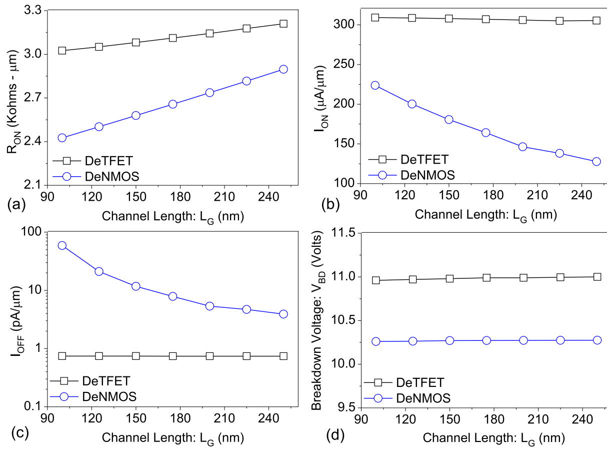

Fig. 13. Comparison of channel length scaling and its effect on DeTFET and DeNMOS device's FOM parameters for switching applications. (a) ON-resistance. (b) ON-current. (c) OFF-current. (d) Breakdown voltage.

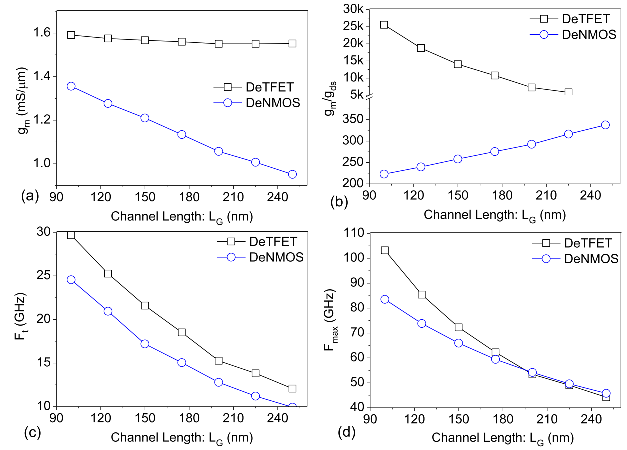

Fig. 14. Comparison of channel length scaling and its effect on DeTFET and DeNMOS device's analog/RF FOM parameters. (a) Transconductance. (b) Intrinsic transistor gain. (c) Cutoff frequency. (d) Maximum oscillation frequency.

scaling for fixed L_{EPI}, unlike DeNMOS device [Fig. 13(b)]. To take advantage of channel length scaling in the case of DeTFET, L_{EPI} has to be increased accordingly.

Similarly, OFF-current is unchanged in the case of a DeTFET, which depicts the absence of channel length modulation and DIBL, unlike the DeNMOS device, which shows increased OFF-current with channel length scaling. Finally, it is worth highlighting that breakdown voltage remains unchanged with channel length scaling. Moreover, for a given channel length and fixed drift region design, DeTFET offers ∼10% higher breakdown voltage than DeNMOS. This is attributed to the absence of subthreshold leakage and parasitic NPN in DeTFET. It is worth highlighting that subthreshold leakage and parasitic NPN present in DeNMOS lowers the intrinsic n-Well to substrate junction breakdown voltage, which are inherently absent in the DeTFET device. It should be noted that R_{ON} in Fig. 13(a) is extracted at $V_{GS} = 0.6$ V, at which DeNMOS R_{ON} was found to be 10% lower than DeTFET. Fig. 13 shows scaling trends; however, do not compare both the devices for a broad operating range. For a fair comparison, it is worth highlighting the trend in Fig. 8(a). It shows that R_{ON} of both the devices at $V_{GS} = 0.55$ are identical. However, below $V_{GS} = 0.55$ V, R_{ON} of DeTFET remains more or less unchanged, whereas R_{ON} of DeNMOS increases exponentially when V_{GS} was scaled. This makes a very big difference for power switching applications, which require as low as possible voltage swing at the gate to reduce dynamic power losses. These trends together validates "$R_{ON} \times V_{BD}$" of DeTFET to be superior compared with the same of DeNMOS for a broad operating range. Fig. 14(a) shows that the DeTFET transconductance does not change with channel length scaling, which is attributed to BTBT-limited channel current. However, DeNMOS shows 40% improvement in transconductance as channel length was scaled down from 250 to 100 nm. In all the cases, DeTFET offers higher transconductance than DeNMOS. Again, to take advantage of channel length scaling in the case of DeTFET, L_{EPI} has to be increased accordingly. Fig. 14(b) shows that the g_m/g_{ds} improves with channel length scaling in the case of DeTFET. This is attributed to significantly improved output characteristics of DeTFET for shorter channel length devices. Unlike this, DeNMOS shows reduced g_m/g_{ds} for shorter channel lengths, which is due to the presence of channel length modulation. For all channel lengths, DeTFET offers orders of magnitude higher g_m/g_{ds} than DeNMOS. Gate-to-drain (miller) capacitance (C_{GD}) of both DeTFET and DeNMOS devices is the same and does not change with the channel length scaling, as the drift region design remains intact when the channel length was scaled. These improvements result DeTFET to offer 20% higher cutoff frequency (F_t) and maximum oscillation frequency (F_{max}), as shown in Fig. 14(c) and (d).

It should be noted that the impact of strain at the Si/SiGe heterostructure was not considered in this paper. However, intrinsic strain at the tunnel interface is expected to further improve the performance of the proposed device [21]. Finally, it is worth highlighting that EOT of 0.6 nm has been chosen in this paper, which is based on scaling roadmap for ultrascaled CMOS technologies. It should be noted that the maximum gate voltage (in general core supply voltage) considered in this paper has been scaled accordingly. For an EOT of 0.6 nm, maximum gate voltage, at which DeTFET offers peak RF/switching performance, is less than 0.4 V. This mitigates any gate leakage concern in DeTFET. However, the same is not true for a DeNMOS device. DeNMOS offers peak switching/RF performance at much higher gate voltage than DeTFET. In ultrascaled technologies, this may give rise to serious gate leakage issues in DeNMOS devices, compared with DeTFET, when biased at peak performance point.

V. Conclusion

High-voltage/high-power devices operating in the range of 5–20 V have become an essential need for system-on-chip designs. While addressing this need for beyond FinFET, SoC, and automotive applications, this paper has disclosed a novel DeTFET device. It was found that the BTBT nature of carrier injection in the proposed device, when compared with thermionic injection in DeNMOS device, leads to several advantages. Higher ON-current, lower leakage with lower threshold voltage, steep subthreshold-slope, higher

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:26:22 UTC from IEEE Xplore. Restrictions apply.

breakdown voltage with lower ON-resistance, and improved RF characteristics of the proposed device make it more attractive for SoC applications as well as automotive applications than its state-of-the-art counterpart. Source engineering was found to be a key to design and realize the proposed device. Finally, the proposed device offers better scalability than the DeNMOS device.

REFERENCES

[1] S.-D. Kim, M. Guillorn, I. Lauer, P. Oldiges, T. Hook, and M.-H. Na, "Performance trade-offs in FinFET and gate-all-around device architectures for 7nm-node and beyond," in *Proc. IEEE SOI-3D-Subthreshold Microelectron. Technol. Unified Conf. (S3S)*, Oct. 2015, pp. 1–3.

[2] M. Shrivastava *et al.*, "Benchmarking the device performance at sub 22 nm node technologies using an SoC framework," in *Proc. IEEE Int. Electron Device Meeting*, Dec. 2009, pp. 1–4.

[3] A. Sharma, A. A. Goud, and K. Roy, "Sub-10 nm FinFETs and tunnel-FETs: From devices to systems," in *Proc. Design, Autom. Test Conf. Exhib. (DATE)*, 2015, pp. 1443–1448.

[4] *ITRS Edition Reports*. accessed on 2015. [Online]. Available: http://public.itrs.net/reports.html

[5] S.-Y. Wu *et al.*, "A 16nm FinFET CMOS technology for mobile SoC and computing applications," in *Proc. IEEE Int. Electron Device Meeting*, Dec. 2013, pp. 9.1.1–9.1.4.

[6] M. Shrivastava *et al.*, "Toward system on chip (SoC) development using FinFET technology: Challenges, solutions, process co-development & optimization guidelines," *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1597–1607, Jun. 2011.

[7] A. Wei *et al.*, "Challenges of analog and I/O scaling in 10nm SoC technology and beyond," in *Proc. IEEE Int. Electron Device Meeting*, Dec. 2014, pp. 18.3.1–18.3.4.

[8] A. Marshall, "Designing with FinFET technology," in *Proc. ISOCC*, Nov. 2014, pp. 30–31.

[9] Q. Huang *et al.*, "First foundry platform of complementary tunnel-FETs in CMOS baseline technology for ultralow-power IoT applications: Manufacturability, variability and technology roadmap," in *Proc. IEEE Int. Electron Device Meeting*, Dec. 2015, pp. 22.2.1–22.2.4.

[10] M. Shrivastava, M. S. Baghini, H. Gossner, and V. Ramgopal Rao, "Part I: Mixed-signal performance of various high-voltage drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[11] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part II: A novel scheme to optimize the mixed-signal performance and hot-carrier reliability of drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 458–465, Jan. 2010.

[12] T. Miyashita *et al.*, "High voltage I/O FinFET device optimization for 16nm system-on-a-chip (SoC) technology," in *Proc. Symp. VLSI Technol. (VLSI Technology)*, Jun. 2015, pp. T152–T153.

[13] M. Shrivastava, H. Gossner, and V. R. Rao, "A novel drain extended FinFET device for high voltage high speed applications," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1432–1434, Oct. 2012.

[14] M. Shrivastava, H. Gossner, and C. Russ, "A drain-extended MOS device with spreading filament under ESD stress," *IEEE Electron Device Lett.*, vol. 33, no. 9, pp. 1294–1296, Sep. 2012.

[15] M. Shrivastava *et al.*, "ESD robust DeMOS devices in advanced CMOS technologies," in *Proc. EOSESD Symp.*, Sep. 2011, pp. 1–10.

[16] K. Hemanjaneyulu and M. Shrivastava, "Fin enabled area scaled tunnel FET," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3184–3191, Oct. 2015.

[17] M. N. Darwish, "Study of the quasi-saturation effect in VDMOS transistors," *IEEE Trans. Electron Devices*, vol. 33, no. 11, pp. 1710–1716, Nov. 1986.

[18] A. Rajoriya, M. Shrivastava, H. Gossner, T. Schulz, and V. R. Rao, "Sub 0.5V operation of performance driven mobile systems based on area scaled tunnel FET devices," *IEEE Trans. Electron Devices*, vol. 60, no. 8, pp. 2626–2633, Aug. 2013.

[19] R. Asra, M. Shrivastava, K. V. R. M. Murali, R. K. Pandey, H. Gossner, and V. R. Rao, "A tunnel FET for V_{DD} scaling below 0.6 V with a CMOS-comparable performance," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 1855–1863, Jul. 2011.

[20] Y. Morita *et al.*, "Introduction of SiGe/Si heterojunction into novel multilayer tunnel FinFET," *Jpn. J. Appl. Phys.*, vol. 55, no. 4S, p. 04EB06, 2016.

[21] K. H. Kao *et al.*, "Tensile strained Ge tunnel field-effect transistors: K.p material modeling and numerical device simulation," *J. Appl. Phys.*, vol. 115, no. 4, p. 044505, 2014.

Mayank Shrivastava (S'09–M'10–SM'16) received the Ph.D. degree from IIT Bombay, Mumbai, India. Since 2013, he has been with the Indian Institute of Science, Bengaluru, India, where he has established Advanced Nanoelectronic Device Research Group and is currently a Faculty Member with the Department of Electronic Systems Engineering. He has authored or co-authored over 65 international publications and holds 30 patents.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:26:22 UTC from IEEE Xplore. Restrictions apply.