Performance and Reliability Codesign for Superjunction Drain Extended MOS Devices

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***Abstract*— Conventionally, integrated drain-extended MOS (DeMOS) like high-voltage devices are designed while keeping only performance targets for a given application in mind. In this paper, for the first time, performance and reliability codesign approach using 3-D TCAD has been presented for various superjunction (SJ) type DeMOS devices. In this context, how to effectively utilize the SJ concept in a DeMOS device for System on Chip applications, which often has stringent switching and RF performance targets, is explored in detail in this paper. Moreover, design and reliability tradeoffs for switching and RF applications are discussed, while considering two unique sets, one with fixed breakdown voltage and other with fixed ON-resistance. Finally, hot carrier generation, safe operating area concerns, and electrostatic discharge physics are explored and compared using 3-D TCAD simulations.**

***Index Terms*— Drain extended MOS (DeMOS), electrostatic discharge (ESD), hot carrier injection (HCI), safe operating area (SOA), superjunction (SJ).**

I. Introduction

SYSTEM ON CHIP (SoC) using advanced CMOS technology nodes is high in demand for hand-held applications like tablets and cellphones [1]. An SoC concept intrinsically demands integration of low-voltage functionalities like digital core, high-voltage functionalities like input/output interfaces, RF functionalities like power amplifiers and power electronics like dc–dc converters for on-chip power management. Such an integration seriously cuts down the manufacturing cost and reduces the time to market. However, except digital cores, other functionalities require high-voltage/high-power switching or RF devices [2], [3], offered over the same technology platform for cost-efficient integration within the same chip. In CMOS technologies, conventional nonshallow trench isolation (STI) drain extended MOS (DeMOS) devices, as depicted in Fig. 1(a), are commonly used for high-voltage operation. Designing such high-voltage devices in ultrascaled technologies, with tight reliability targets [4]–[6], often limits the device design flexibility. As a result, a number of drift region architectures have been explored in last decade to improve breakdown voltage *versus* ON-resistance tradeoff. Superjunction (SJ) concept, as depicted in Fig. 1(b)–(d), is one promising approach among those, which was first proposed for vertical power MOSFET designs [7], [8] and recently adopted for lateral SOI [9]–[12] as well as bulk DeMOS devices [13], [14]. The SJ region or additional P-type implant in the drain extended region allows further depletion in the drift region, which suppresses the peak electric field and improves the breakdown voltage [2], [3], [13]–[16].

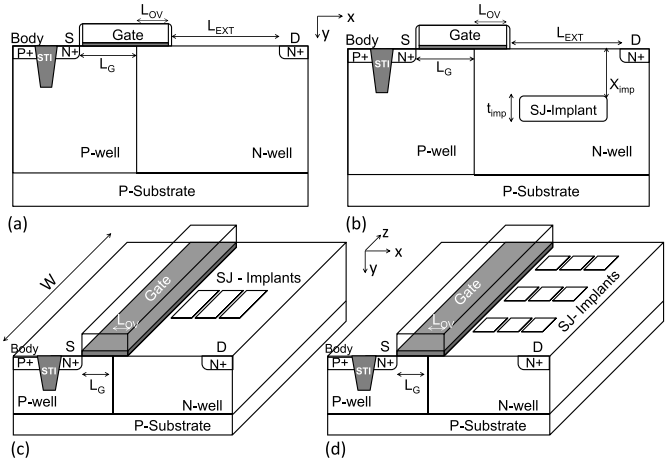

Fig. 1. Schematic of (a) conventional non-STI DeMOS structure, (b) single SJ DeMOS with $X_{imp} > 0$, (c) multiple SJ DeMOS-I, and (d) multiple SJ DeMOS-II.

These high-voltage devices are often designed while keeping only performance targets in mind. As a result, discussion on performance and reliability codesign for these devices, which often have stringent performance and reliability requirements, is missing in the literature. This paper, while using 3-D TCAD, is the first attempt in this direction. Similarly, a detailed design and reliability study for various SJ type DeMOS devices are missing in the literature. This paper for the first time presents design guidelines for SJ-DeMOS devices while exploring safe operating area (SOA) and electrostatic discharge (ESD) failure physics using 3-D TCAD.

II. ON-Resistance Versus Breakdown Voltage Tradeoff

This section studies the ON-resistance (R_{ON}) versus breakdown voltage (V_{BD}) tradeoff of various SJ-DeMOS devices in detail and compares it with conventional non-STI DeMOS

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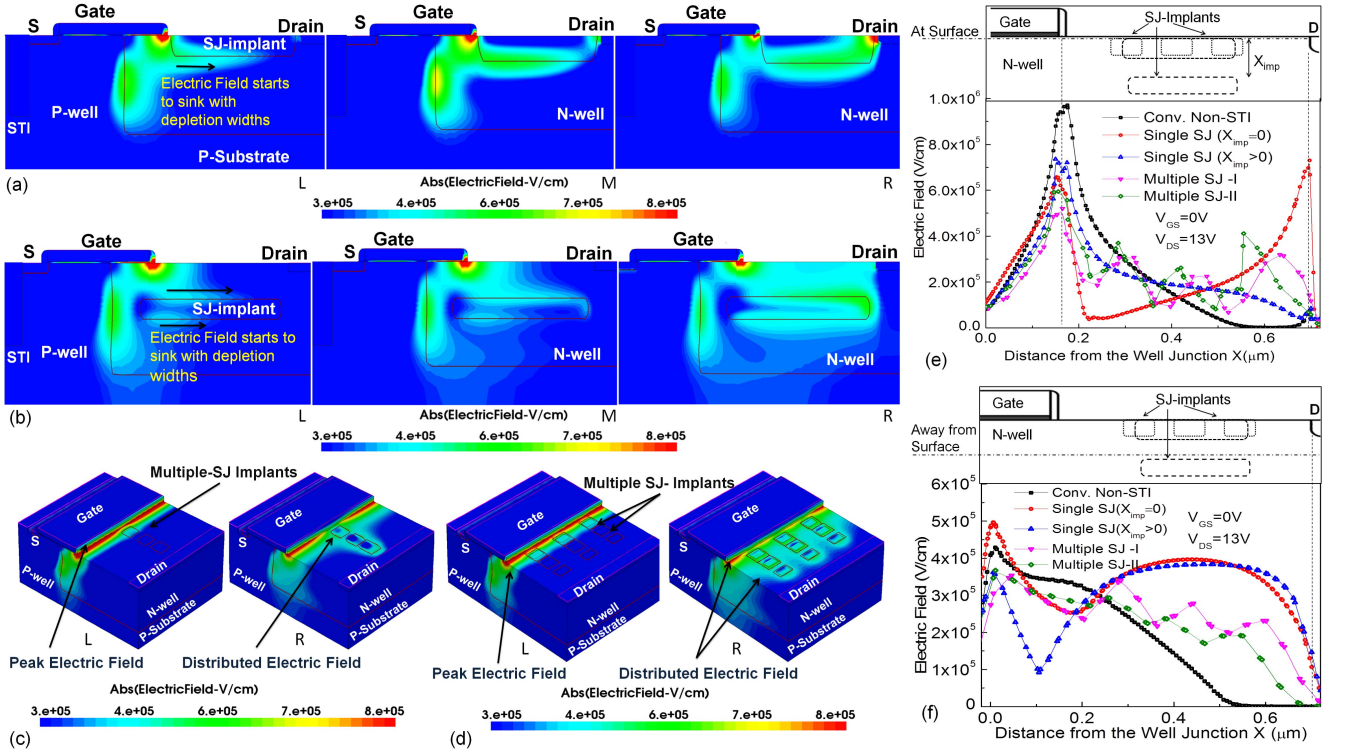

Fig. 2. (a)–(d) Electric field contours across various SJ devices when the SJ doping was increased from left (L) to right (R). (a) Single SJ-DeMOS with $X_{imp} = 0$. (b) Single SJ-DeMOS with $X_{imp} > 0$. (c) and (d) Multiple SJ-DeMOS. Electric field profile along the transport direction of conventional DeMOS compared with the same across various SJ devices (e) close to surface and (f) 120 nm away from the surface.

device. TCAD and calibration setup used in this paper are discussed in detail in earlier works [4], [17]. The key to minimize ON-resistance while maximizing breakdown voltage is to distribute space charge as much as possible in order to suppress electric field at a given drain voltage without significantly: 1) affecting cross-sectional area available for carrier transport in the drift region and 2) lowering background doping concentration. Fig. 2 shows electric-field distribution across various SJ devices when the SJ doping was increased (in figure from left to right) and compares it with the conventional non-STI DeMOS device. It shows that various SJ-DeMOS devices with lower SJ doping have an electric field profile similar to that of conventional DeMOS device; however, when SJ doping was increased, the electric field gets shared between well junction as well as SJ region to n-well junction. Moreover, the field around the SJ region increases when the SJ doping concentration was increased. Independent of SJ concept, the peak field across the SJ device was found to be lower compared with conventional device; however, if the SJ doping is increased beyond a critical point, i.e., the field around SJ region continue to increase, the electric field gets crowded near the drain contact, which leads to a premature avalanche breakdown. Unlike single SJ with $X_{imp} = 0$, device with $X_{imp} > 0$ shows peak electric field above the SJ region. This causes device with $X_{imp} = 0$ to offer maximum reduction in peak electric field at the surface, close to gate edge; however, device with $X_{imp} > 0$ offers maximum reduction in peak electric field away from the surface, close to well junction. Moreover, the electric field away from the surface was found to be distributed in the drift region, however, close

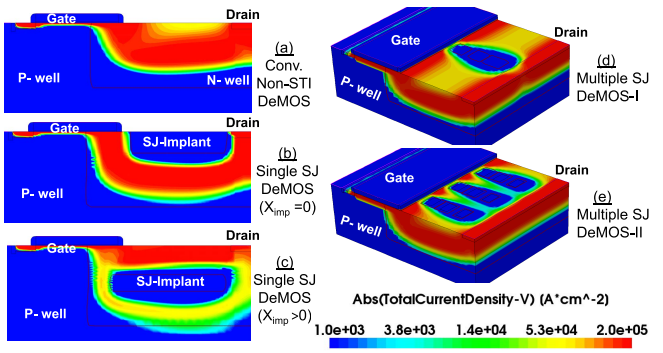

Fig. 3. Conduction current density under ON state across (a) conventional DeMOS, (b) single SJ-DeMOS with $X_{imp} = 0$, (c) single SJ-DeMOS with $X_{imp} > 0$, (d) multiple SJ-DeMOS-I, and (e) multiple SJ-DeMOS-II.

to surface, it was always localized close to the gate to n-well-overlap region edge. Among multiple SJ-I and SJ-II, no change in the peak electric field was found, which in both the cases was higher than single-SJ devices.

Fig. 3 shows conduction current density in ON state across various devices under study. SJ-DeMOS device with $X_{imp} > 0$ tend to offer current conduction through the drift region surface like the conventional devices. However, SJ-DeMOS device with $X_{imp} = 0$ and multiple SJ-DeMOS device offers current conduction via a longer drift path attributed to the presence of SJ in the surface region. This leads to a tradeoff in ON-resistance when SJ is formed close to the drift region surface. Besides distributed electric field profile, the added advantage of multiple SJ-DeMOS is that

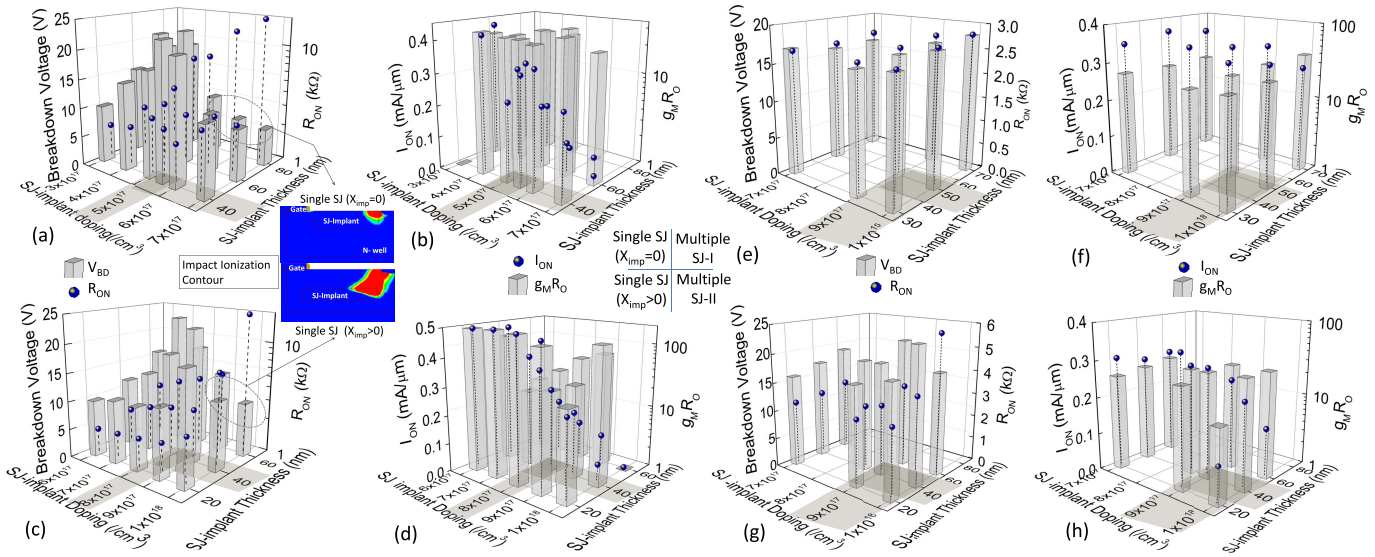

Fig. 4. R_{ON}, V_{BD}, I_{ON}, and $g_m.R_O$ versus SJ doping and thickness for different SJ-DeMOS devices under study. ON-state parameters are extracted at $V_{GS} = 1.8V$ and $V_{DS} = 6V$, whereas breakdown voltage was extracted under OFF-state ($V_{GS} = 0V$). (a) and (b) Single SJ DeMOS with $X_{imp} = 0$, (c) and (d) Single SJ DeMOS with $X_{imp} > 0$. (e) and (f) Multiple SJ DeMOS-I. (g) and (h) Multiple SJ DeMOS-II. The shaded regions depict optimum tradeoff.

it offers surface conduction between SJ region. This helps in terms of mitigating R_{ON} *versus* V_{BD} tradeoff when compared with conventional device.

The additional design feature discussed previously is expected to extend the drift region design window, which may improve the device figure of merit like R_{ON} *versus* V_{BD}. This has been depicted in Fig. 4 and discussed here. Fig. 4(a) and (c) show R_{ON} *versus* V_{BD} tradeoff as a function of SJ implant doping and depth (vertical thickness) for single SJ devices. For lower and higher doping, the breakdown voltage was found to be on the lower side. In the case of lower doping, the SJ region is not effective in distributing space charge and sharing the depletion region, however, at higher doping concentrations, high field around the SJ layer leads to an early avalanche breakdown around drain region, as depicted in the inset. Given that lower doping does not deplete the drift region, ON resistance is maintained at a lower value, however, as the SJ doping increases, it reduces the effective conduction area by depleting the drift region, which increases ON resistance significantly. Similar trends were found for SJ-implant depth/thickness (t_{imp}), as the ON resistance tradeoff is due to effectiveness of SJ region and overdesign by depleting drift region. Interestingly, on one hand, ON resistance increases with SJ-implant depth/thickness, whereas breakdown voltage for a given SJ doping does not change relatively by increasing SJ-implant depth/thickness (t_{imp}). This allows an optimum doping and thickness combination, which maximizes V_{BD}, minimizes R_{ON}, as depicted by the shaded region. Fig. 4(b) and (d) shows that ON current (I_{ON}) falls linearly with SJ region doping, which is attributed to reduced drift area due to increased depletion width at higher p-type doping. On the other hand, intrinsic gain ($g_m R_O$) on the devices does not change significantly. Overall, ON current and intrinsic gain of device with $X_{imp} > 0$ was found to be higher than $X_{imp} = 0$, whereas R_{ON} and V_{BD} were found to be in the same range. Fig. 4(e)–(h) shows R_{ON} *versus* V_{BD} and I_{ON} *versus* $g_m R_O$ tradeoff as a function of SJ implant doping and depth for multiple SJ devices. Unlike single SJ devices, multiple SJ-I offers relatively least variation in all the figure of merit parameters, which signifies the robustness of multiple SJ-I design. On the other hand, when the SJ implant island density was increased (multiple SJ-II design), a tradeoff between R_{ON} *versus* V_{BD} and I_{ON} *versus* $g_m R_O$ was found. This depicts an optimum design with maximum V_{BD}, I_{ON}, and $g_m R_O$ and least R_{ON} between multiple SJ-I and SJ-II. Overall, multiple SJ devices offers least ON resistance compared with single SJ DeMOS, which is attributed to its 3-D nature, i.e., combination of conventional DeMOS and single SJ DeMOS. The shaded regions in Fig. 4 show the optimum parameters of SJ-implants for all the devices, which were then considered for rest of the investigation, while categorizing devices into the following two sets. (a) Set-1: all the devices with the same R_{ON}. (b) Set-2: all the devices with the same V_{BD} (Fig. 5).

III. Analog/RF Performance

Besides the SOA, ESD [18] and OFF-state hot carrier reliability [19] issues, advanced DeMOS devices seriously suffer due to early quasi-saturation [18], [20], [21], which hinders transistor to reach its intrinsic limits. Hence, for efficient circuit operation, especially for analog/RF and mixed signal applications, quasi-saturation effect is also worth investigating besides minimizing R_{ON} versus V_{BD} tradeoff. Quasi saturation, which is an electrical consequence of early space charge modulation in the drift region, occurs when injected majority carrier density is higher than background doping concentration in the n-well drift region. This leads to significant mobility degradation and loss of gate control over channel current modulation. It becomes relevant for SJ devices due to reduced drift area available for carriers to flow, which increases the current density inside the n-well region of SJ devices at a given current. For Set-1 devices, it can be noted from Fig. 6 that single SJ-DeMOS devices in Set-1 have 50% higher

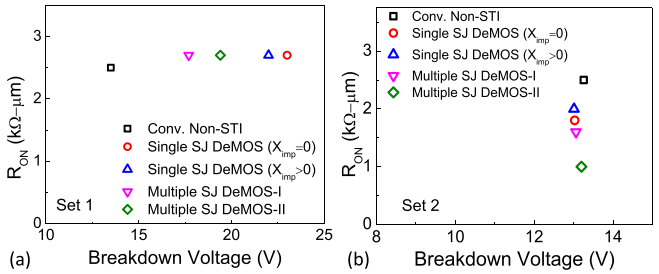

Fig. 5. V_{BD} versus R_{ON} tradeoff of various DeMOS devices in the following two sets. (a) Set-1 consists of devices with fixed ON-resistance. (b) Set-2 has devices with fixed breakdown voltage. Note: all the devices compared here have the same footprint.

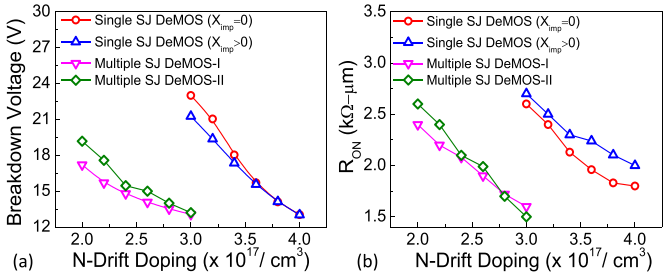

Fig. 6. V_{BD} versus R_{ON} tradeoff as a function of n-well doping for various DeMOS devices under study. ON-state parameters are extracted at V_{GS} = 1.8V and V_{DS} = 6V, whereas breakdown voltage was extracted under OFF-state (V_{GS} = 0V).

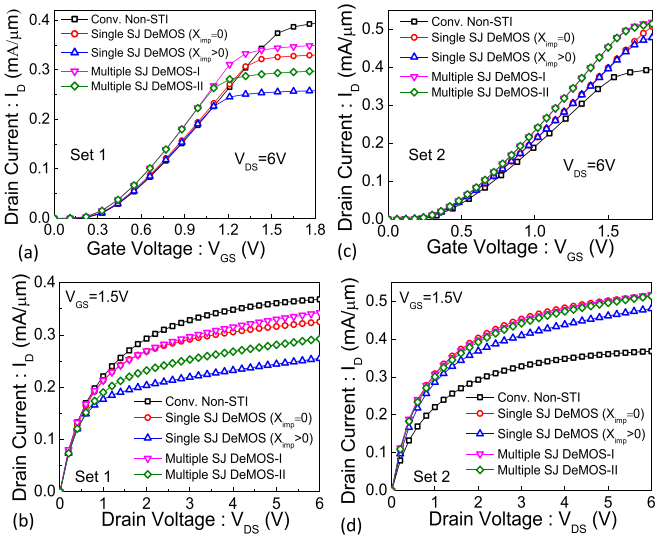

Fig. 7. (a) and (c) Simulated drain current (I_D) versus gate voltage (V_G) characteristics and (b) and (d) drain current versus drain voltage (V_{DS}) characteristics of (a) and (b) Set-1 and (c) and (d) Set-2 devices. I_D–V_G characteristics was extracted at V_{DS} = 6V, whereas I_D–V_D characteristics was extracted at V_G = 1.8V.

drift region doping compared with other designs, whereas it has 33% and 200% higher doping compared with multiple SJ-DeMOS devices and conventional device, respectively, in Set-2.

Fig. 7(a) and (b) shows the transfer and output characteristics, respectively, of Set-1 devices. Similarly, transfer and output characteristics of Set-2 devices are depicted in Fig. 7(c) and (d), respectively. For fixed ON-resistance, single SJ with $X_{imp} = 0$ offers significant performance improvement over single SJ with $X_{imp} > 0$. The SJ with $X_{imp} = 0$

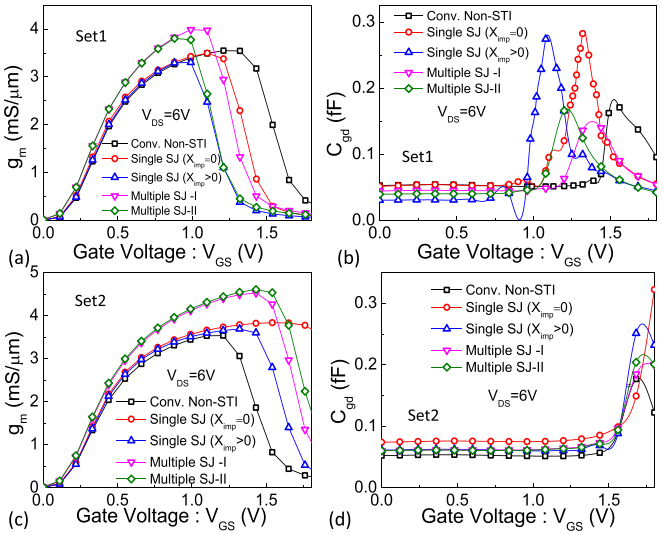

Fig. 8. (a) and (c) Transconductance (g_m) versus gate voltage (V_G) characteristics and (b) and (d) miller capacitance (C_{GD}) versus gate voltage (V_G) characteristics of (a) and (b) Set-1 and (c) and (d) Set-2 devices. Both the characteristics were extracted at V_{DS} = 6V.

offers 200% higher breakdown voltage at the cost of 15% reduction on ON-current, when compared with conventional device. It is worth highlighting that most of the devices suffer from quasi-saturation. Given that single SJ with $X_{imp} = 0$ offers maximum improvement in breakdown voltage for a given ON-resistance, the cost it has to pay in terms of onset of quasi-saturation at 10% lower gate voltage is not significant. Other devices do not seem to offer a better tradeoff in terms of breakdown voltage and ON-current for fixed ON-resistance, which is due to early quasi-saturation noticed in multiple SJ DeMOS-II and single SJ device with $X_{imp} > 0$. For fixed breakdown voltage case, SJ designs clearly outperform the conventional design. Except Single SJ with $X_{imp} > 0$, other designs offer 50% higher ON-current when compared with conventional designs, due to delayed quasi-saturation. Multiple SJ devices have a marginal quasi-saturation at higher gate voltage, which in the case of single SJ device is completely missing. This is attributed to an increased n-well doping window for SJ devices.

Transconductance (g_m) and miller capacitance (C_{GD}) are the key parameters to access analog and RF capability of DeMOS devices. Fig. 8(a) shows that among Set-1 devices multiple SJ devices offer maximum g_m, however, attributed to an early quasi saturation, g_m falls dramatically at 33% lower gate voltage compared with conventional device. This seriously lowers the maximum gate swing allowed, which limits its uses for large signal power RF applications. Furthermore, single SJ devices does not offer g_m improvement; whereas causes a loss of 15% in the maximum allowed gate swing due to early quasi-saturation. Fig. 8(b) reveals that single SJ devices of Set-1 significantly adds to nonlinearity in feedback/miller capacitance, at higher gate voltage, compared with multiple SJ and conventional devices. This is attributed to the nonlinearity in the field distribution at gate edge, at higher currents, in single SJ devices. Moreover, an interesting trend can be observed, device having lowered onset of quasi-

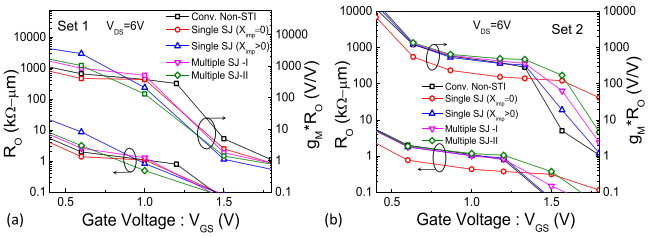

Fig. 9. Output resistance (R_O) and intrinsic gain (g_mR_O) of devices in (a) Set-1 and (b) Set-2.

saturation has least miller capacitance. Fig. 8(c) shows that among Set-2 multiple SJ devices offer maximum g_m, however, a lower gate voltage swing due to relatively an early quasi-saturation compared with single SJ (X_{imp}=0) device. Single SJ ($X_{imp} = 0$) device has the same g_m as compared with the conventional device and single SJ device with $X_{imp} > 0$, however, it offers maximum gate swing, which in the case of conventional device and single SJ device with $X_{imp} > 0$ is the least. Therefore, single SJ ($X_{imp} = 0$) device allows maximum input voltage swing, which is a desirable parameter for power RF applications. Finally, Fig. 8(d) depicts that SJ device $X_{imp} = 0$ has highest miller capacitance and nonlinearity at higher gate voltage compared with other devices.

Fig. 9 shows output resistance and intrinsic transistor gain for both Set-1 and Set-2 devices. Fig. 9(a) depicts that for fixed ON-resistance single SJ device with $X_{imp} > 0$, which has close to the maximum junction breakdown voltage in this set, offers maximum output conductance and intrinsic gain, which, however, falls below the other devices as soon as quasi-saturation is triggered. On the other hand, single SJ device with $X_{imp} = 0$ with maximum breakdown voltage and conventional device with minimum breakdown voltage offer the least output conductance and intrinsic gain. Multiple SJ devices, which falls between single SJ and conventional devices, in terms of breakdown voltage, offer a moderate intrinsic gain and output conductance. These trends hint role of drift region field engineering while designing device for maximizing transistor gain and output conductance, which, however, require further investigations. Fig. 9(b) depicts that for fixed breakdown voltage, single SJ device with $X_{imp} = 0$ offers the least output conductance and intrinsic gain; however, offers maximum input swing. Other devices offers very similar R_O and g_mR_O performance; however, shows a roll-off as soon as quasi-saturation is triggered. Moreover, the extent of roll-off is also found to be the same as strength of quasi-saturation.

Fig. 10 shows cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) of both Set-1 and Set-2 devices. In principle, Fig. 10 shows an overall manifestation of trends on Figs. 7–9. Fig. 10(a) and (b) depicts that conventional device, which suffers the least from quasi-saturation effect, offers the maximum f_t and f_{max}, even when all the devices in this set have the same ON-resistance. This is attributed to longer drift length of SJ devices and early quasi-saturation effect. On the other hand, Fig. 10(c) and (d) shows that SJ devices outperform the conventional device when the design was for fixed breakdown voltage. Interestingly single SJ device with $X_{imp} > 0$ offers higher f_{max}, whereas device with $X_{imp} = 0$ has

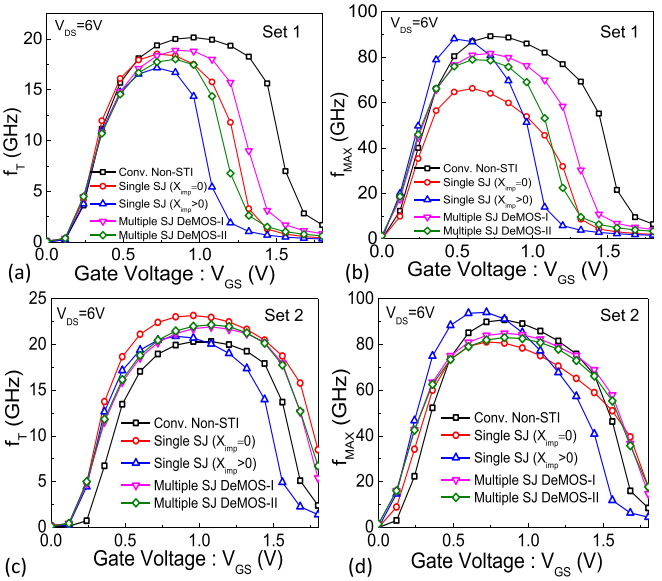

Fig. 10. (a) and (c) Transistor cutoff frequency (f_t) versus gate voltage (V_G) characteristics and (b) and (d) maximum oscillation frequency (f_{max}) versus gate voltage (V_G) characteristics of (a) and (b) Set-1 and (c) and (d) Set-2 devices. Both the characteristics were extracted at $V_{DS} = 6V$.

maximum cutoff frequency. This is attributed to lower miller capacitance and higher intrinsic gain of single SJ device with $X_{imp} > 0$ compared with device with $X_{imp} = 0$.

IV. HCI/ESD Reliability and SOA

Besides quasi saturation, reliability issues like OFF-state hot carrier injection (HCI) [19], SOA [22], and ESD [18] are extremely critical issues and strongly depend on device design. In this section, we will study and compare HCI, SOA, and ESD reliability behavior of various SJ DeMOS devices using 3-D TCAD.

A. Hot Carrier Reliability Versus Superjunction Design

HCI reliability of various DeMOS devices is studied using spherical harmonic expansion of Boltzmann transport equation, which allows extraction of hot carrier profile and hot carrier-induced interface/bulk trap density and is well-established method for hot carrier studies and relative comparisons [23]. However, it is worth highlighting that it is an indirect approach to study hot carrier behavior and is not used here for life time predictions. For ON-state HCI investigations, all devices were biased at gate voltage, which offers maximum substrate current and drain voltage close to avalanche breakdown [24], [25]. For OFF state, gate and source were grounded, whereas drain was biased close to junction breakdown voltage. Fig. 11 compares hot electron and hot hole profiles of various SJ devices from Set-1 under ON and OFF states. It clearly depicts that the single SJ DeMOS devices, both with $X_{imp} = 0$ and $X_{imp} > 0$, have considerably lower electron and hole energy, both in the ON and OFF states, when compared with conventional DeMOS device. In the case of multiple SJ-I and multiple SJ-II, carrier energy was found to be significantly lower along and around the SJ region (C_2), whereas the same between two SJ islands (along C_1) was found to be close to conventional device. Similar trends

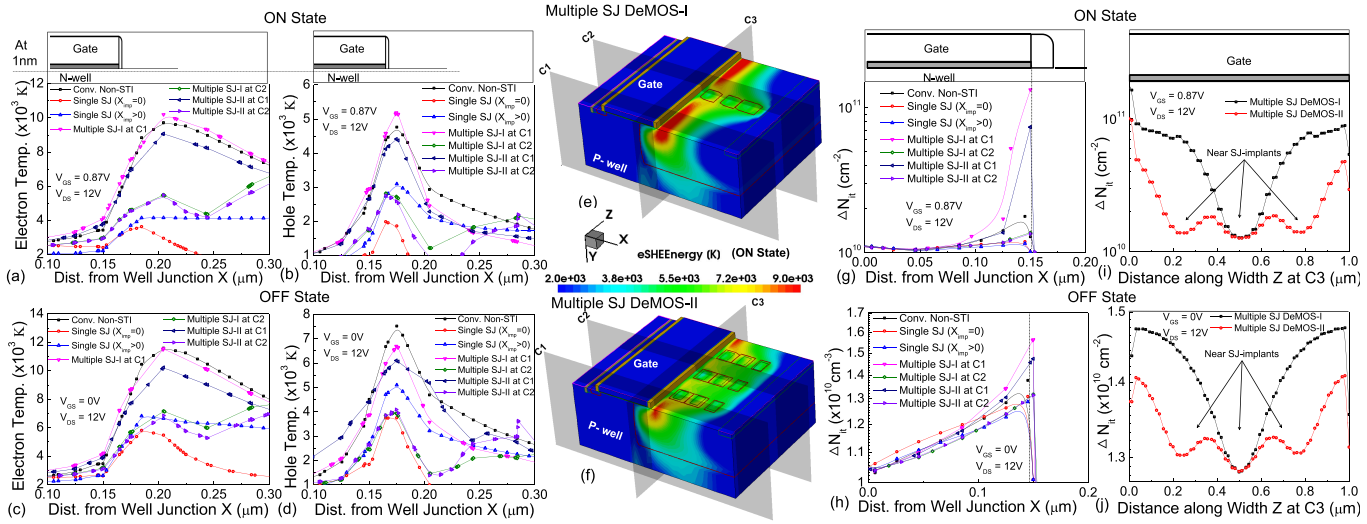

Fig. 11. Hot carrier energy profile of various Set-1 devices, as a function of lateral distance, extracted at 1 nm away from SiO_2/Si interface. (a) Hot electron and (b) hot hole profiles under ON state. (c) Hot electron and (d) hot hole profiles under OFF state. 3-D countour depicting hot electron energy distribution across (e) multiple SJ-I and (f) multiple SJ-II devices. Interface trap concentration along the channel and drift length under (g) ON and (h) OFF state. Interface trap concentration along the device width under (i) ON and (j) OFF state.

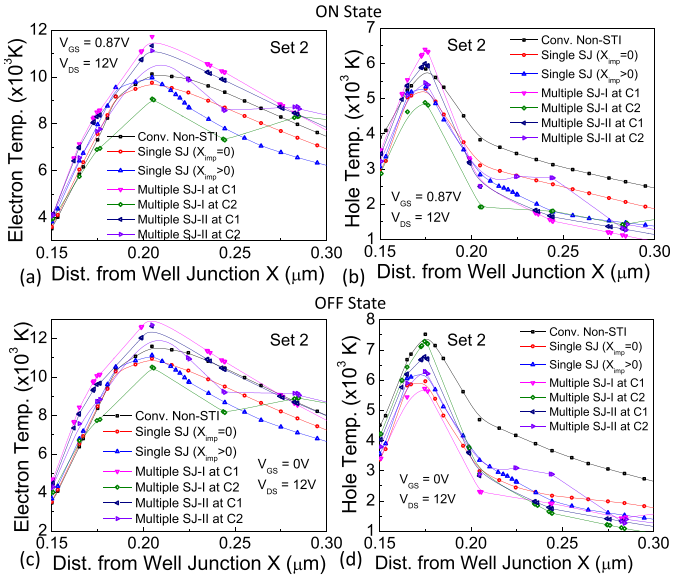

Fig. 12. Hot carrier energy profile of various Set-2 devices, as a function of lateral distance, extracted at 1 nm away from SiO_2/Si interface. (a) Hot electron and (b) hot hole profiles under ON state. (c) Hot electron and (d) hot hole profiles under OFF state.

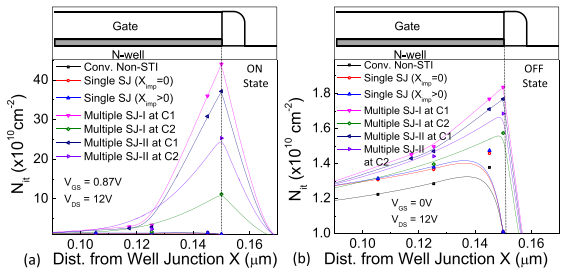

Fig. 13. Interface trap concentration along the channel and drift length of various devices in Set-2 under (a) ON and (b) OFF state.

can be found from generated interface traps as depicted in Fig. 11(g) and (h). Among all SJ devices, single SJ devices were found to be the most reliable. Among multiple SJ-I

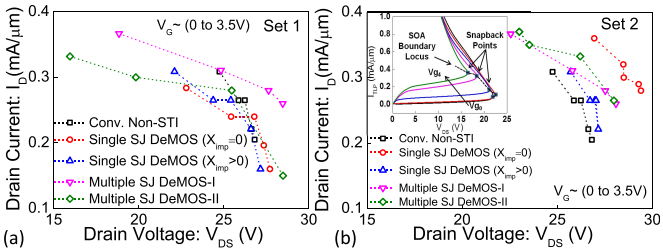

Fig. 14. Simulated SOA boundary of conventional as well as various SJ DeMOS devices in (a) Set-1 and (b) Set-2, extracted using 3-D electrothermal TCAD-based pulse *I–V* simulations with 100-ns pulsewidth.

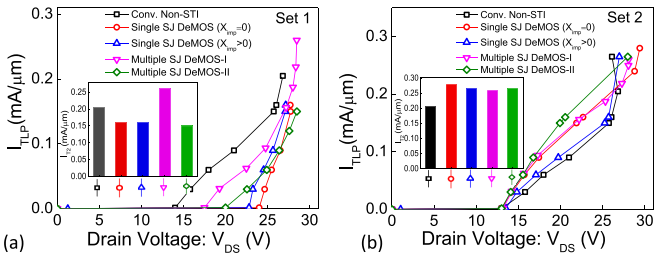

Fig. 15. Simulated TLP characteristics of conventional and SJ DeMOS devices of (a) Set-1 and (b) Set-2 under study. Inset: failure current (It2) of various devices.

and SJ-II, multiple SJ-II having higher number of SJ implant islands shows lower hot carrier energy and generated interface trap density compared with the multiple SJ-I. This is further clarified in Fig. 11(i) and (j), which depicts interface trap concentration along the width of multiple SJ DeMOS devices. Clearly, the interface trap generation, both in ON and OFF state, is minimum in the region in and around SJ islands. However, the same in regions away from SJ islands approaches interface trap concentration equivalent to conventional device. This is attributed to the presence of depletion under the gate edge around SJ islands, which, however, vanishes while moving away from these islands. The presence of depletion mitigates hot carrier generation. Overall, trends from multiple SJ device

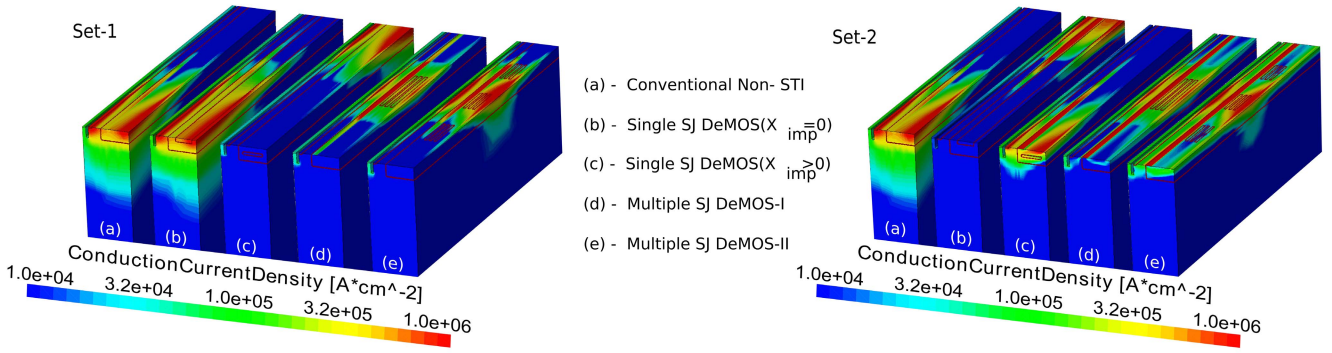

Fig. 16. Conduction current density across various devices at current close to ESD failure point (It2), extracted using 3-D TCAD simulations, for devices in Set-1 and Set-2.

indicate a need for an optimization strategy for the placement of SJ islands with design parameters like island doping, depth, and pitch to suppress hot carrier generation without sacrificing performance. Broadly similar trends were found for devices in Set-2 as depicted in Figs. 12 and 13. Therefore, from the HCI point of view a slower rate of degradation, i.e., N_{it} being lower would be a preferred choice for device's long term reliability.

B. Safe Operating Area

Fig. 14 shows simulated SOA boundary of conventional and SJ DeMOS devices. The SOA boundary represents the safe I–V margin of device under circuit operations [inset in Fig. 14(b)]. In principle, there are three different ways in which SOA boundary is extracted: 1) thermal SOA: by stressing the device using steady state (few 10 s of millisecond long) pulses, which results in purely thermal failure; 2) electrical SOA: by stressing the device using sub-10 ns long pulses, which mitigates self-heating and causes devices failure purely due to electrical instabilities; and 3) electrothermal SOA: by stressing the device using 100-500-ns-long pulses, which accounts for both thermal and electrical aspects and causes device to fail due to electrothermal instabilities [18]. From real-world application point of view, in this paper, electrothermal SOA is studied and compared. Fig. 14 shows that among Set-1 devices, with fixed ON resistance, except multiple SJ-I, all other devices offer similar SOA boundary. Multiple SJ-I device offers relatively better SOA, however, a marginal improvement over others. This is attributed to fixed ON resistance of the devices. It is worth highlighting that SOA boundary is defined by I–V required for filamentary failure in DeMOS devices, which is due to charge modulation and is directly related to drift region doping profile [4]. Fixed ON resistance designs keep the current density more or less unchanged in the drift region, which leads to unchanged SOA boundary. On the other hand, Set-2 devices having fixed breakdown voltage show consistent improvement in SOA boundary while moving from conventional design to multiple SJ and then single SJ implant design. In this case, the conventional device with highest ON resistance for a given breakdown voltage offers an inferior SOA boundary compared with single SJ device with a least ON resistance. These trends also show that SJ implant-based device not only improves the R_{ON} *versus* V_{BD} tradeoff, but also results in an extended SOA boundary.

C. ESD Reliability

ESD reliability of DeMOS devices has been studied extensively in the past [18], [26]. DeMOS devices under ESD condition fail due to electrical or electrothermal instability triggered after space charge modulation. This is often related to drift region profile, conduction current density, and background doping. As soon as mobile electrons exceed the background doping, space charge modulation takes place, which forms destructive filament leading to catastrophic damage. Fig. 15 shows tranmission line pulse (TLP) I–V characteristics of Set-1 and Set-2 devices. Among Set-1 devices, single SJ and multiple SJ-II devices, due to restricted flow of current, lead to early failure when compared with conventional device. However, multiple SJ-I device, due to relaxed SJ implant placement, takes advantage of both the conventional design as well as SJ region. It gives maximum failure current (failure current per unit width) while offering higher breakdown voltage compared with the conventional design. On the other hand, among Set-2 devices, all SJ designs offer 10%–20% higher failure current compared with conventional design. This is attributed to higher drift region doping allowed in SJ designs for a given breakdown voltage. Higher background doping shifts the onset of space charge modulation, thereby improves the failure current. Fig. 16 confirms that failure in all SJ designs, like conventional DeMOS device, is expected to be due to an early filament formation, which leads to sharp increase in lattice temperature with respect to time and catastrophic failure.

V. Conclusion

This paper gives a comprehensive insight toward design for performance as well as reliability of SJ DeMOS devices. SJ-DeMOS devices, for an optimum SJ doping and implant depth, allow electric field to share between well junction and SJ region. Independent of SJ type, the peak field across the SJ device was found to be lower compared with conventional DeMOS device. This makes SJ devices superior in terms of ON resistance versus breakdown voltage tradeoff. The SJ concept has helped improving breakdown voltage by 2 × without affecting ON-resistance or has allowed reducing ON-resistance by 2.5 × without changing the breakdown voltage. For fixed ON resistance, SJ concept delays the onset of quasi-saturation

and therefore improves analog and RF performance when compared with conventional DeMOS device. In terms of hot carrier reliability, single SJ DeMOS devices, both with $X_{\text{imp}} = 0$ and $X_{\text{imp}} > 0$, have considerably lower electron and hole energy, both in the ON and OFF state, when compared with conventional DeMOS device. Multiple SJ devices were found to be in between single SJ and conventional devices. In multiple SJ devices, hot carrier generation and interface trap generation, both in ON and OFF state, are minimum in the region in and around SJ islands. However, moving away from SJ islands, the traps generation approaches the rate similar to conventional devices. Overall, trends from multiple SJ device indicate a need for an optimization strategy for the placement of SJ islands with design parameters like island doping, depth, and pitch to suppress hot carrier generation without sacrificing performance. Finally, it was found that SJ implant-based device not only improves the R_{ON} *versus* V_{BD} tradeoff, but also results in an extended SOA boundary and 10%–20% higher ESD failure current compared with conventional design. This is attributed to mitigated space charge modulation due to higher drift region doping allowed in SJ designs for a given breakdown voltage. The ESD failure in all SJ designs, like conventional DeMOS device, was found to be due to filament formation, attributed to space charge modulation driven electrical instability.

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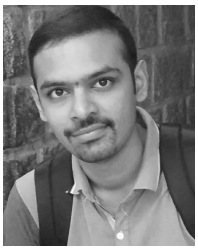

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