The Root Cause Behind a Peculiar Dual-Mode ON-State Breakdown in High Voltage LDMOS

Aakanksha Mishra, *Graduate Student Member, IEEE*, Mayank Shrivastava, *Senior Member, IEEE*, and Ankur Gupta, *Member, IEEE*

***Abstract*—This work investigates the often-observed current discontinuity much before avalanche breakdown (dual-mode ON-state breakdown) in the output characteristics of a laterally diffused metal–oxide–semiconductor (LDMOS) device. The physical origin of the dual-mode ON-state breakdown, often reasoned to be due to parasitic n-p-n, is shown to be independent of parasitic n-p-n. A laterally diffused tunnel FET (LDTFET) with a drift region profile same as LDMOS was experimented to rule out the effect of parasitic n-p-n. LDTFET device, which intrinsically cannot have parasitic n-p-n, also shows similar output characteristics with dual-mode ON-state breakdown. This proved that the parasitic bipolar turn-on is not the root cause behind the observed behavior. On the contrary, it was found to be dependent on the onset of space charge modulation (SCM) in the drift region, resulting in localized high electric field and quasi-saturation effects at low drain voltages. The effect of mobility degradation due to the high electric field in the drift region post-SCM is also presented, emphasizing that the observed behavior results from the high field mobility degradation of majority charge carriers.**

***Index Terms*—Laterally diffused MOS (LDMOS), laterally diffused tunnel FET (LDTFET), mobility degradation, ON-state breakdown, parasitic bipolar, quasi-saturation (QS), safe operating area (SOA), space charge modulation (SCM).**

I. Introduction

THE laterally double-diffused metal–oxide–semiconductor (LDMOS) devices are often employed for high voltage switching in on-chip applications like power system-on-chip (SoC) or automotive [1]–[4]. In these devices, the lightly doped N-drift region is engineered to achieve high OFF-state breakdown voltage (V_{BD-OFF}) for least ON-resistance (R_{ON}); however, such drift region engineering adversely affects the ON-state breakdown (V_{BD-ON}), and thereby limits the safe operating area (SOA) of the device. SOA is an essential factor in determining the ruggedness and reliability of the device. It is defined by a specific window within the I_D–V_{DS} characteristics, where the device operates without any functional/electrical or thermal failure [5], [6]. Several investigations have been reported on SOA limitation and the ways to improve it [7]–[21].

Hower *et al.* [11] defined the SOA boundary as the "snapback" point, after which the device suffers from filamentation. Ludikhuize [12] has attributed the decrease in V_{BD-ON} (drain voltage at snapback point) to the Kirk effect, which shifts the peak electric field from p-/n-well junction to drain contact. Khemka *et al.* [13] analyzed the electrical and thermal limitations to the static and dynamic SOA, relating it with the turn-on of the parasitic n-p-n. Consequently, suppressing parasitic n-p-n has been the most popular and effective way to improve V_{BD-ON}. The bipolar suppression techniques, such as the placement of dotted hole collection sites along the gate width in the channel region [14], the realization of a highly resistive body [15], and the source-side underlap [16], have shown improvement in the device SOA. Additionally, Hower *et al.* [17] proposed inserting a "buried body" implant under the source that suppresses the parasitic bipolar action by reducing its base–emitter shunt resistance.

The drift region engineering can potentially push the device to experience a peculiar dual-mode ON-state breakdown having unique "compression" and "expansion" regions with I_D–V_{DS} characteristics [18]. It is still not clear whether this peculiar behavior is intrinsic to the MOS operation [19] or due to the turn-on of the parasitic bipolar [20], [21]. Since device engineering is influenced by the root cause responsible for such peculiarities, physical insights must be developed to understand the mechanisms responsible for the peculiar dual-mode ON-state breakdown. We have addressed this using detailed TCAD simulations, while independently accounting for various factors affecting the nature of carrier transport. Our investigations show that the parasitic n-p-n is not the root cause behind this peculiar dual-mode ON-state breakdown. To validate our model and missing role of parasitic n-p-n, we have also investigated the dual-mode ON-state breakdown behavior in a laterally diffused tunnel FET (LDTFET) device, which intrinsically has no parasitic n-p-n, but has the same drift region profile as LDMOS.

This article is categorized in sections as follows. Section II explains the device structure and simulation setup.

Manuscript received December 28, 2021; accepted January 31, 2022. Date of publication February 23, 2022; date of current version March 28, 2022. This work was supported in part by the IMPRINT Program of Government of India, funded to the Indian Institute of Science Bengaluru and in part by the Defence Research and Development Organization (DRDO), Government of India, under Grant JATC-EMDTERA-06. The review of this article was arranged by Editor B. Zhang. *(Corresponding authors: Aakanksha Mishra; Ankur Gupta.)*

Aakanksha Mishra is with the Centre for Applied Research in Electronics, IIT Delhi, New Delhi 110016, India, and also with the Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: aakanksha.mishra@care.iitd.ac.in).

Mayank Shrivastava is with the Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: mayank@iisc.ac.in).

Ankur Gupta is with the Centre for Applied Research in Electronics, IIT Delhi, New Delhi 110016, India (e-mail: ankur.care.iitd@gmail.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3149236.

Digital Object Identifier 10.1109/TED.2022.3149236

0018-9383 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 04:46:53 UTC from IEEE Xplore. Restrictions apply.

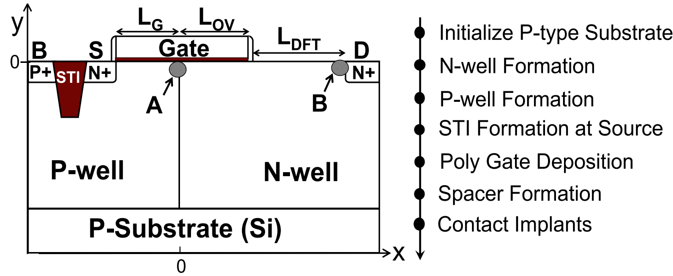

Fig. 1. 2-D cross section of a 100-V-LDMOS with CMOS compatible process flow. Point *A* indicates p-well to n-well junction (channel edge) and point *B* denotes n-well to N$^+$ drain junction (drain edge), which are critical for further investigation.

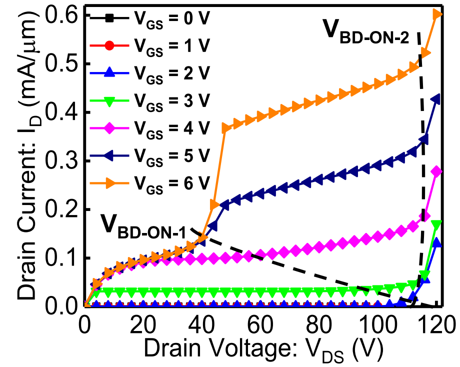

Fig. 2. Output characteristics (I_D–V_{DS}) of LDMOS indicating initial and final ON-state breakdowns, i.e., $V_{BD-ON-1}$ and $V_{BD-ON-2}$, respectively.

It also provides a detailed physical insight into the observed root cause and mechanism of dual-mode ON-state breakdown. Section III describes the role of high field mobility degradation (HFMD) in the drift region, proving that parasitic n-p-n is not the reason behind the observed device characteristics, and validates the argument using the LDTFET device with no parasitic n-p-n. Finally, a conclusion is drawn in Section IV.

II. Device Structure and Simulation Setup

Fig. 1 shows the schematic of a 100-V n-type LDMOS device realized using a CMOS compatible process flow. The device has an oxide thickness (T_{OX}) of 20 nm. The channel length (L_G) is 2 μm, the gate–drain overlap length (L_{OV}) is 1.75 μm, and the drift length (L_{DFT}) is 7 μm. The doping concentration used for p-type substrate is 1×10^{14} cm^{-3} and the p-well region is highly doped at 4×10^{17} cm^{-3} to suppress the parasitic bipolar. The n-well drift region uses a retrograde doping profile with peak doping concentration at 5×10^{15} cm^{-3} and is optimized to achieve high V_{BD-OFF} and least ON-state resistance. The device consists of separate source and body contacts to study their current contributions. A well-calibrated TCAD framework, as discussed in our earlier works [22], [23], is used to probe the physical mechanism. The device physics is captured using the TCAD models, such as UniBo2 avalanche generation for electrical breakdown, mobility models with carrier–carrier scattering, doping-dependent and high field saturation, and Shockley–Read–Hall (SRH) and auger recombination models.

III. Dual-Mode ON-State Breakdown: Observations

This section reexamines the root cause and physics of the ON-state breakdown speculated in the past research works and attempts to connect earlier findings with new observations. The output characteristics of the LDMOS device are shown in Fig. 2. The I_D–V_{DS} curve exhibits current conduction in dual-mode, where the drain current shows compression up to $V_{DS} = 40$ V, i.e., the initial breakdown point ($V_{BD-ON-1}$), and then it displays an unusual recovery for higher V_{GS} and V_{DS} values until the final SOA limit at $V_{BD-ON-2}$, as observed in [17]. It is worth highlighting that the electrical SOA of the LDMOS device for increasing V_{GS} is maintained at approximately the same V_{DS}. The fundamental physics behind the dual-mode ON-state breakdown is explored further.

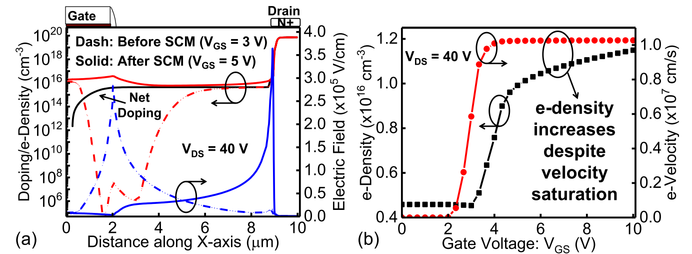

Fig. 3. (a) Net doping concentration, electron density, and electric field along the horizontal cutline near the surface for $V_{GS} = 3$ V (before SCM) and $V_{GS} = 5$ V (after SCM). (b) Electron density and electron velocity at Point *B* (shown in Fig. 1) as a function of gate voltage (V_{GS}).

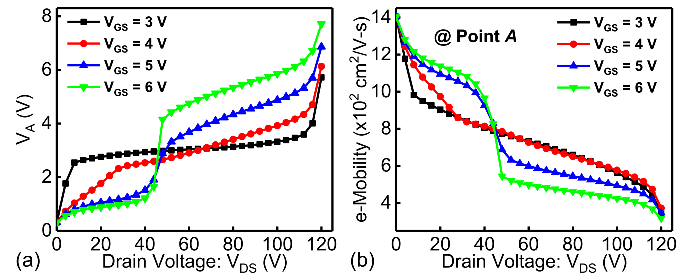

Fig. 4. (a) Change in internal voltage at Point *A* (V_A) and (b) electron mobility at Point *A* with respect to V_{DS} for different V_{GS}.

A. Drain Current Compression Mode: Up to $V_{BD-ON-1}$

Typically, the drain current for lower V_{GS} saturates due to the pinchoff of the intrinsic MOS channel at Point *A* since the peak electric field is confined to the gate to the n-well edge. However, when subjected to high current conditions, the LDMOS device experiences space charge modulation (SCM) [22]. SCM occurs when the channel injects excess majority charge carriers in the drift region, making the excess carrier concentration higher than the n-well doping. This gradually shifts the peak electric field from the gate edge to the drain edge (Point *B*), as shown in Fig. 3(a). Furthermore, Fig. 4(a) shows that for V_{DS} up to 40 V, the internal voltage at Point *A* (V_A) reduces with increasing gate bias due to increased channel conductivity. This improves the carrier mobility at Point *A* [Fig. 4(b)] and channel injects more charge carriers in the drift region. The increased carrier density with V_{GS} strengthens the electric field at Point *B* and leads to early carrier velocity saturation, as shown in Fig. 3(b).

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 04:46:53 UTC from IEEE Xplore. Restrictions apply.

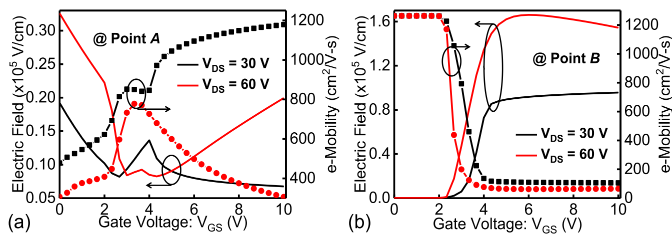

Fig. 5. Electric field and electron mobility with respect to gate voltage at (a) Point A and (b) Point B for $V_{DS} = 30$ and 60 V.

As a result, the drain current continues to increase despite carrier velocity saturation with V_{GS}. With further increase in the injected carrier density, the electric field screening occurs at Point B and the carrier mobility degrades to a saturated value, as shown in Fig. 5(b). This is acknowledged as the insensitivity of the drain current to gate voltage, often called quasi-saturation (QS) effects. Moreover, the compression in the I_D–V_{DS} curve corresponds to the onset of QS, and as soon as the drain current becomes independent of the gate bias, the peak g_m degrades severely. The higher electric field at Point B results in hotspot formation due to impact ionization near the drain. This causes the onset of the first breakdown, $V_{BD-ON-1}$. In the later section, we will see that the device operation in compression mode is entirely dominated by the drift region.

B. Drain Current Recovery Mode: Up to $V_{BD-ON-2}$

The drain, source, and body currents (I_D, I_S, and I_B, respectively) as a function of V_{DS} for $V_{GS} = 3$ V (before SCM) and $V_{GS} = 6$ V (after SCM) are shown in Fig. 6(a). The SCM-induced high electric field at the drain in the compression mode generates excessive carriers due to avalanche multiplication that marks the onset of impact ionization. Owing to the increasing impact ionization near the drain, the currents (drain, source, and body) at $V_{GS} = 6$ V show a sudden discontinuity much before avalanche breakdown, which is also referred to as the current "enhancement" effect [19]. It is worth noting that the source current saturates right after the current discontinuity, whereas the body current continues to increase due to avalanche generated increased carrier density. This has led to the speculation that the Kirk effect combined with the parasitic bipolar turn-on is responsible for this unusual drain current behavior [20], [21].

Unlike the compression mode, a different trend is observed for $V_{DS} > 40$ V. When V_{DS} is increased, the potential at Point A (V_A) shows an abrupt increase with V_{GS} due to the corresponding increase in the drift region conductivity at the onset of regenerative avalanche injection phenomenon near drain [Fig. 4(a)]. It is evident from the Fig. 6(b) that once $V_{BD-ON-1}$ has occurred, the potential barrier at the source-channel edge significantly drops (by ~200 meV), allowing more carriers to jump across the barrier. Thus, the conduction current density increases in the channel (Point A) as well as near drain (Point B), enhancing the overall conductivity of the drift region, as shown in Fig. 7(b). The increase in V_{DS} strengthens the electric field at the drain and thus impact ionization, as shown in Fig. 7(d). However, the increasing

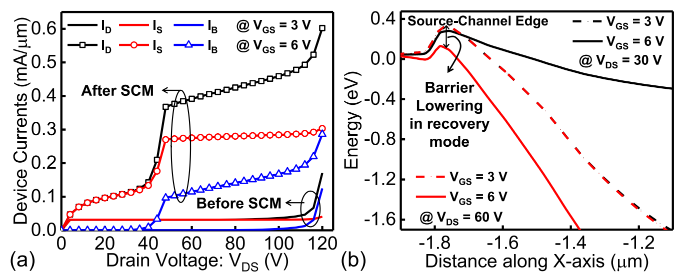

Fig. 6. (a) Drain, source, and body currents as a function of drain voltage for $V_{GS} = 3$ and 6 V. (b) Conduction band energy along the lateral cross section of LDMOS shows barrier lowering of ~200 meV between compression and recovery mode operation.

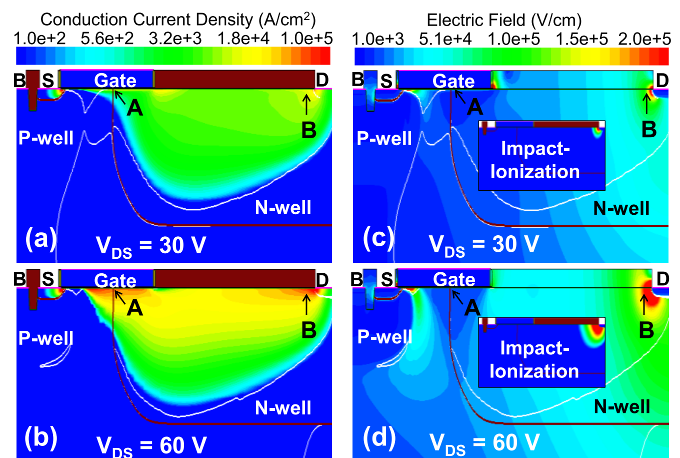

Fig. 7. (a) and (b) Conduction current density and (c) and (d) electric field (inset: impact ionization) at $V_{GS} = 6$ V for $V_{DS} = 30$ and 60 V, respectively.

current density at Point B does not allow the electric field to increase further with V_{GS}. Interestingly, relocation of the electric field profile occurs so that the mobility at Point B no more degrades due to high field saturation. Instead, it shows a recovery. Fig. 5(a) and (b) confirm the change in the field orientation where the electric field decreases at Point B, but increases at Point A under high drain and gate voltage conditions. This shows that the change in the field orientation toward the channel mitigates the HFMD in the drift region. As an effect, the drain current recovers to reach the original level, i.e., without the high field effects. With a further increase in V_{DS}, the peak electric field at the gate to the n-well edge strengthens. The resulting impact ionization creates two hot spots, i.e., at the gate to n-well edge and at Point B, leading to avalanche breakdown at $V_{BD-ON-2}$. It should be noted that the device operation in recovery mode is influenced by the onset of SCM in the drift region, resulting in localized electric field and QS effects at low drain voltages.

C. Self-Heating Versus Dual-Mode on-State Breakdown

Lattice heating is the result of electron–phonon interaction and energy exchange between the hot electrons and the crystal lattice, which increases phonon population (or lattice temperature). Lattice heating may affect the onset of QS and other reliability aspects of the device [24]. Fig. 8 shows a comparison of the output characteristics of LDMOS device with and

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 04:46:53 UTC from IEEE Xplore. Restrictions apply.

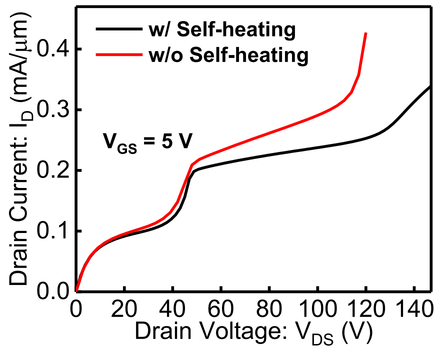

Fig. 8. I_D–V_{DS} characteristics of LDMOS device with and without self-heating effect, depicting the onset of dual-mode ON-state breakdown being independent of lattice heating.

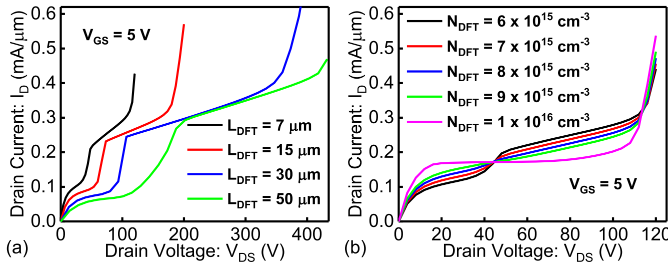

Fig. 9. I_D–V_{DS} characteristics of LDMOS device for increasing drift region (a) length (L_{DFT}) and (b) doping (N_{DFT}) at $V_{GS} = 5$ V.

without the self-heating effect. As shown, the onset and the presence of dual-mode ON-state breakdown are independent of lattice heating. This is attributed to the fact that the onset of SCM, which is causing dual-mode ON-state breakdown, is a phenomenon driven by background carrier density and not lattice temperature. However, since the lattice heating would slightly change the electrostatics (by lowering mobility, which in turn will affect current density, leading to change in charge concentration and eventually affecting electrostatics), the onset of dual-mode ON-state breakdown is observed at a slightly lower current. The second breakdown is observed to be at a higher voltage, which is due to reduced impact ionization rate in the presence of lattice heating.

D. Drift Region Design Versus Dual-Mode on-State Breakdown

The design parameters of the drift region such as its length (L_{DFT}), doping (N_{DFT}), and gate–drain overlap length (L_{OV}) were found to have direct influence on the device's dual-mode ON-state breakdown characteristics. The device with longer drift region length exhibits the same dual-mode ON-state breakdown characteristics shown in Fig. 9(a), but at higher V_{DS}. Increasing L_{DFT} pushes the injected carriers deep into the N-drift region, which lowers the injected carrier density for a given injected current and shifts the onset of SCM to higher gate voltages. Fig. 9(b) shows that increasing N_{DFT} shifts the onset of SCM to higher drain currents, which improves the device R_{ON} and drives the current toward single-mode conduction regime at an expense of OFF-state breakdown voltage. Also, increasing L_{OV} relaxes the excess carrier density for delayed SCM onset, but potentially increases the device

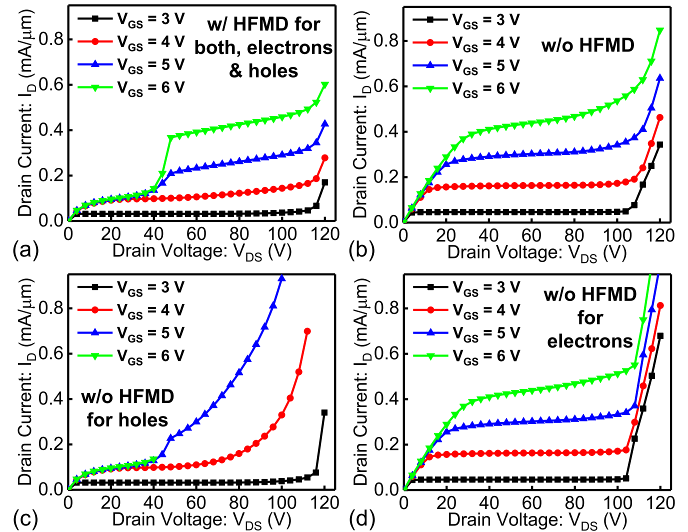

Fig. 10. I_D–V_{DS} characteristics with effect of HFMD model. (a) With HFMD for both electrons and holes, (b) without HFMD, (c) without HFMD for holes, and (d) without HFMD for electrons.

parasitic capacitance. These findings further emphasize that the observed behavior is independent of the breakdown voltage, but dependent on the drift region design, i.e., onset of QS or SCM.

Thus, the drift region engineering is essential to avoid early onset of SCM, by minimizing the electric field peaking and carrier crowding, to prevent the dual-mode ON-state breakdown. Furthermore, it will not be an exaggeration to counter that the dual-mode ON-state breakdown in the output characteristics of the high voltage LDMOS device is independent of the parasitic n-p-n bipolar triggering. Therefore, it is indispensable to validate our findings with reasonable counterarguments and computational experiments.

IV. Root Cause

A. Role of HFMD—Probing the Root Cause

At high current conditions, the effect of HFMD in the drift region becomes prominent as it leads to charge modulation and therefore field localization. To validate the effect of mobility degradation in the dual-mode current conduction, the LDMOS device is simulated with and without the HFMD model while accounting for the electron and hole contribution in the device behavior, as shown in Fig. 10. Without the HFMD model, the drain current does not show compression at lower drain voltages and $V_{BD-ON-1}$ vanishes completely. It should be observed from Fig. 10(a) and (b) that once the current discontinuity occurs due to electric field relocation, the drain current with HFMD model attempts to reach back at the current level without HFMD. This confirms the impact of mobility degradation in compression and recovery mode of current conduction in the presence of SCM/QS.

To further understand the role of parasitic bipolar, a computational experiment was carried out using the HFMD model. When HFMD model is switched-OFF for holes and only electrons (majority charge carriers) are acting, the excessive generation of electrons and holes due to impact ionization enhances the current density. The device shows an early breakdown,

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 04:46:53 UTC from IEEE Xplore. Restrictions apply.

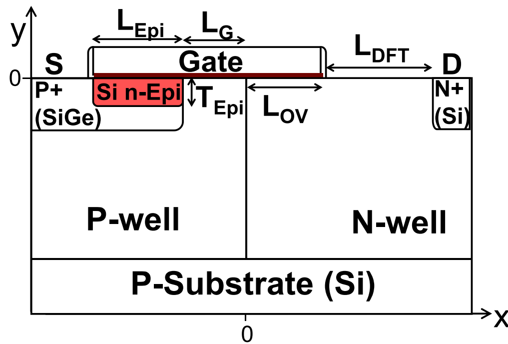

Fig. 11. Schematic of the proposed LDTFET where the device design parameters include epi length (L_{Epi}) = 330 nm, epi thickness (T_{Epi}) = 20 nm, and epi doping (N_{Epi}) = 1×10^{20} cm^{-3}. The source-to-drain pitch of LDTFET is same as the LDMOS in the previous section.

as shown in Fig. 10(c). The avalanche-injected holes (minority charge carriers) are swept away by the high electric field from the space charge region near the drain to the channel region, increasing the mobility of holes. This essentially turns-ON the parasitic bipolar and current rises faster in the recovery mode due to enhanced bipolar efficiency, leading to early $V_{\mathrm{BD-ON-2}}$. On the other hand, when HFMD model for electrons are switched-OFF and only holes are acting, no compression in I_{D}–V_{DS} curve is observed, as shown in Fig. 10(d). This is because the carrier density is not high enough to cause SCM and electric field localization at the drain till higher gate voltages, resulting in wholly disappeared $V_{\mathrm{BD-ON-1}}$. This proves that the dual-mode ON-state breakdown behavior of LDMOS device results from HFMD due to electrons instead of holes, and the parasitic n-p-n has no role to play in it.

B. Model Validation—What Happens When Parasitic N-P-N Was Missing?

For more robust validation, we choose a LDTFET device, as shown in Fig. 11, with a similar drift region profile as LDMOS but a tunneling source to eliminate the effect of parasitic n-p-n action. The investigation of tunnel FET concept in drain extended MOS has already been reported [23]. The LDTFET device uses a p^{+} SiGe source with a Si n-Epi region beneath the gate-stack instead of a n^{+} Si source diffusion, and so, it intrinsically cannot have a parasitic bipolar. The device's working principle is based on the area tunneling of minority charge carriers from p^{+} SiGe source into the Si n-Epi region along the gate field, where the thermionic carrier injection at the source side is replaced by band-to-band tunneling (BTBT)-based carrier injection. The high current behavior of LDTFET is captured using a nonlocal BTBT model, apart from the models used in LDMOS device. This model uses two-band dispersion relationship for evaluating tunneling probability and SRH recombination model for trap-assisted tunneling, which is thoroughly discussed in [25].

Fig. 12(a) shows that the n-Epi region at the source side of LDTFET device is designed in such a way that its ON-current (I_{ON}) nearly matches that of the LDMOS in the absence of high field effects. Interestingly, for the same n-Epi design, the LDTFET device in the presence of the HFMD effects exhibits similar output characteristics with the dual-mode

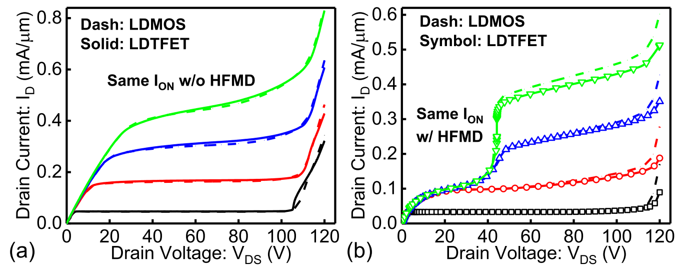

Fig. 12. Comparison of I_{D}–V_{DS} characteristics between LDMOS and LDTFET devices (a) without and (b) with the HFMD model. The comparison is made based on similar ON-currents in both devices.

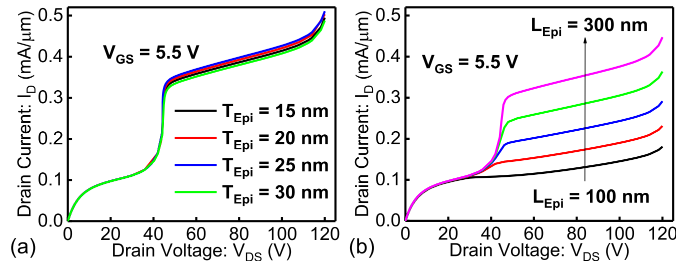

Fig. 13. I_{D}–V_{DS} characteristics of LDTFET with variation in (a) n-Epi thickness (T_{Epi}) and (b) n-Epi length (L_{Epi}) with a step size of 50 nm at $V_{\mathrm{GS}} = 5.5$ V.

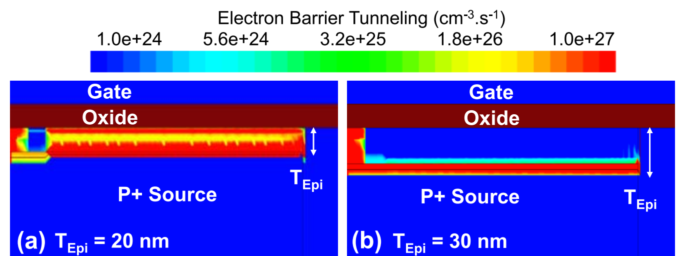

Fig. 14. ON-state electron barrier tunneling rate between the p^{+} SiGe source and Si n-Epi region. (a) $T_{\mathrm{Epi}} = 20$ nm and (b) $T_{\mathrm{Epi}} = 30$ nm.

ON-state breakdown at similar drain voltage as LDMOS. This confirms that the parasitic n-p-n is not the root cause behind the observed device behavior rather it is purely dependent on the behavior of the drift region.

The key parameters associated with the source-side design are the n-Epi thickness (T_{Epi}) and n-Epi overlap length under the gate oxide (L_{Epi}). Figs. 13(a) and 14 show that for smaller T_{Epi}, the carrier tunneling rate from the source-to-drain increases, increasing the current density in the recovery mode. As T_{Epi} reaches 30 nm, the current drops, due to increased barrier width for carrier tunneling and reduced gate control over the tunnel junction. Figs. 13(b) and 15 show that for smaller L_{Epi}, the low carrier density and no electric field localization at the drain depict a delayed SCM/QS and completely vanished $V_{\mathrm{BD-ON-1}}$. However, on increasing L_{Epi}, the overall BTBT area increases, which increases the carrier injection from the source-to-drain and induces the SCM/QS effects. Thus, by increasing T_{Epi} and reducing L_{Epi}, one can control the carrier injection rate from the source into the drain. As soon as we limit the number of carriers injected into the drift region to less than the carriers required to

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 04:46:53 UTC from IEEE Xplore. Restrictions apply.

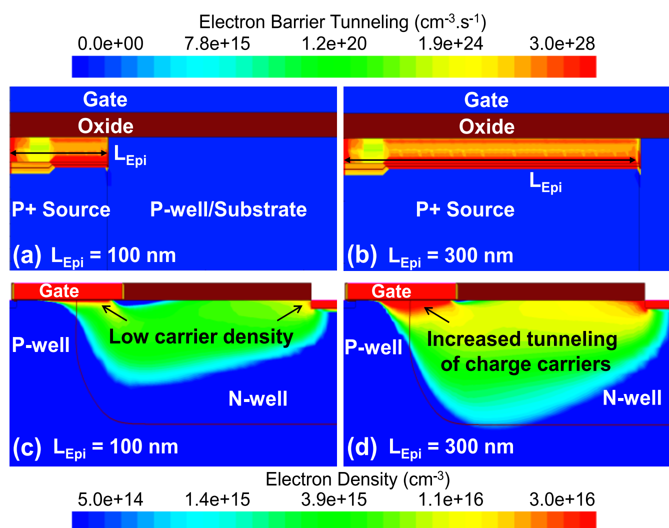

Fig. 15. ON-state electron barrier tunneling rate between the p^+ SiGe source and Si n-Epi region for (a) L_{Epi} = 100 nm and (b) L_{Epi} = 300 nm. Electron density across the device for (c) L_{Epi} = 100 nm and (d) L_{Epi} = 300 nm.

cause SCM, the drain current compression disappears, and $V_{BD-ON-1}$ completely vanishes.

V. Conclusion

Dual-mode ON-state breakdown, often observed in rugged LDMOS devices, is investigated in this work. Much before the avalanche breakdown, the drain current discontinuity in the output characteristics was shown to be related to the SCM and HFMD in the drift region at lower drain voltages. Interestingly, the drain current recovery at higher drain and gate voltages was also found to be dependent on the SCM-induced QS behavior. The observed behavior was found to be independent of parasitic n-p-n but dependent on drift region design. An LDTFET device with a tunneling source was chosen to validate the arguments. It was found that for the same ON-current, the LDTFET device exhibits the same output characteristics as LDMOS, even in the absence of the parasitic n-p-n bipolar. However, when the carrier injection from the channel to the drift region was lowered by reducing the source-side tunneling rate, dual-mode ON-state breakdown behavior disappeared. This further validated that the parasitic n-p-n bipolar is not the root cause behind the onset of the ON-state breakdown and engineering the drift region to avoid early SCM is the key to prevent the dual-mode ON-state breakdown.

References

[1] B. J. Baliga, "Power MOSFETs," in *Fundamentals Power Semiconductor Devices*. Boston, MA, USA: Springer, 2008, pp. 276–503.

[2] Z. Parpia and C. A. T. Salama, "Optimization of RESURF LDMOS transistors: An analytical approach," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 789–796, Mar. 1990.

[3] A. W. Ludikhuize, "A review of RESURF technology," in *Proc. 12th Int. Symp. Power Semiconductor Devices*, 2000, pp. 11–18.

[4] M. Shrivastava, M. S. Baghini, H. Gossner, and V. R. Rao, "Part I: Mixed-signal performance of various high-voltage drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[5] P. L. Hower, "Safe operating area—A new frontier in LDMOS design," in *Proc. 14th Int. Symp. Power Semiconductor Devices*, 2002, pp. 1–8.

[6] M. Shrivastava and H. Gossner, "A review on the ESD robustness of drain-extended MOS devices," *IEEE Trans. Electron Devices*, vol. 12, no. 4, pp. 615–625, Dec. 2012.

[7] Y. S. Chung and B. Baird, "Electrical-thermal coupling mechanism on operating limit of LDMOS transistor," in *IEDM Tech. Dig.*, Dec. 2000, pp. 83–86.

[8] H. Li, K. B. Sundaram, Y. Zhou, J. A. Salcedo, and J.-J. Hajjar, "Characterization and modeling of the transient safe operating area in LDMOS transistors," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2019, pp. 1–5.

[9] H.-J. Schulze, F.-J. Niedernostheide, F. Pfirsch, and R. Baburske, "Limiting factors of the safe operating area for power devices," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 551–562, Feb. 2013.

[10] P. Moens and G. Van den Bosch, "Characterization of total safe operating area of lateral DMOS transistors," *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 3, pp. 349–357, Sep. 2006.

[11] P. Hower, J. Lin, S. Haynie, S. Paiva, R. Shaw, and N. Hepfinger, "Safe operating area considerations in LDMOS transistors," in *Proc. 11th Int. Symp. Power Semiconductor Devices*, vol. 1999, pp. 55–58.

[12] A. W. Ludikhuize, "Kirk effect limitations in high voltage IC's," in *Proc. 6th Int. Symp. Power Semiconductor Devices*, 1994, pp. 249–252.

[13] V. Khemka, V. Parthasarathy, R. Zhu, A. Bose, and T. Roggenbauer, "Experimental and theoretical analysis of energy capability of RESURF LDMOSFETs and its correlation with static electrical safe operating area (SOA)," *IEEE Trans. Electron Devices*, vol. 49, no. 6, pp. 1049–1058, Jun. 2002.

[14] T. Khan, V. Khemka, R. Zhu, and A. Bose, "Rugged dotted-channel LDMOS structure," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4.

[15] M. Shrivastava, J. Schneider, M. S. Baghini, H. Gossner, and V. R. Rao, "Highly resistive body STI NDeMOS: An optimized DeMOS device to achieve moving current filaments for robust ESD protection," in *Proc. IEEE Int. Rel. Phys. Symp.*, Oct. 2009, pp. 754–759.

[16] M. S. Bhoir, K. N. Kaushal, S. R. Panda, A. K. Singh, H. S. Jatana, and N. R. Mohapatra, "Source Underlap—A novel technique to improve safe operating area and output-conductance in LDMOS transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4823–4828, Nov. 2019.

[17] P. Hower *et al.*, "A rugged LDMOS for LBC5 technology," in *Proc. 17th Int. Symp. Power Semiconductor Devices*, vol. 2005, pp. 327–330.

[18] J. Lin and P. L. Hower, "Two-carrier current saturation in a lateral DMOS," in *Proc. Int. Symp. Power Semiconductor Devices*, 2006, pp. 1–4.

[19] S. Reggiani *et al.*, "Explanation of the rugged LDMOS behavior by means of numerical analysis," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2811–2818, Nov. 2009.

[20] C.-C. Cheng *et al.*, "Investigation of parasitic BJT turn-on enhanced two-stage drain saturation current in high-voltage NLDMOS," in *Proc. IEEE 23rd Int. Symp. Power Semiconductor Devices*, May 2011, pp. 208–210.

[21] H.-L. Chou *et al.*, "0.18 μm BCD technology platform with best-in-class 6 V to 70 V power MOSFETs," in *Proc. 24th Int. Symp. Power Semiconductor Devices*, Jun. 2012, pp. 401–404.

[22] B. S. Kumar and M. Shrivastava, "Part I: On the unification of physics of quasi-saturation in LDMOS devices," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 191–198, Jan. 2018.

[23] M. Shrivastava, "Drain extended tunnel FET—A novel power transistor for RF and switching applications," *IEEE Trans. Electron Devices*, vol. 64, no. 2, pp. 481–487, Feb. 2017.

[24] B. S. Kumar and M. Shrivastava, "Part II: RF, ESD, HCI, SOA, and self heating concerns in LDMOS devices versus quasi-saturation," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 199–206, Jan. 2018.

[25] K. Hemanjaneyulu and M. Shrivastava, "Fin enabled area scaled tunnel FET," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3184–3191, Oct. 2015.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 04:46:53 UTC from IEEE Xplore. Restrictions apply.