Physics of Current Filamentation in ggNMOS Devices Under ESD Condition Revisited

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***Abstract*—This paper revisits the physics of current filamentation in grounded-gate NMOS (ggNMOS) devices and presents new physical insights which were not addressed in earlier works. A clear distinction between electrical and thermal instabilities is presented. Moreover, filament dynamics under electrical and thermal instability in both silicided and silicide blocked devices is discussed while highlighting observations which contradict with established theory of current ballasting. Interplay between electrical and thermal instabilities and its dependence on the presence or absence of silicide blocking is explored further. Filament spreading in ggNMOS devices and it is dependence on silicide blocking is discussed. Finally, while using the developed physical insights, missing correlation between TLP and HBM extracted failure current of silicided ggNMOS device is explained.**

***Index Terms*—Current filamentation, electrical instability (EI), electrostatic discharge (ESD), grounded-gate NMOS (ggNMOS), nonuniformnonuniform triggering, secondary breakdown, TCAD.**

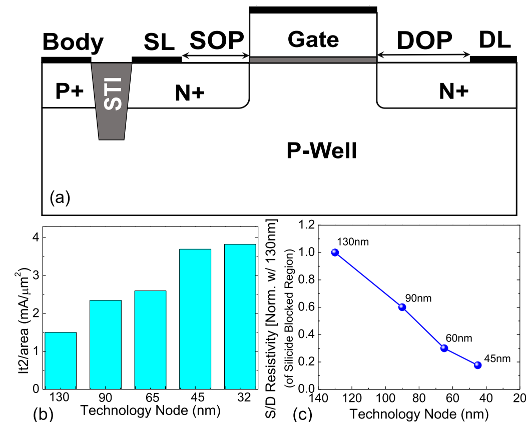

Fig. 1. (a) Cross-sectional view of ggNMOS device. (b) Failure current (It2) of ggNMOS device with technology scaling extracted from [15] and [16]. (c) Normalized S/D resistivity of silicide blocked region with technology scaling.

I. Introduction

GROUNDED-GATE NMOS (ggNMOS), as depicted in Fig. 1(a), based electrostatic discharge (ESD) protection concepts are well established in advanced planar CMOS nodes [1], [2] with a potential to be used in the FinFET technology as well [3]. In advanced CMOS nodes, silicided devices were found to suffer from current filamentation and early ESD failure [4], which was conventionally attributed to nonuniform parasitic bipolar turn-*on* [5], [6]. Parasitic bipolar turn-*on* results in negative differential resistance (NDR) state [7], which leads to a voltage snapback and often device failure before achieving a holding state. The nonuniform turn-*on* is suppressed by introducing silicide blocking in the drain and source region [8]. Silicide blocking has consistently shown significant improvement in failure current (It2) for a number of CMOS nodes [9], [10]. This improvement with silicide blocking is often attributed to current ballasting [8] across the device width. It is believed that the added S/D resistance, due to silicide blocking, helps in ballasting the current across the device width. However, this theory was never supported by extensive 3-D TCAD-based explorations, except some early investigations reported in [11]. Literary works till date [12]–[14] have described current instabilities leading to filament formation in semiconductor devices either due to isothermal effects or attributed purely to thermal effects at high currents. This paper for the first time presents a thorough analysis of these two and the interaction-correlation between the two types of filament instabilities present in ggNMOS devices. The nonuniform conduction across the device is evidently a 3-D phenomenon; hence, this paper uses a 3-D TCAD approach for fundamental explorations of such a scenario, which results in precise understanding to build deeper physical insights [3].

Based on experimental observations [2], [4], [17], [18] for silicide blocked ggNMOS devices from over five CMOS generations, as depicted in Fig. 1, this paper brings several pertinent questions related to filament dynamics and criteria for current instabilities in ggNMOS devices. Moreover, the conditions under which these instabilities become critical for device failure is presented in detail. The inconsistencies

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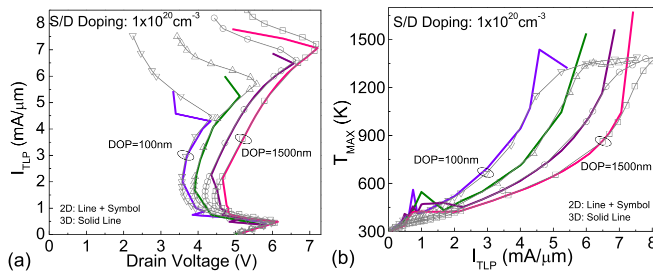

Fig. 2. (a) TLP I–V characteristics, and (b) TMAX vs. ITLP characteristics for ggNMOS device with different silicide blocking lengths extracted from 2-D and 3-D TCAD simulations. 3-D ggNMOS simulations are performed for a device width of 10 μm.

of current ballasting theory in ggNMOS devices and its relation with the silicide block resistance are summarized in Section II. Sections III and IV uncover the physics of current filamentation in ggNMOS devices while exploring thermal and electrical instabilities to probe filament dynamics as a function of technology and design parameters. In Section V, we have used the developed understanding to explain missing correlation between HBM and TLP extracted failure current, in particular for silicided ggNMOS devices. Finally, the new findings are concluded in Section VI.

II. 2-D Versus 3-D: Contradictory Observations

Although planar technologies are quite matured, there is a great need to understand the scientific aspects of current filamentation in ggNMOS devices, since for the development of advanced CMOS technologies such as FinFET and Nanowires a lot of understanding is borrowed from planar CMOS generations. Fig. 1(b) shows experimentally extracted It2 trends with technology scaling [15]. It is interesting to note that the It2 per unit area of a silicide blocked device improves with technology scaling, despite its lowered S/D sheet resistance [Fig. 1(c)], due to the increased S/D doping.

Fig. 2(a) and (b) shows the TLP I–V and lattice temperature versus TLP current characteristics of ggNMOS device with finite silicide blocking lengths, extracted using 2-D as well as 3-D TCAD simulations. The It2 failure criteria in the TCAD simulations was considered to be the current value corresponding to the second snapback observed in the TLP I–V characteristics. It was also ensured that the simulated structure's width is kept sufficiently big (10μm) such that the filamentary behavior and It2 is not dependent on the device width. The simulation framework adopted for this investigation is borrowed from [19]–[22]. 2-D TCAD enforces uniform electrical and thermal conditions along the width plane of the device. Variations in electrical and thermal response of the device in width plane is, however, naturally captured when 3-D geometry is studied using 3-D TCAD simulations [3]. It is interesting to note from Fig. 2 that there is no change in high current TLP characteristics of silicide blocked ggNMOS devices predicted using 2-D and 3-D TCAD simulations. However, in the NDR region, after the first snapback, varying snapback depths with increasing pulse amplitude is clearly evident from 3-D TCAD simulations, unlike the smooth NDR region predicted by 2-D simulations. This could be termed as the onset of electrical instability (EI), which shall be discussed in detail in Section III. Typically, this instability is a nonthermal effect and is attributed to the nonuniform turn-*on* of the parasitic bipolar across the device width, which can be clearly seen from the 3-D results. It can also be noticed that the predicted onset of second snapback was the same from both 2-D and 3-D simulations regardless of steep rise in lattice temperature present in 3-D simulations due to presence of current filament, which was naturally missing in 2-D simulations. This current filamentation is due to the thermal instability, which leads to the formation of destructive current filaments at higher stress values, effectively captured by 3-D simulations. Fig. 3(a) shows improvement in It2 when S/D doping was increased as a result of technology scaling, which was found to be independent of substrate resistivity. To ensure that impact of substrate resistivity is captured, two extreme cases are studied here: high resistive (HR) substrates with doping 1×10^{15} cm^{-3}, and low resistive substrates with doping 1×10^{18} cm^{-3} (LR). Finally, Fig. 3(b) and (c) depicts It2 and power-to-fail improvement with the increase in silicide blocking length (DOP). This was surprisingly found to be independent of dimensionality of geometry studied for finite silicide blocking length. However, for silicided devices, 2-D simulations tend to overestimate failure current when compared to 3-D simulations. In other words, silicide blocking, which is often discussed to offer current ballasting, was found to improve failure current even when injected current was forced to flow uniformly in the width plane—by using 2-D TCAD simulations. This indeed is counter intuitive while referring to earlier discussions on silicide blocking. With all care, these observations indicate contradictions with conventional theory of current ballasting and role of S/D ballast resistance. For example, as reported in [5] and [11], the purpose of silicide blocking is to increase S/D resistance, which has been often discussed to increase current ballasting in width plane. However, It2 improvement depicted in Fig. 3 by reducing S/D resistance, which can be observed from 2-D simulations as well, signifies that It2 improvements due to silicide blocking may not be entirely due to 3-D current ballasting or may not be a 3-D phenomena as believed in earlier works. Conventionally, it is believed that silicide blocking mitigates early filament formation or bipolar instability by increasing S/D resistance, which is expected to offer a ballasting action.

Furthermore, contradictory observations depicted above raise important concerns regarding the correlation between current instabilities and failure in relation with silicide blocking and S/D resistance. For instance, it is not clear how silicide blocking improves the ESD robustness of the device. If the nonuniform conduction along the width plays a critical role, then why It2 extracted using 2-D and 3-D simulations are the same, as depicted in Fig. 2. This paper aims to address these relevant questions in the subsequent sections for a unified understanding.

III. Electrical Instability (EI)

Section II highlights, though it has been observed at various occasions in the past, that It2 improves significantly with

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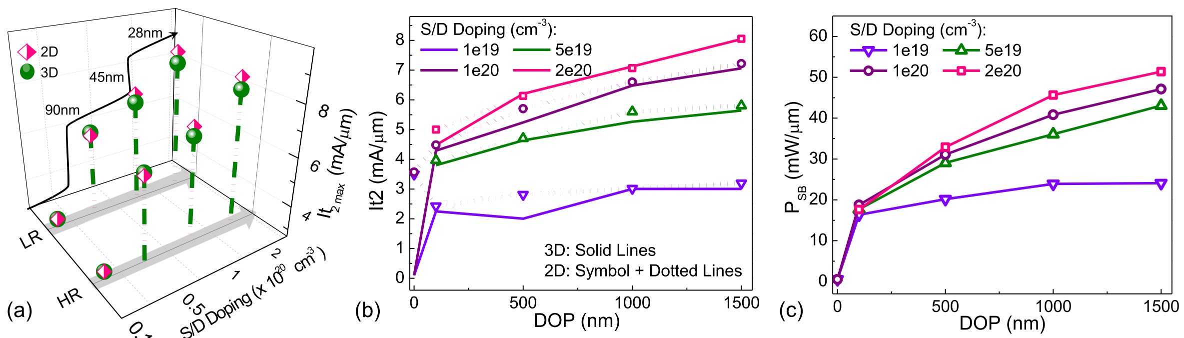

Fig. 3. It2 and power to fail as a function of S/D doping. (a) It2 versus S/D doping for substrates with different resistivities. (b) It2 versus drain side silicide blocking length (DOP) for a different S/D doping. The characteristics shown are extracted using both 2-D and 3-D TCAD simulations. 3-D ggNMOS simulations are performed for a device width of 10 μm. (c) Power to fail versus DOP for a different S/D doping extracted using 3-D TCAD simulations.

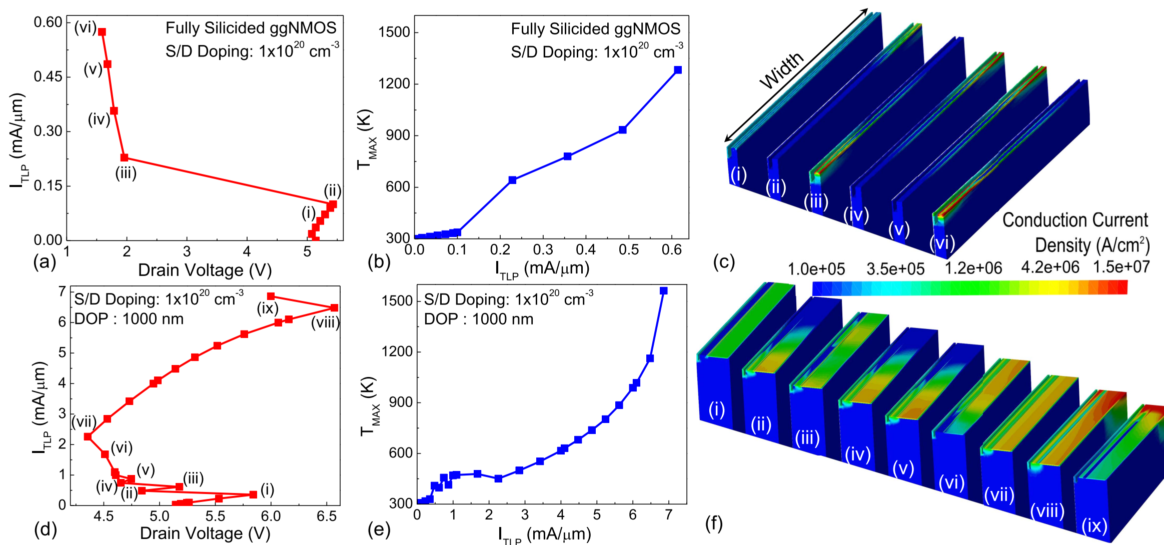

Fig. 4. TLP characteristics and conduction current density extracted for two extreme DOP values, from 3-D TCAD simulations, for a device width of 10 μm. (a) and (b) TLP characteristics of silicided ggNMOS device. (d) and (e) TLP characteristics of silicide blocked ggNMOS device. (c) 3-D current density countour extracted (at 100 ns) across silicided ggNMOS device at different currents depicting a filamentary state or presence of EI right after first snapback, which is independent of stress current. (f) 3-D current density countour extracted (at 100 ns) across silicide blocked ggNMOS device at different currents depicting a filamentary state or presence of EI right after first snapback, which recovers to a spreading state at moderate current and eventually leads to a uniform conduction state at higher stress currents.

higher silicide blocking length, DOP as well as with advancing technology node. From 3-D TCAD simulations point of view, we have considered two extreme cases in this section, to begin with. Fig. 4(a) and (d) shows TLP I–V characteristics of silicided ggNMOS device and a silicide blocked ggNMOS device with relatively high DOP and high S/D doping. This allows two extremes to compare, one with least It2 (silicided) and other having highest It2 (silicide blocked), respectively. Furthermore, Fig. 4(b) and (e) compares maximum lattice temperature across both the devices, respectively, as a function of stress current, extracted at 100 ns of TLP pulse. Fig. 4(c) and (f) compares 3-D current density contours across both the devices, respectively, probed at 100 ns of TLP pulse, with TLP current ranging from snapback current (It1) to little higher than holding current (I_{HOLD}). Fig. 4 reveals that the device undergoes an EI right after first snapback and thermal instability around second snapback at higher currents. This is independent of presence or absence of silicide blocking. However, in case of silicide blocked device, state with uniform conduction is present at moderate currents. This highlights that in case of a silicide blocked device, filament spreading takes place immediately after filament instability post first snapback. This is attributed to thermally induced current homogenization due to the negative temperature coefficient of impact ionization (II), [23] which leads to a uniform conduction state and delayed thermal failure. The same, however, is missing in case of silicided device, which causes filament formation after instability and a significant increase in lattice temperature leading to catastrophic failure. It should be noted here that silicide material in addition degrades at much lower temperature than the silicide blocked material (i.e., silicon), [24] which is another factor for early destruction of silicided device.

It was noticed that EI causing an early filament formation and thermal filament at higher currents leading to

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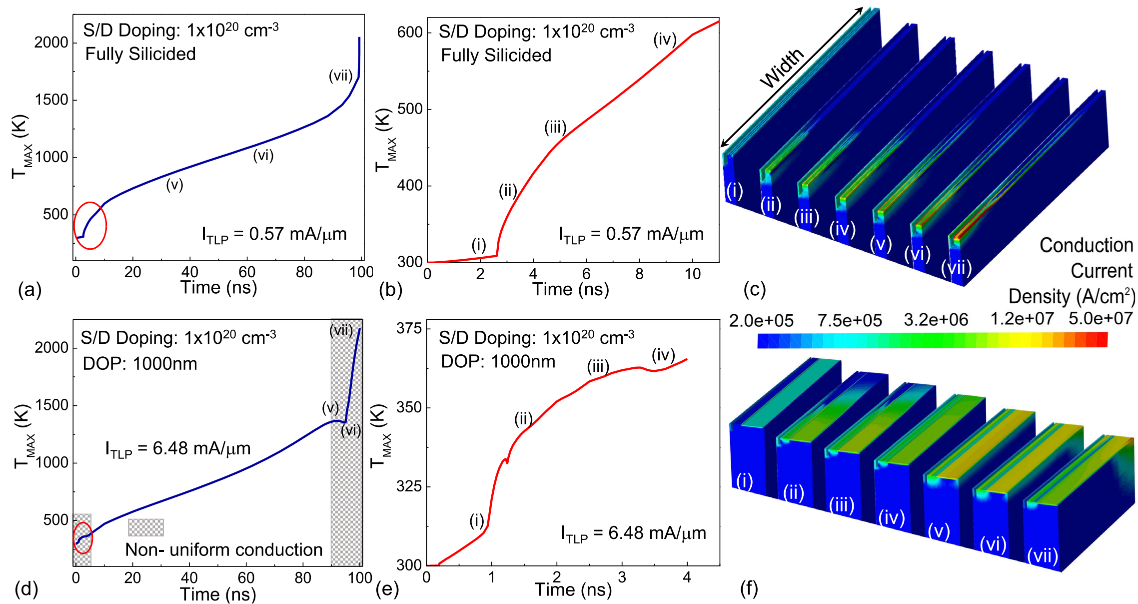

Fig. 5. Maximum lattice temperature versus stress time, extracted across ggNMOS devices stressed close to failure threshold for (a) and (b) silicided and (d) and (e) silicide blocked devices, extracted from 3-D TCAD simulations, for a device width of 10 μm. Evolution of current filament across (c) silicided and (f) silicide blocked device. Figure depicts three distinct events or states, namely, 1) nonuniform EI; 2) uniform conduction across the device followed by; and 3) thermal filament formation or runaway. The intermediate state is missing for silicided device.

failure are two distinct events. However, they can have an interplay in some specific conditions, specially in case of silicided devices. This is further explored in Fig. 5, where Fig. 5(a) and (b) shows maximum lattice temperature as a function of stress time, across a silicided device, while keeping stress current slightly higher than It1. Note that silicided device was found to fail immediately after It1 (It1 = It2). Similarly, Fig. 5(d) and (e) shows the same for silicide blocked device, while keeping stress current the same as It2 (It2 $\gg$ It1). Fig. 5(c) and (f) shows conduction current density at different stress times, depicting different states of current filamentation across silicided and silicide blocked devices, respectively. For silicided device, it can be noticed that a persistent filamentary state exists, which is independent of stress time, once the filament is formed. It can be noticed that the filament was formed at smaller stress times, when the lattice heating was merely negligible. This is due to an EI right after bipolar turn-*on* or first snapback. The sharp increase in lattice temperature immediately after this first snapback is attributed to EI, which leads to this persistent filamentary state in silicided devices. On the other hand, for silicide blocked device a temporary filament was seen after bipolar turn-*on*, which later, i.e., at higher stress times, spreads across the entire conduction plane. This resulted in a dip in lattice temperature as a function of stress time, which signified the presence of current spreading after EI. In silicide blocked device, a uniform conduction state can be noticed, after initial EI or filament formation, at moderate stress times. This, however, is missing in silicided device, due to this, on one hand, silicided devices experiences a sharp increase in lattice temperature, which leads to thermal instability or runaway right after EI. On the other hand, silicide blocked device experiences a gradual increase in lattice temperature which delays its failure. Finally, at higher stress times, silicide blocked device experiences another filamentary state, attributed to thermal instability or thermal runaway. In summary, these observations reveal that in principle both ggNMOS devices undergo the following distinct events when stressed under ESD conditions.

1) An EI causing nonuniform turn-*on* and filament formation.
2) Persistent filamentary state in case of silicided device, which leads to sharp increase in lattice temperature.
3) Filament spreading and uniform conduction in case of silicide blocked devices, which relaxes lattice temperature.
4) Thermal instability, as soon as lattice temperature exceeds critical temperature, which leads to thermal failure or runaway.

For completeness, the EI causing nonuniform turn-*on* can be explained as follows. At the verge of snapback, the nonuniform II at the drain side [Fig. 6 (a)], leads to nonuniform base-emitter junction potential (V_{BE}) drop. A slight change in V_{BE} [Fig. 6(b)] perturbs the emitter current exponentially [Fig. 6(c)]. This in turn boosts further localization of II, as depicted in Fig. 6(d). This phenomena sets up a stage for regenerative/positive feedback between nonuniform carrier generation leading to nonuniform turn-*on*, which causes EI and formation of early current filament at the verge of first snapback.

To validate our arguments above, Fig. 7 compares TLP I–V characteristics of (a) silicided and (b) silicide blocked device extracted using electrothermal simulations with the same extracted using isothermal simulations. Presence of filament instability or formation of filament in isothermal 3-D simulations confirms that the instability present at the verge of snapback is truly electrical in nature, which is present in both

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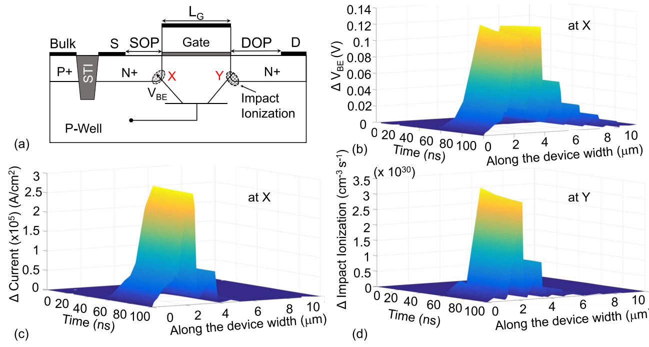

Fig. 6. (a) ggNMOS device schematic and critical probe locations. (b) Base to Emitter voltage(V_{BE}) at location X versus stress time and device width. (c) Conduction Current Density at location X versus stress time and device width. (d) II at location Y versus stress time and device width, extracted from 3-D TCAD simulations, for a device width of 10 μm [25].

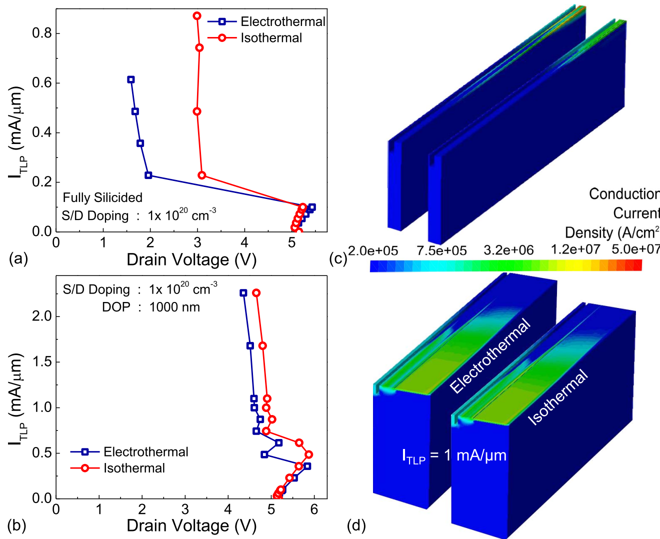

Fig. 7. TLP *I*–*V* characteristics and conduction current density contours extracted using isothermal as well as electrothermal 3-D simulations for device width = 10 μm, for (a), (c) silicided and (b), (d) silicide blocked ggNMOS device respectively.

silicided as well as silicide blocked devices. It was also found that as the stress current density increases, the rate at which filament instability takes place increases too. This is further accelerated by presence of lattice heating, which can also be confirmed from Fig. 7. The current further localizes as a consequence of this positive feedback mechanism, which leads to a significant increase in lattice temperature, causing device failure. At this stage, it is worth highlighting, as depicted in Fig. 8, that increasing DOP, S/D doping, and substrate resistivity shifts T_{CRIT} to higher values. This is attributed to the spreading of the filament which mitigates the EI.

This is evident for 2-D ggNMOS device simulations as well, where there is no scope of nonuniformity to be present along the width direction. The extent of filament spreading improves with DOP, which has been verified in Fig. 9. Here, the silicide blocking length has been changed, however, keeping the total junction area constant (i.e., the total junction length = silicide blocking length + silicided region length). Clearly, when the junction area was kept constant, It2 was found to be independent of DOP. However, with increase in DOP, It2 was

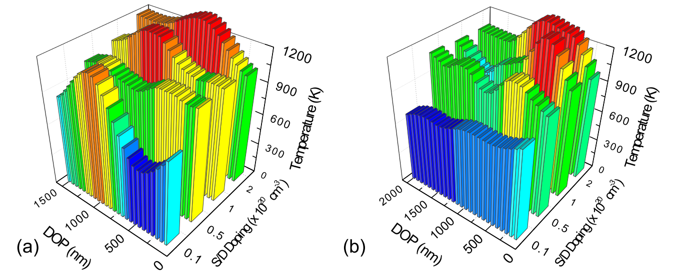

Fig. 8. Critical lattice temperature for the onset of thermal filament/failure across ggNMOS device as a function of DOP, technology node (i.e., S/D doping) and substrate types, extracted using 3-D TCAD simulations (for device width = 10 μm), for (a) LR substrates and (b) HR substrates.

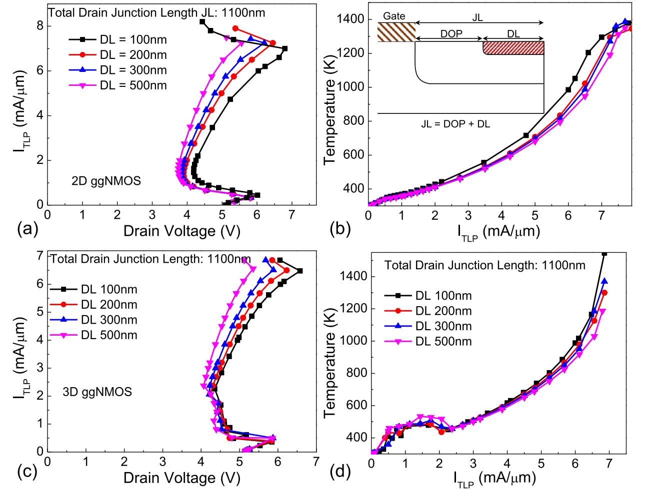

Fig. 9. TLP *I*–*V* characteristics and Lattice Temperature vs. ITLP curves for (a), (b) 2-D ggNMOS and (c), (d) 3-D ggNMOS device, respectively, keeping total drain junction length (JL = DOP + DL) constant while increasing the drain contact length (DL) only, i.e., by reducing the silicide blocked length (DOP).

found to improve for both 2-D as well as for 3-D structures, which is due to the vertical current spreading enabled by increased junction area. The same lowers the space charge density thereby relaxing peak electric field, which brings the peak lattice temperature down and improves device failure by shifting T_{CRIT} to higher values. The improved current spreading and controlled EI is also evident from Fig. 10(a), which depicts increased It1 as a function of DOP. In particular, there is an abrupt jump in It1 from silicided devices (DOP = 0) to silicide blocked devices (DOP > 0). As a result of this instability, which is naturally missing in 2-D simulations, the ratio of failure current extracted from 2-D and 3-D simulations is significantly greater than one for silicided devices (DOP = 0), whereas it is close to one for silicide blocked devices. This is depicted in Fig. 10(b), which signifies role of EI in silicided devices, which, however, is mitigated in silicide blocked devices. The relation between T_{CRIT} and DOP with details of device failure dynamics are explained in Section IV.

IV. Thermal Instability: Current Filamentation Leading to Device Failure

So far, we have explored dynamics of EI and how it is related to S/D doping and silicide blocking. However, why silicide blocking mitigates EI is not clear yet.

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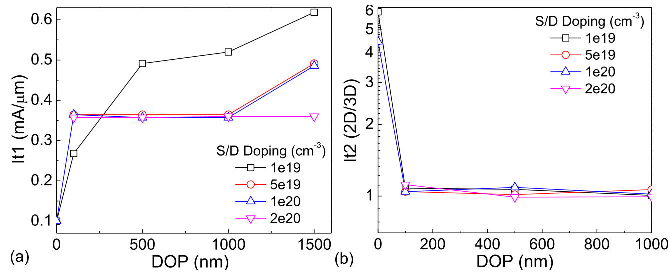

Fig. 10. (a) Change in trigger current (It1) with respect to the silicide blocked length (DOP) and S/D Doping. (b) Ratio of failure current (It2) extracted from 2-D and 3-D simulations for device width = 10 μm.

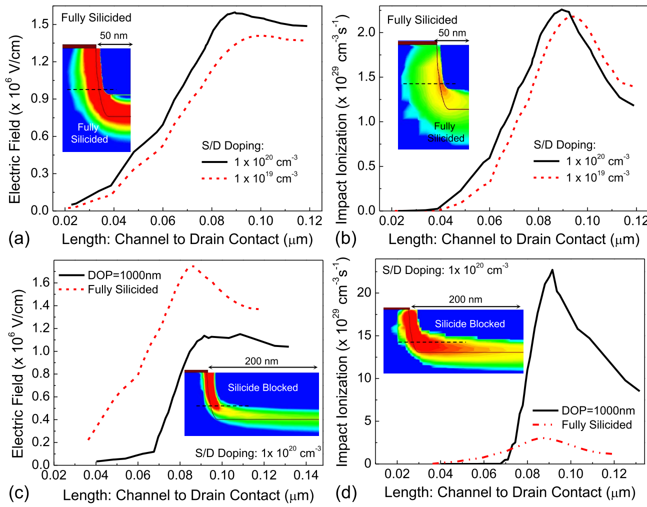

Fig. 11. Impact of (a) and (b) S/D doping density and (c) and (d) DOP on the (a) and (c) electric field and (b) and (d) II rate along drain to substrate junction, extracted from 3-D TCAD simulations, for device width = 10 μm. Inset: 2-D electric field and II profile across the drain-substrate junction for silicided as well as silicide blocked devices.

Fig. 11(a) and (b) shows that peak electric field and II rate does not change significantly as a function of S/D doping. On the other hand, Fig. 11(c) shows that the peak electric field along the drain-channel junction falls as the silicide blocking length is increased. Furthermore, inset contours show a relaxed peak electric field in case of silicide blocked device, which has spread across the entire drain-substrate junction. Introducing silicide blocking increases the effective junction area, which relaxes the space charge density and hence electric field. Relaxed electric field leads to relaxed lattice temperature during the event of EI as well as during the state of uniform conduction. Relaxed lattice temperature further promotes the rate of II, which strengthens filament spreading. In addition to lowering peak electric field, increased DOP, which increases the junction area, in turn increases peak II, as depicted in Fig. 11(d). Inset contours show II across entire drain-substrate junction. Enhanced II increases the number of holes present in substrate for bipolar turn-*on*, which in turn lowers the intensity of EI.

For completeness, Fig. 12 depicts that strength and onset of filament formation due to EI in silicided devices depends on gate length and S/D doping as well. With reduced S/D doping, silicided device fails at a lower current, which is attributed to

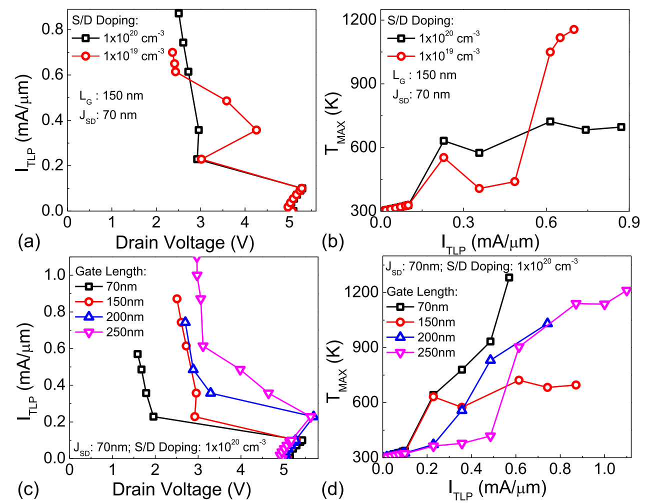

Fig. 12. TLP *I–V* characteristics of silicided ggNMOS device extracted using 3-D TCAD simulations (for device width = 10 μm) to study impact of (a) and (b) S/D doping and (c) and (d) gate length on strength and onset EI. Here, snapback depth (Vt1 − V_{HOLD}) and maximum lattice temperature right after filament instability represents strength of EI. Higher the snapback depth, hence lattice temperature, higher the EI.

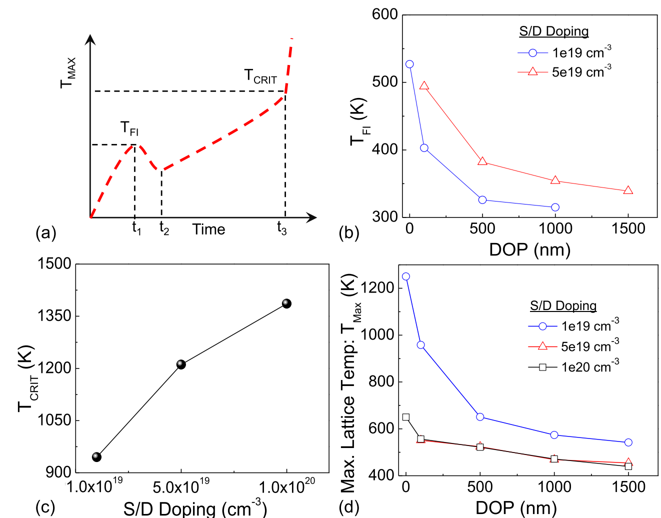

Fig. 13. (a) Dynamics of maximum lattice temperature across the device as a function of time depicting key parameters defining filament dynamics example, maximum temperature post filament instability (T_{FI}) and critical temperature required for thermal instability/filament (T_{CRIT}). (b) and (c) T_{FI} and T_{CRIT} as a function of DOP and S/D doping. (d) Maximum lattice temperature as a function of DOP and S/D doping, extracted from 3-D TCAD simulations.

lower bipolar efficiency and lower II generation access holes present to support filament spreading. Similarly, with lower gate lengths, silicided device experiences a pronounced EI at an early current, which leads to early snapback and failure. This is attributed to higher and localized electric field at gate-drain junction in the shorter channel devices. As discussed above, higher and localized electric field and localized II strengthens the EI.

Using the observations above, Fig. 13(a) shows a typical lattice temperature versus stress time behavior of a silicide blocked device. Here, T_{FI} is the peak temperature after EI,

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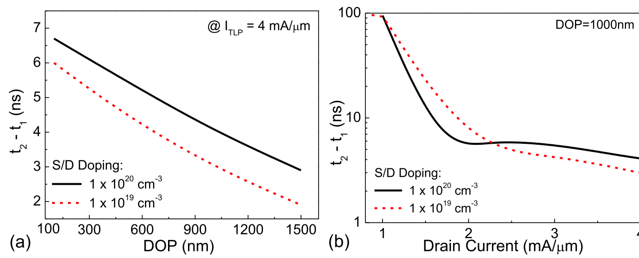

Fig. 14. Time required for the filament to spread as a function of (a) DOP and (b) stress current. Here, t1 is the onset time for filament spreading and t2 is the time when filament spreading gets over, extracted from 3-D TCAD simulations, for device width = 10 μm.

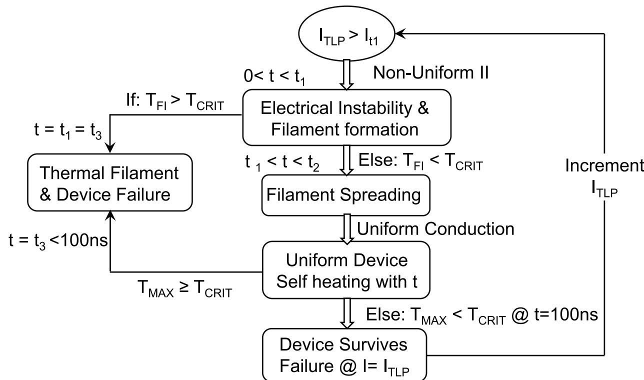

Fig. 15. Flowchart summarizing filament and failure dynamics.

T_{CRIT} is the critical temperature required for thermal instability, T_1 is the time at which filament instability achieves an equilibrium state, and thereafter device experiences a spreading state from T_1 to T_2. T_3 is the time when maximum lattice temperature across the device exceeds a critical temperature, which triggers formation of thermal filament. As the T_{FI} depends on extent of filament instability, T_{FI} falls with increasing silicide blocking length. It, however, increases with increased S/D doping as depicted in Fig. 13(b). T_{CRIT} solely depends on S/D doping and increases with drain doping concentration, as shown in Fig. 13(c). Finally, it is worth noticing, as shown in Fig. 13(d), that the maximum lattice temperature for a given current falls as S/D doping and DOP are increased.

Fig. 14(a) depicts that silicide blocking, beside delaying T_1 as discussed earlier, also shifts T_2 close to T_1. Here, $T_2 - T_1$ falls as a function of DOP. This assists the ggNMOS device with higher DOP to recover faster from the temporary filamentary state to the filament spreading. In order words, the state of current localization persists for a shorter period of time in case of higher DOP devices, which delays its failure and improves the ESD robustness. It is worth highlighting that T_2 is a strong function of injected stress current, as the event is accelerated at higher currents, whereas T_1 remains more or less unchanged. Hence, the difference rapidly falls as a function of stress current due to faster spreading at higher current, as depicted in Fig. 14(b). In any case, the recovery must be faster than the rate of change in lattice temperature for device to survive filament instability driven failure.

Based on the observations presented above, Fig. 15 summarizes the dynamics of filament formation in ggNMOS

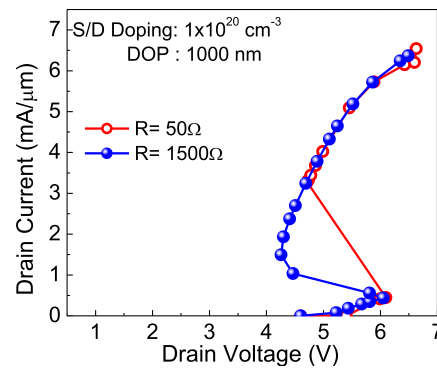

Fig. 16. TLP characteristics extracted using 50-Ω and 1500-Ω loadline to study impact of loadline resistance on snapback and failure characteristics.

devices leading to device failure. As the stress current across the device exceeds the minimum current required to turn-*on* parasitic bipolar, device experiences an EI due to uneven II profile and related positive feedback along the device width. If the maximum lattice temperature during the EI exceeds the critical temperature required for thermal filament formation, i.e., $T_{FI} > T_{CRIT}$, the device immediately undergoes thermal filament formation and consecutive failure. Otherwise, device experiences a filament spreading state, which is attributed to the fall in II rate inside the filament due to self-heating that extends filament width by triggering adjacent bipolar regions. During this period, the lattice temperature across the device relaxes significantly and leads to a uniform conduction state, where the injected stress current flows uniformly across the device width. Under this uniform conduction state, lattice temperature across the device increases gradually, which when exceeds the critical temperature limit, leads to thermal failure.

V. Loadline Dependence

The physics of nonuniform conduction and filament instability presented above also helps us explaining the missing correlation between failure current extracted using 50 Ω TLP and HBM like (1500Ω loadline) measurements. To understand this missing correlation, while using the new knowledge developed above, and relate it to filament instability post snapback, Fig. 16 compares TLP I–V characteristics extracted using HBM like (1500 Ω) and TLP like (50 Ω) loadline resistance. Except snapback and holding current, Fig. 16 shows perfect agreement in terms of breakdown, trigger, and failure characteristics when extracted using TLP and HBM like loadline resistances. From the snapback regions compared in Fig. 16, it is not difficult to extrapolate that due to lower loadline resistance in TLP setup, when compared to HBM, the holding current post EI in TLP measurements is significantly higher compared to HBM like high loadline measurements. For silicided devices, the TLP measured holding current is often higher than that of HBM like measured failure current. This leads to TLP measurements of silicided devices often depicting failure immediately after It1, hence It2 = It1. However, for HBM like high loadline resistance measurements, the device survives failure post EI, offering It2 > It1.

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VI. Conclusion

Three distinct states of current filamentation are discovered, which are 1) early filamentation due to EI after first snapback; 2) filament spreading between holding and failure current; and 3) thermal instability or runaway causing filament formation and failure near It2. The conditions required to trigger different filamentary states are discussed. In case of silicide blocked devices, all the three states are present. However, in silicided devices, filament spreading state is missing, due to which device enters into thermal runaway immediately after EI. This leads to thermal failure immediately after first snapback. It can be clearly concluded from this paper that uniform conduction and improved It2 in silicide blocked devices is not related to increased S/D resistance. Increased silicide blocking length improves It2 by spreading current deeper into the device by taking advantage of increased junction area. This further suppresses the peak electric field and enhances II rate across the drain-substrate junction, which in turn mitigates EI. This allows the filament to spread as soon as it experiences an instability. Moreover, it relaxes the peak temperature immediately after EI, which increases the gap between onset of EI and thermal instability. Furthermore, we found that as 1) the critical temperature for thermal instability and 2) II rate increases with higher background doping, increasing S/D doping improves It2 for a given DOP by delaying onset of thermal instability, unlike what conventional theory of current ballasting would have predicted.

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