On the ESD Behavior of Large-Area CVD Graphene Transistors: Physical Insights and Technology Implications

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***Abstract*— In this paper, for the first time, the record high-performance top-gated graphene technology platform is used for electrostatic discharge (ESD) physics exploration while investigating the implications of various design and technology options. Impact of diffusive versus ballistic carrier transport on the failure mechanism in top-gate as well as back-gate graphene FET (GFET) is investigated. A unique contact limited failure in graphene transistors is reported. Physical insights on current saturation in GFET and unique step-by-step failure in dielectric capped transistors are presented for the first time. Moreover, device degradation under ESD timescales and its implications on current saturation are revealed. Finally, the influence of various top-gate designs on the ESD performance is reported. New physical insights and matured GFET technology has eventually enabled record high ESD robustness.**

***Index Terms*— Contact limited failure, electrostatic discharge (ESD), graphene, RF FETs.**

I. Introduction

GRAPHENE, a single-atom-thick carbon allotrope, has been widely explored since its first demonstration [1] for RF transistor applications and its potential uses in the terahertz (THz) regime [2]. Unique band structure with extremely high carrier mobility, transconductance, and thermal conductivity makes graphene a strong contender to replace bulk semiconductors for THz applications. Over the past decade, there have been efforts from different research groups to obtain chemical vapor deposition (CVD) grown large area high-performance graphene transistors that can work in the THz regime. The graphene-metal contact resistance was proven to be a performance killer for THz application. Works in [3] and [4] have focused on optimizing the graphene-metal contacts to reduce the contact resistance. The other challenge has been in terms of achieving saturating drain current characteristics that can offer very high output impedance, hence, high-voltage gain [5], [6]. Usage of 2-D dielectrics that can offer better surface properties with graphene [7], [8] is still a topic of research.

Attributed to technological advancements and its future potential, the long-term [9]–[11] and electrostatic discharge (ESD) reliability [12], [13] of graphene FETs (GFETs) too received attention very recently. ESD reliability studies involve investigations of device failure under high-current high-voltage stress applied for a sub-100-ns duration [14]. The ESD comes under the category of electrical overstress damages in integrated circuits, which is a short-term reliability threat. Understanding the ESD behavior of novel technologies during the technology development phase not only reduces the time required for design for reliability but also lowers significant part of the technology development time. The major challenges for ESD reliability explorations in graphene technology have been: 1) unavailability of high-quality CVD-grown large-area graphene in initial years; 2) lack of matured technology; and 3) use of back-gated geometries for explorations. For instance, ESD behavior of graphene was first reported using an exfoliated material [12] and more recently [13] using CVD graphene, both without a top-gate or dielectric passivation. In this paper, for the first time, we have used a matured CVD-grown large-area graphene technology platform with record FET's performance [15] for ESD physics explorations while investigating implications of various design and technology options. It is worth highlighting that the focus of this paper is to explore the physics of current transport and failure of GFETs under ESD conditions.

This paper, which is an extension of our earlier work [16], is arranged as follows. Section II introduces various device architectures used for ESD investigations together with device fabrication details. Section III reveals the basic ESD behavior of GFET and highlights record high failure current achieved in this paper. The details regarding the electrothermal carrier transport and its implications on the device failure are presented in Section IV. Section V presents investigations on high-k dielectric encapsulated graphene transistors. Unique ESD behavior with the novel failure mechanism in dielectric encapsulated devices is presented in detail. Finally, a high-k top metal gate-stack-based GFET's robustness against ESD stress is discussed in Section VI. The role of top-gate electrode with key design guidelines is presented before concluding this paper in Section VII.

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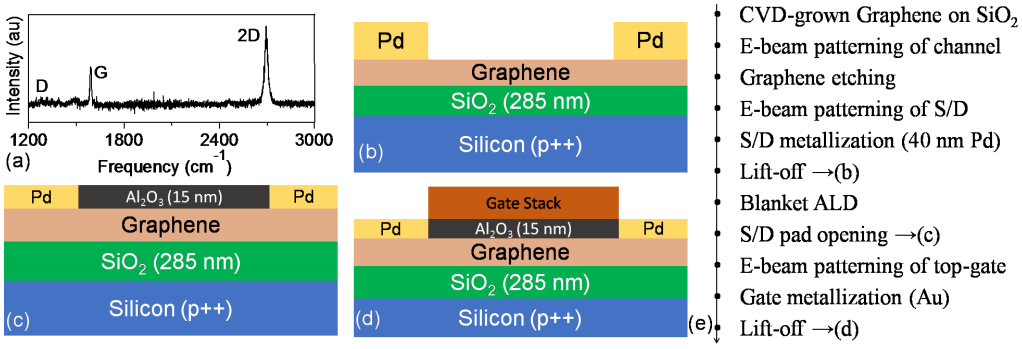

Fig. 1. (a) Sharp 2-D peak and suppressed D peak in Raman spectra of post transfer graphene indicates pristine nature of monolayer graphene. Schematic of various GFETs architectures investigated. (b) Back-gated FET. (c) Back-gated FET with dielectric capping. (d) Top-gated FET with high-k metal gate stack. (e) Process flow used in this paper for graphene device fabrication.

II. Graphene Device Fabrication and Experimental Setup

High-quality CVD grown graphene on Cu was transferred to SiO_2/Si substrate using polymethyl methacrylate-based wet transfer technique, which was then patterned using electron-beam lithography and O_2 plasma. The graphene-metal contacts are engineered, by controlled removal of carbon atoms from the monolayer graphene sheet underneath the contact region using high-energy electron beam [15]. Source/drain metal (palladium) pads were deposited using ultra high voltage electron-beam evaporation, followed by liftoff and high-temperature anneal (400 °C). At this stage, the back-gated graphene device as depicted in Fig. 1(b) is realized. To realize top-gated architectures, a blanket atomic layer Al_2O_3 deposition (ALD) was done with postdeposition dielectric anneal (400 °C). The back-gated device with dielectric encapsulation is obtained at this step, which is depicted in Fig. 1(c). Furthermore, the top-gate metal was deposited, followed by a postmetallization anneal (400 °C) to achieve top-gated graphene devices, as depicted in Fig. 1(c). The top-gated devices designed in this paper have intentional underlap and overlap of the top gate with the S/D regions. Finally, Al_2O_3 over S/D contact pads was removed using reactive ion etching to open probe pads for electrical measurements. The developed technology has resulted in record high performance as presented in detail in our earlier work [15]. For ESD investigations, the designs depicted in Fig. 1(a)–(c) were fabricated with electrical width up to 40 μm. A commercial transmission line pulse (TLP) tester as depicted in Fig. 2 with ultralow current sensing capability (50 μA) is used to extract the device I–V characteristics under ESD like conditions. The square voltage pulses with increasing pulse amplitude (up to 2 KV) are forced to the device under test (DUT) with 50 transmission line. The setup has the provision to tune forced voltage pulse duration (1 ns–1.5 μs) and rise time (100 ps–10 ns). The voltage across the device is measured with the sense probe with series resistance to control the voltage drop across the 50-Ω transmission line, and hence, a lower voltage can be seen at the input of the oscilloscope. The current is measured using the current sensor (basically a transformer) connected in the force side. The sensed voltage

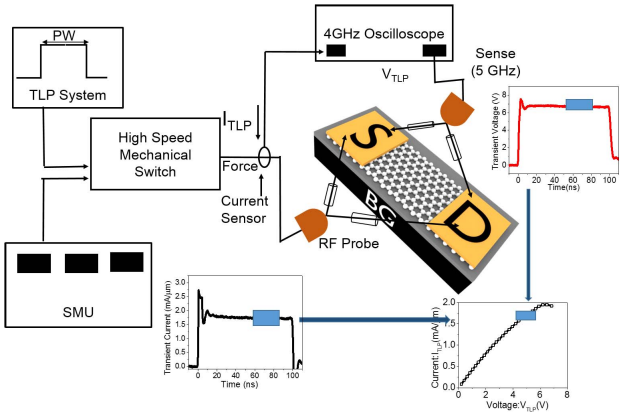

Fig. 2. TLP generation and measurement setup. Current sensor with 5-mV/mA sensitivity and 4-GHZ oscilloscope is used to measure the ultralow current with high sensitivity. The voltage and current pulses measured across the DUT are averaged out to obtain the quasi-static I–V characteristics. Consequently, between every pulse measurement a low-bias dc measurement (V_D = 0.1 V) is performed to understand the stress-induced device degradation and eventual failure.

(V_{TLP}) and current pulses (I_{TLP}) across the device are averaged out in 70%–90% of the total pulse duration to obtain one data point in the I–V characteristics. To track the stress-induced device degradation, a one-point dc measurement is performed at low-drain dc voltage after every pulse. The mechanical switch is present to change from pulse mode to the dc mode input. This point dc measurement is known as spot measurement hence the name I_{spot}. Hence, I_{TLP} is the pulse current and I_{spot} is the dc spot current.

III. GFET's ESD Behavior and Record High Failure Current

To understand the fundamental carrier transport and different electrothermal phenomena under ESD such as discharge in graphene, the back-gated architectures are used. The obtained knowledge is further extended to high-k top-gated device architectures.

Fig. 3(a) depicts TLP I–V characteristics of back-gated graphene transistor biased at different gate voltages. Inset in Fig. 3(b) reveals dc transfer characteristics (I_D–V_G) of DUT

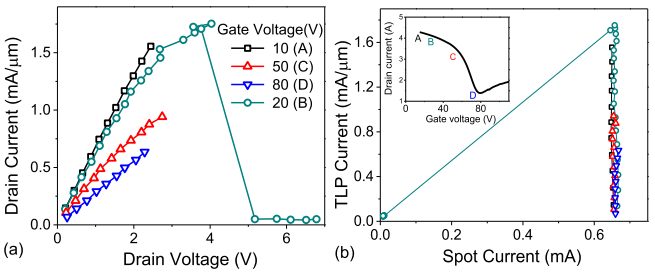

Fig. 3. (a) TLP 1–*V* characteristics of back-gated GFET in ambient condition at different gate voltages. Device was stressed till failure for back-gate voltage (V_{BG}) = *20* V, with voltage pulses of increasing amplitude, and duration of PW = 100 ns. The channel length of DUT is 1 μm. (b) Low bias (V_{SD} = 0.1 V and V_{BG} = 0 V) dc spot current measured after each pulse. Abrupt collapse in TLP current or dc spot current is a signature of failure. In case of abrupt failure, postfailure data points are not shown in subsequent figures for clarity. Inset: dc *I–V* characteristics of device under stress.

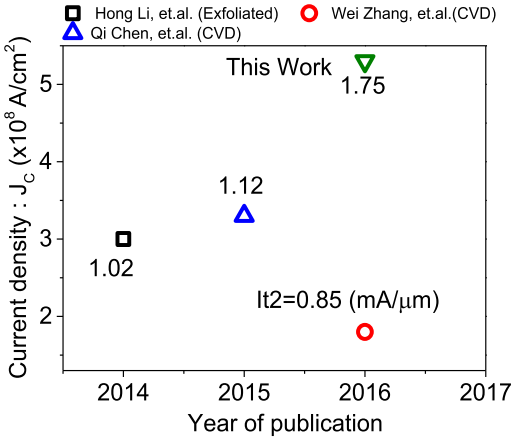

Fig. 4. Summary of failure current density, under ESD condition, reported till date. Failure current (mA/μm) normalized to a monolayer is listed next to respective data point.

and highlights corresponding gate voltages used during TLP measurement. It is worth highlighting that the gate voltages are chosen to cover all the key operating regions. Change in the TLP current in Fig. 3(a), for different gate voltages at a constant drain bias, shows the strong sensitivity of graphene channel carrier concentration to the gate voltage and also confirms transistor action. It is also observed that none of the characteristics in Fig. 3(a) have shown saturation in the drain current. The physics of current saturation and its implication on device failure under ESD conditions is discussed in Section IV in detail. Devices under back-gate voltage (V_{BG}) of 20 V are stressed till failure. Pulse current was found to increase linearly with stress voltage until device experiences failure. At the onset of device failure, a collapse in drain current can be seen. At the failure point, high field across the source–drain region causes inelastic scattering of carriers with substrate's surface optical phonons. The excessive Joule heating in graphene channel increases its lattice temperature till the oxidation temperature of carbon in graphene lattice. Subsequently, oxidation of carbon takes place, which forms an open between the source and drain regions. Similar failure signature is also evident from low-bias dc spot current data in Fig. 3(b), which shows an abrupt collapse in the measured dc spot current. Beside onset of device failure and gradual channel damage, low-bias dc spot current data are extracted to also track stress induced nonreversible device degradation, which are missing in earlier works [12], [13]. Post TLP pulse spot dc measurement is performed at a drain bias of 0.1 V and back-gate bias of 0 V.

Fig. 4 depicts the failure current density achieved in this paper along with the failure current densities reported in the literature under 100-ns TLP pulse stress condition. The reported literature used both epitaxial and CVD grown graphene. Fig. 4 also highlights the failure current values scaled to monolayer thick graphene. The obtained improvement in ESD robustness is attributed to the high-performance graphene transistors [15] used in this paper for ESD investigations. The details of the technology development and insights into the contact engineering for record high channel performance can be found in our earlier work [15].

IV. Carrier Transport and Related Failure Under ESD Conditions

The electrothermal carrier transport in 2-D material transistor is significantly different from that of bulk silicon technologies. Though the transport under low-bias condition is widely studied and well understood in the literature, the high-field and high-current effects under ESD like conditions in graphene technology are not very well understood. The electrothermal carrier transport during ESD event is investigated using back-gated GFET design without dielectric capping [Fig. 1(b)], which is extended eventually to top-gated architectures while using a step-by-step approach. First, graphene channel is encapsulated with top dielectric and the deviations in device's ESD behavior are studied. Then, implications of top metal gate on heat transport in graphene channel and eventual failure are studied in the end.

A. Channel Length Scaling Versus Carrier Transport

To understand the carrier transport under ESD condition and its implication on the device failure, the experiments are designed with GFETs having varying channel length and width. Consequently, these devices were stressed for varying stress duration. Fig. 5 depicts the TLP *I–V* characteristics of back-gated graphene transistors with different channel lengths and on-the-fly low-bias dc spot current versus TLP stress current relation. At shorter channel lengths, drain current increases linearly with stress voltage until its failure. However, for longer channel lengths, early saturation in drain current before the onset of device failure can be observed. The early saturation in drain current, with increasing channel length, is attributed to shift from quasi-ballistic carrier transport in short-channel FETs to diffusive transport in long-channel devices. The current saturation at high source–drain fields in graphene transistor is attributed to substrate induced optical phonons. When carriers traverse from source-to-drain through graphene channel, they continuously gain energy due to the source–drain field and loses the same due to inelastic scattering with the substrate optical phonons. As the optical phonon

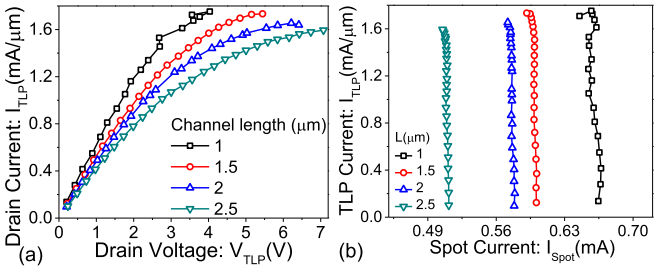

Fig. 5. (a) TLP *I–V* characteristics of back-gated GFET without dielectric capping for different channel lengths. With increase in channel length nature of carrier transport shifts from quasi-ballistic to diffusive, consequent of which reduction and saturation in current is observed. The important parameters are $V_{BG} = 20$ V and PW = 100 ns. (b) Spot measurement ($V_{spot} = 0.1$ V) does not show any change, corroborating the fact that length-dependent change in TLP *I–V* is indeed a transport behavior and not prefailure degradation.

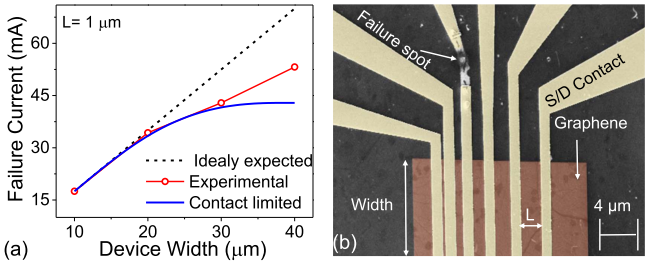

Fig. 6. (a) Failure current as a function of device width (W) depicted for three different cases. The experiments are conducted with $V_{BG} = 20$ V and PW = 100 ns. (b) False-color SEM image depicting the S/D contact failure due to electromigration of contact metal.

energy of intrinsic graphene is much higher (150–160 meV) than that of the polar SiO_2 substrate (54 meV), the substrate contributes to dominate in terms of the electron–phonon scattering during the high-field high-current stress by continuously populating the surface optical phonons. The inelastic carrier scattering in long channel (diffusive transport) devices lowers the carrier mobility and, hence, leads to carrier velocity saturation, which is visible in form of drain current saturation.

Compared to the diffusive channel, carriers in quasi-ballistic channel, which are relatively shorter channels, encounter relatively lesser scattering centers. This mitigates the electron–phonon scattering in the channel region by lowering the number of scattering centers. This results in a negligible carrier mobility degradation, unlike diffusive channel, which avoids carrier drift velocity to saturate before the failure point. The failure location was also found to be dependent on carrier transport. Higher scattering in the channel region in case of diffusive transport implies that carrier would lose most of its energy in the channel region. This results in higher channel temperature when compared to rest of the device active region, which leads to onset of physical failure at the center of graphene channel. However, for quasi-ballistic channel, failure takes place closer to the drain contact region. This is attributed to carrier energy relaxation via electron–phonon scattering next to the drain contact. Fig. 5 also depicts that early saturation in drain current lowers the failure current. The reduction in the dc spot current in Fig. 5(b) with increasing channel length is, however, attributed only to increase in channel resistance with channel length.

B. Width Scaling and Contact Limited Failure

In principle, the failure current must linearly scale with the device electrical width. To investigate this, GFETs with channel width up to 40 μm are realized and tested. Fig. 6(a) depicts the failure current (It2) as function of device width. Independent of whether the carrier transport is quasi-ballistic in nature or diffusive, failure current was found initially to scale linearly with device width (i.e., till W = 20 μm). However, at larger device width (>20 μm), the electromigration of the contact was found to dominate the intrinsic graphene failure, which leads to the absolute failure current to saturate at larger device width. It is worth highlighting that graphene is an atomically thin layer, whereas S/D metal pads used here were 100 nm thick, which emphasizes the extreme current carrying capability of graphene. Moreover, the obtained trends reveal the significance of S/D contact design for ESD robust graphene transistors as well as highlight the need for thicker S/D contacts to benefit from high current carrying capability of graphene. The false-color SEM image in Fig. 6(b) revels the failure spot in contact region, which as explained earlier is attributed to electromigration of drain contact metal, whereas the channel region was found to remain intact. To validate our argument, GFET with thicker (150 nm) S/D metal pads were realized and tested. Fig. 6(a) shows quasi-saturated failure current versus device width characteristics with thicker S/D contacts, which depicts failure current recovery when S/D contact was not the show stopper.

C. Ambipolar Transport

Fig. 7(a) depicts TLP *I–V* characteristics of back-gated GFET with different channel lengths, stressed using 25-ns wide pulses to probe the nature of electron transport without thermal effects. A kink in the *I–V* characteristics can be seen in under high-field condition where the current first saturates and then increases again, as depicted using an *I–V* cartoon in Fig. 7(c). Such an output characteristics of GFETs, first observed in [5], is attributed to ambipolar nature of the graphene channel. Under certain field condition, minority carriers are injected from the drain contact into channel region, which screens the source-to-drain field along the channel. This shifts the charge neutrality point (CNP) away from the drain contact as depicted using the schematic in Fig. 7(c). This leads to an increase in the drain current post drain current saturation with increasing drain field, as depicted in Fig. 7(a). Fig. 7(c) also explains the observed kink with the help of energy band diagram for graphene channel. It should be noted that the observed kink in this paper is not due to the applied ESD stress or stress duration; however, it is specific to initial channel doping and field conditions across the device. Ambipolar transport was also found to induce trapped charges in the gate oxide. This can be explained as the following: when CNP is inside the channel, high-field centered around CNP generates hot carriers, which are trapped in the gate oxide. These trapped

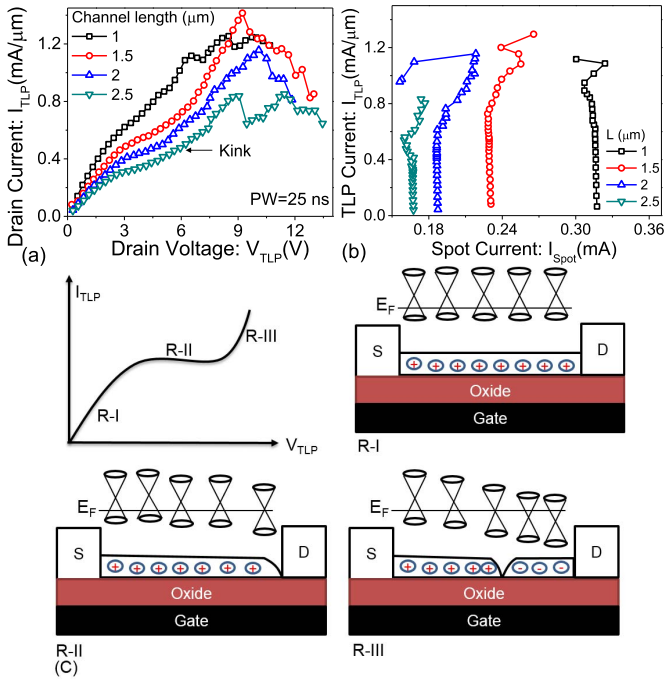

Fig. 7. (a) TLP characteristics of back-gated devices stressed using 25-ns TLP pulse at a back-gate voltage of $V_{BG} = 20$ V. (b) Increase in spot current measured after each pulse confirms shift in the Dirac point before device failure. (c) Energy band diagram along graphene channel at different regions of device operation during the stress.

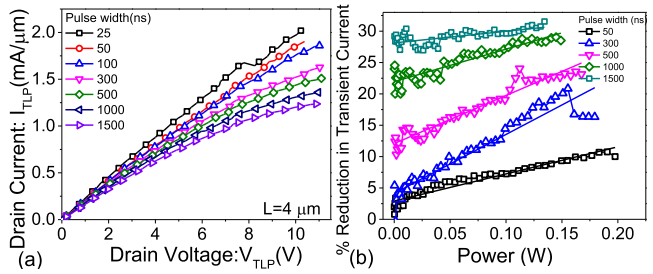

Fig. 8. (a) TLP *I–V* characteristics of GFET stressed using varying pulse widths ranging from 25 ns to 1.5 μs. All the devices have channel length of $L_{ch} = 4$ μm and $V_{BG} = 20$ V and device width of 20 μm. (b) Percentage reduction in transient drain current for varying pulse widths as a function of applied stress power.

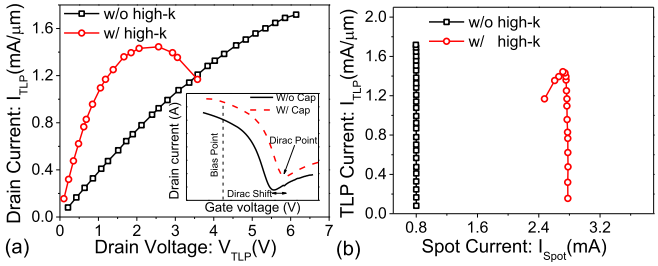

Fig. 9. (a) TLP *I–V* characteristics of back-gated GFET with and without dielectric cap. Early current saturation and failure in capped devices are due to higher self-heating. The inset of the figure depicts Dirac point shift. (b) Reduction in spot current with increasing I_{TLP}, which is depicted as a signature of gradual failure of capped device. Both the devices have channel length of 1 μm and stressed PW = 100 ns, $V_{BG} = 20$ V, thickness of high-k oxide on top of the graphene channel is 15 nm.

carriers result in shifting of the Dirac point, which is evident from shift in low-bias spot measured dc current at higher ESD stress, as depicted in Fig 7(b). The CNP induced hot carrier trapping–detrapping and associated Dirac point shift also causes instability in the device's pulse characteristics under higher field conditions before the catastrophic failure of the device.

Pulse *I–V* characteristics using increasing pulse duration gives insights into the electrothermal transport and its implications on the failure thresholds. Fig. 8(a) depicts TLP *I–V* characteristics of back-gated GFET, stressed using pulses with duration from 25 ns to 1.5 μs. At low pulsewidth, the drain current continue to increase linearly with source–drain field; however, with increasing pulsewidth, current begins to saturate at higher source–drain electric field. Moreover, the onset source–drain field for current saturation, shift to lower drain voltage with increasing pulsewidth. The saturation in drain current, with increasing pulsewidth, is attributed to channel self-heating, which is due to carrier scattering with the substrate induced optical phonons. This is also evident from percentage reduction in transient drain current with pulse time and applied power, as depicted in Fig. 8(b).

V. Implications of High-k Dielectric Capping

So far, the back-gated graphene transistor architectures were used to understand the fundamental carrier transport in graphene, under ESD conditions. This section extends the ESD investigations to dielectric capped (encapsulated) back-gated GFETs by keeping the graphene technology evolution in mind.

A. Carrier Transport With High-k Dielectric Cap

Fig. 9 depicts the TLP *I–V* characteristics of back-gated GFETs with and without high-k dielectric capping [see Fig. 1(c)]. Aluminum oxide (Al_2O_3) is being used to isolate the graphene channel from the ambient. The difference in low-bias resistance of these transistors is attributed to the difference in gate-induced channel carrier concentration, which is due to a difference in their respective Dirac voltages. Note that the back gate of both the transistors is connected to the same potential ($V_{BG} = 20$ V) during TLP stress, to ensure the same vertical field. The inset of Fig. 9(a) shows Dirac point shift in dielectric capped device, which increased gate induced conduction in graphene channel for a given gate voltage. The difference in Dirac point for both the device configurations is also evident from low-bias dc spot current data shown in Fig. 9(a), where the device with dielectric capping contributes to higher channel current for the same gate voltage. Furthermore, under high fields Fig. 9(a), a comparison of both the architectures shows that the GFET without dielectric capping offers negligible current saturation before the onset of device failure. However, the device with dielectric capping fails relatively at lower current and lower power with early drain current saturation. Dielectric capping in graphene transistor results in an enhanced carrier scattering, which in turn lowers the carrier velocity and leads to drain current saturation. It is observed that the carrier transport is no longer quasi-ballistic with dielectric capping,

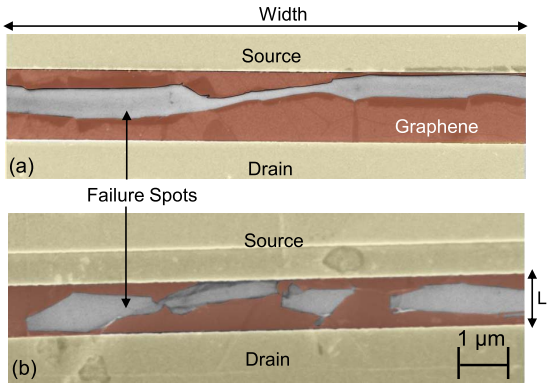

Fig. 10. False-color SEM image of GFET. (a) Without dielectric cap. (b) With dielectric cap.

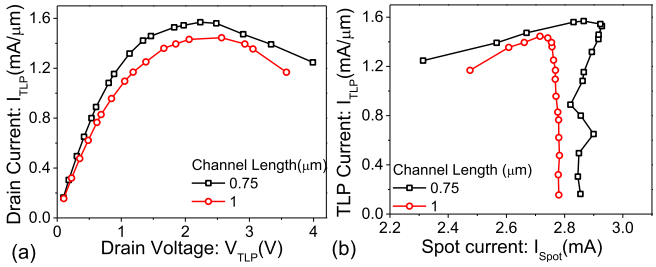

Fig. 11. TLP I–V characteristics of dielectric capped GFET for different channel lengths. Devices are stressed with PW = 100 ns and V_{BG} = 20 V. Thickness of high-k oxide is 15 nm.

even at the same channel length when compared to device without dielectric passivation. Beyond the current saturation, a negative differential conductance (NDC) region is observed, before drain current collapse for dielectric capped device. The observed NDC is not intrinsic to graphene. The NDC in capped devices is attributed to the unique gradual failure mechanism in GFETs, where the graphene channel is not exposed to the ambient. Contrary to abrupt/hard failure of GFETs in ambient, a gradual fall in drain current (both pulse and dc spot current) is observed in case of dielectric-capped GFETs. The localized heating in graphene with high-k encapsulation implies that a portion of the carbon atoms gets oxidized first the physical failure gradually spreads along the width in consequent pulses. In dielectric capped devices, the gradual failure or burning of carbon lattice along the width is attributed to the reduced degree of freedom for the carbon atoms to get oxidized. The false-color SEM images as depicted in Fig. 10 confirm the same. In Fig. 10(a), a continuous failure spot is observed in GFET without high-k dielectric cap. The same, however, in the case of dielectric capped devices was found to be distributed along the width in form of small patches. Finally, Fig. 11 depicts an upward shift in saturated drain current when channel length was scaled; however, the saturation behavior and failure trend remains the same. This confirms that the trends discussed earlier for dielectric capped devices are universal and independent of nature of carrier transport, i.e., channel length.

B. Transient Behavior

The failure analysis and novel gradual failure mechanism presented from the quasi-static data can be understood

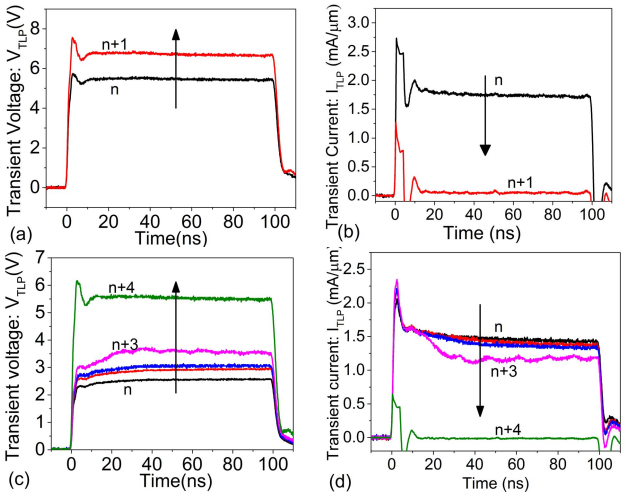

Fig. 12. Transient analysis of back-gated GFET (a) and (b) without dielectric cap, (c) and (d) with dielectric cap (15-nm-thick Al_2O_3) at the onset of failure. Both the devices are of 1 μm long, biased at V_{BG} = 20 V. Direction of arrow indicates (a and c) increase in pulse voltage amplitude and (b and d) subsequent collapse in drain current with increasing ESD stress amplitude, in steps.

systematically from the on-the-fly captured transient current and voltage waveforms, as depicted in Fig. 12 at the onset of device failure. With increasing ESD stress drain current collapses abruptly at the onset of failure from pulse n to $n + 1$ in device without dielectric passivation. The same, however, collapses gradually in devices with dielectric passivation, as it required four subsequent stress pulses to result in complete failure. Fig. 13, while using an atomistic representation, summarizes various transport dependent ESD failure locations and mechanisms in GFET. In GFET without high-k dielectric encapsulation [Fig. 13(a) and (b)], for a diffusive graphene channel, the failure was found to be at the center of the graphene channel, however, if the transport is quasi-ballistic in nature, mobile carriers lose their energy next to the contacts leading to graphene failure at the edge of drain contact. In device with dielectric capping [Fig. 13 (c) and (d)], the mode of carrier transport is always diffusive due to additional boundary scattering. In this case, the failure in the channel region spreads along the device width in smaller patches with increasing pulse stress.

VI. High-k Metal Gate Graphene FETs

ESD investigations are further extended to high-k metal gate architectures. Experiments designed include various top-gate configurations with gate-to-source underlap and gate-to-source overlap, together with different top-gate biasing schemes.

A. Top Gate: Underlap Versus Overlap

Fig. 14 compares the TLP I–V characteristics of various top-gated graphene transistors with back-gated FET with high-k dielectric cap. An underlap/overlap of 150 nm, of the top-gate metal with source and drain regions, is intentionally introduced. Top-gate electrode is grounded and bottom gate is connected to 20-V source during the TLP investigations.

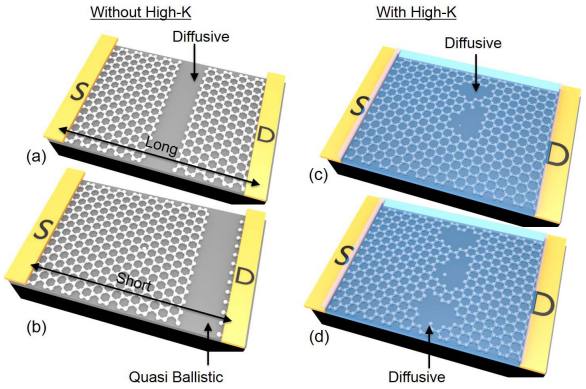

Fig. 13. Atomistic view of device failure. (a) Back-gated GFET without dielectric cap with diffusive channel. (b) Back-gated GFET without dielectric cap with quasi-ballistic transport. (c) Back-gated GFET with dielectric cap at first failure. (d) Back-gated GFET with dielectric cap after eventual failure. Cyan color: ALD Al_2O_3.

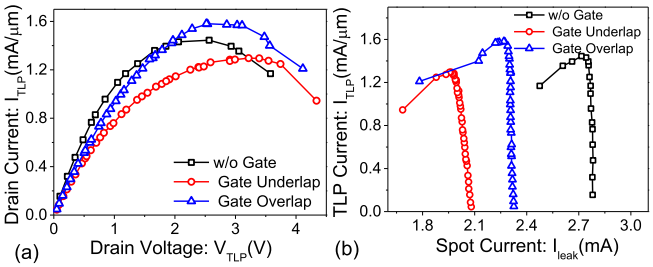

Fig. 14. (a) TLP *I–V* characteristics of GFET compared for devices with: 1) top gate to S/D underlap; 2) top gate to S/D overlap; and 3) without top gate. In all cases, the top gate is grounded and $V_{BG} = 20$ V, PW = 100 ns, and $L_{ch} = 1$ μm and top-gate oxide thickness is 1- nm Al_2O_3. (b) Spot measured ($V_{Spot} = 0.1$ V) dc current after each stress pulse, plotted as a function of stress current.

For a given gate field condition, the difference in low-field resistance for the three configurations investigated is due to difference in respective channel carrier concentrations which is due to their respective gate placements. Moreover, the device conducting higher current was found to offer higher failure current without any observable difference in failure voltage. This is interesting because the power to fail here is found to be an increasing function of channel conductivity. The improved ESD robustness of top-gated device can also be partially attributed to additional heat removal from the graphene channel through the top metal gate. This can be noticed from higher failure current of gate overlap device in which the gate metal completely encapsulates the hot spot, unlike the underlap device. On the other hand, in GFET without top gate and with a high-k dielectric cap, severe self-heating occurs attributed to the substrate optical phonons and additional thermal resistance from the dielectric capping. The same is mitigated when a metal gate is placed on top of the channel region, which also acts as an efficient nanoheat sink and cools down the graphene channel through the ultrathin high-k dielectric. This behavior is also evident from the right shifted (delayed) drain voltage required for drain current saturation, for the overlapped top-gated device. On the other hand, the device with gate

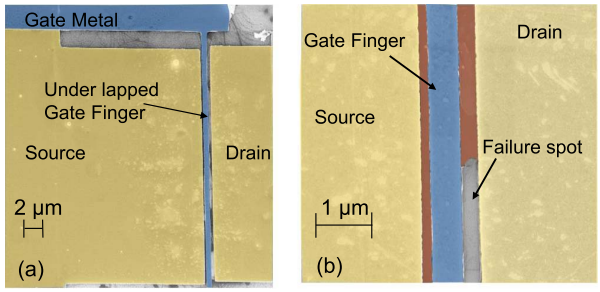

Fig. 15. False color (postfailure) SEM image of (a) under lapped high-k metal gate graphene transistor and (b) zoomed-in view at of the failure spot.

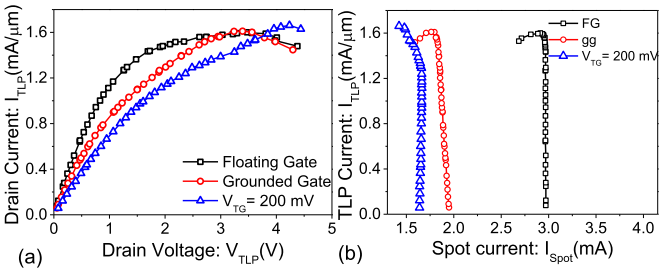

Fig. 16. TLP *I–V* characteristics of top-gated GFET under different gate biasing schemes. For these investigations, $V_{BG} = 20$ V, PW = 100 ns, and $L_{ch} = 1$ μm and top-gate oxide thickness is 15-nm Al_2O_3. (b) Change in dc spot current with increasing pulse current confirms shift in Dirac point due to carrier trapping in the top-gate dielectric.

underlap failed at lower current with early drain current saturation.

False-color SEM image of underlap GFET device, as depicted in Fig. 15, reveals graphene failure between the gate and drain edge, which confirms dominance of self-heating and localized hotspot formation in the region where the gate metal was missing. It should be noted that graphene in the source side underlap region, as depicted in Fig. 15(b), was found to be intact, which further validates presence of hotspot only near the drain contact.

B. Top-Gate Electrostatics and Related ESD Behavior

Various top-gate biasing configurations are explored, to study the impact of the top-gate field on carrier transport and GFET's ESD behavior. Fig. 16 depicts that the TLP *I–V* characteristics of top-gated graphene transistor, with top-gate biased at different voltages (grounded gate, a positive bias of 200 mv and floating gate conditions). Difference in the low field on resistance is attributed to the difference in operating point with respect to top- gate. Under floating gate condition, gate-to-drain capacitance dynamically charges the top gate, which increases the gate field with increasing drain voltage. This contributes to faster carrier velocity saturation, which leads to an early drain current saturation when compared to the other two configurations. When the top gate is biased at a fixed dc voltage, drain current is found to increase beyond saturation. Fig. 16(b) shows that, in all the three configurations, hot carrier trapping was found to be present as evident from negative shift in dc spot current data at

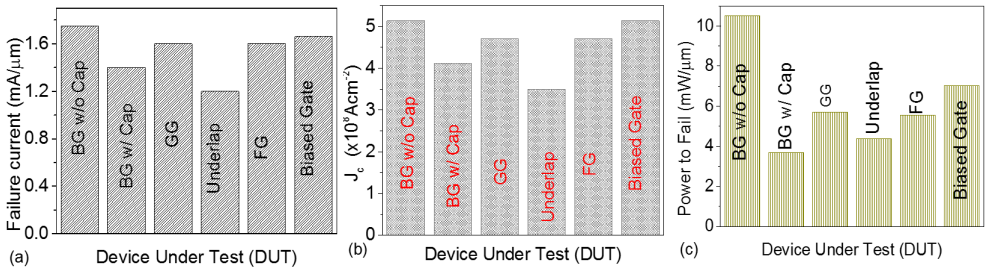

Fig. 17. Comparison of (a) failure current, (b) maximum current density, and (c) power to fail for various device architectures and biasing schemes investigated in this paper. Here, back gate with cap and back gate without cap are back-gate GFET with and without dielectric cap, respectively. GG is the grounded top-gate architecture, FG is floating top gate and biased gate is the top-gate device biased at 200 mV.

higher pulse currents. Fig. 17 summarizes the failure current, maximum current density, and power-to-failure of all architectures and device configurations investigated in this paper. Back-gated GFET without dielectric cap was found to have highest ESD robustness. The high-k dielectric capped devices were shown to have the least ESD robustness, attributed to the diffusive transport due to additional boundary scattering. However, top-gate architecture with overlapped gate was found to improve the ESD robustness, thanks to the metal gate over high-k dielectric which helps to mitigate the self-heating by taking the thermal energy away from the graphene channel.

VII. Conclusion

Saturation in drain current just before failure, with increasing channel length, was observed, which was found to be due to shift from quasi-ballistic transport in short channel FETs to diffusive transport in long channel devices. Failure current, however, was found more or less insensitive to channel length, depicting intrinsic failure limit of channel material, which is independent of channel capability. Moreover, it was found that GFETs with shorter channel having quasi-ballistic transport fail due to thermal-assisted breakdown of graphene near drain contact, while diffusive channel FETs experience excessive heating at the middle of graphene channel. It was observed that the devices stressed using shorter pulses (<25 ns) survive higher stress voltage, however, higher drain field leads to device degradation attributed to hot carrier trapping in gate dielectric. Beside higher failure voltages, increased channel current was observed for shorter pulses, which is attributed to the mitigated self-heating or absence of carrier scattering with substrate optical phonons. Shorter pulse investigation pulsewidth was kept much shorter than thermal diffusion time, also helps to reveal the upper/intrinsic limit of channel conduction. Furthermore, this paper reveals that devices without dielectric capping fail abruptly, whereas devices with dielectric capping or top-gate-stack fail gradually with increasing stress amplitude. Interestingly, power to fail was found to be lower for devices with dielectric capping, as the dielectric capping introduce additional interface scattering, which causes localized heating. Finally, top-gated devices were found to have better ESD robustness when compared to devices only with dielectric capping, due to efficient heat removal from the graphene channel through the metal gate. The detailed physical insight and high-performance GFET technology have enabled record high failure current.

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