Unique ESD Behavior and Failure Modes of AlGaN/GaN HEMTs

Bhawani Shankar, Mayank Shrivastava
Advance Nanoelectronic Device and Circuit Research Laboratory, Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore 560012, India, email: mayank@dese.iisc.ernet.in

***Abstract*— Present experimental study reports various failure modes under ESD stress conditions and distinct ESD behavior of AlGaN/GaN HEMTs for the first time. Effect of MESA isolation and gate finger on the ESD behavior of HEMTs is analyzed. Effect of pulse width on ESD robustness and snapback voltage is observed and a unique power law like behavior is found. Cumulative nature of device degradation under ESD stress condition is discovered. Correlation between depth of snapback and failure threshold with % device degradation is found. Finally, impact of inverse piezoelectric effect in AlGaN/GaN system, fringing electric field, role of contact resistivity, temperature and field induced contact metal migration and premature breakdown of parasitic MESA Schottky junction are studied in context to AlGaN/GaN HEMT failure ESD conditions.**

***Index Terms*-- Electrostatic Discharge (ESD), Failure Modes, Gallium Nitride (GaN), High Electron Mobility Transistor (HEMT), Power Law.**

I. Introduction

Gallium Nitride on Si based High Electron Mobility Transistor (HEMT) has attracted great attention in recent years as potential alternative of Si power and RF devices. Thanks to its wide bandgap (3.4eV), high breakdown field (3.3MV/cm) and realization of AlGaN/GaN hetero-junction over Si substrate with high 2DEG density (10^{13} cm^{-2}), high electron peak velocity (2.5×10^{7}cm/s) and high electron saturation velocity (1.5×10^{7}cm/s). Long term reliability, attributed to inverse piezoelectric effect and hot carrier trapping, which is typically accelerated under high electric field conditions, has been greatly studied for GaN HEMT devices. However, discussion on ESD reliability of these devices is very limited in the literature [1-6]. For example, snapback behaviour was shown in [1]; however with limited explanation while using model and failure physics for GaAs HEMT system [7]. Lee et. al. reported an increase in device current under ESD condition due to shorting from drain to source [2]. Field and power dependence of failure mechanism in GaN HEMT was highlighted in [3]. The other works [4] – [6] focused on the ESD behavior of the gate–to–S/D Schottky diode.

II. Devices under ESD Stress

AlGaN/GaN HEMTs stack (Fig. 1a) was grown over a 2" Si (111) wafer using MOCVD. 100μm wide, normally – ON devices (i) w/ and w/o gate metal, (ii) w/ and w/o MESA isolation were processed using UV lithography. MESA isolation was processed using Chlorine based ICP-RIE. Ti/Al/Ni/Au metal stack was deposited using E-beam evaporation, which was later annealed at high temperature (~850 ºC) to form ohmic contacts. Ni/Au based Schottky gate was deposited at the last followed by a low temperature anneal stage (Fig. 1b). Surface passivation was ignored in this lot. Transmission Line Pulsing (TLP) method with varying pulse width (PW) and fixed rise time (1ns) was used to investigate ESD behavior of HEMT devices. After each pulse, linear drain current (I_{DS}) was measured at low drain bias (V_{DS} = 50mV), to monitor device degradation and failure.

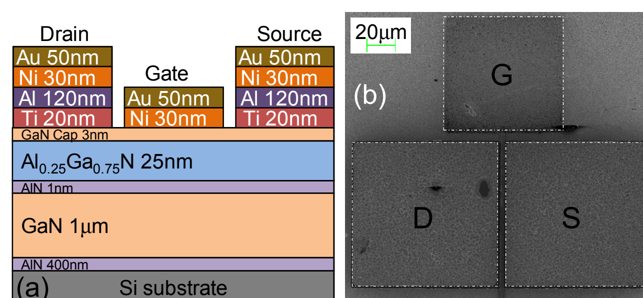


Figure 1: (a) Cross-sectional view of AlGaN/GaN HEMT with layer stack; and (b) SEM micrograph of the top view depicting gate finger between Source and Drain. Devices under stress are HEMTs w/ & w/o gate, w/ & w/o MESA and floating gate devices with different source-to-drain spacing (L_{SD}).

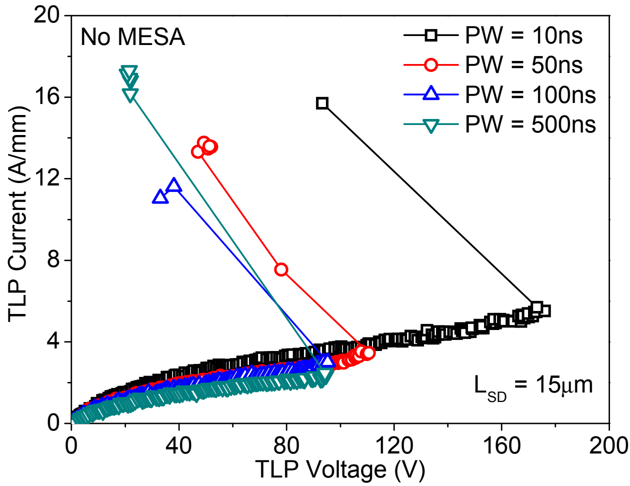
III. TLP Characterization and Results

Fabricated HEMT devices were characterized under various configurations (Fig. 2 – 7). Investigation of HEMT devices (a) without gate finger and MESA isolation, (b) without gate finger and with MESA isolation, (c) with gate under floating condition and (d) with gate grounded condition, stressed while varying (i) pulse widths and (ii) source to drain spacing reveals similar TLP characteristics. Attributed to the normally – ON nature of realized HEMTs, devices exhibit a linear TLP current vs. TLP voltage characteristics. At high voltages, close to avalanche breakdown, devices exhibit unique snapback characteristic. In most of the cases a holding state, post snapback, is missing, i.e. device fails after few pulses in the snapback state. However, very rarely a holding state after snapback was also observed. Degradation in linear drain current, which was measured after each stress pulse, can be noticed from the spot measurements (discussed in later section). Finally, following observations can also be drawn from the TLP measurements: (i) lowering of snapback voltage (V_{SNAP}) and increased R_{ON} at higher pulse widths, which is attributed to enhanced self heating at higher pulse widths and (ii) V_{SNAP} increases with increasing source to drain spacing (Fig. 2 – 7), which is attributed to the reduced channel electric field.

This work was financially supported by Department of Electronics and Information Technology (DeitY), Govt. of India under National Mission on Power Electronic Technology (NaMPET), through project no. NaMPET-Ph-II/SP13/Ex05

978-1-4673-9137-5/16/$31.00 ©2016 IEEE

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on November 25,2022 at 10:05:17 UTC from IEEE Xplore. Restrictions apply.



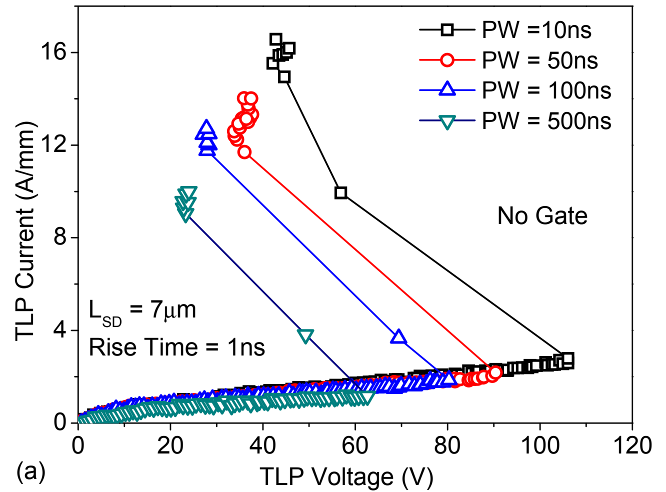


Figure 2: TLP characteristics of 50µm wide HEMTs without gate and MESA isolation with varying pulse width (PW). V_{SNAP} decreases and R_{ON} increases with increase in PW due to increased self heating in device.

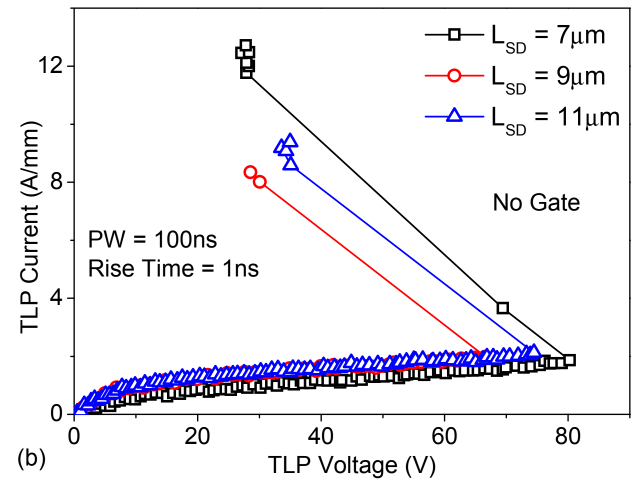


Figure 3: TLP characteristics of 100µm wide HEMTs without gate with varying (a) pulse width and (b) L_{SD}. Figure shows (a) decrease in V_{SNAP} and increase in R_{ON} with increase in PW due to increased device self heating & (b) improvement in V_{SNAP} with increase in L_{SD} at fixed PW = 100ns. Note: Device with L_{SD} = 7µm shows highest V_{SNAP} owing to its lowest On-current, attributed to device–to–device variability across wafer.

IV. Power Law Characteristics

The power required to trigger the device into the snapback state is observed to decrease with increase in pulse width, exhibiting a power law like characteristics in all measured configurations (Fig. 8a). This can be attributed to either increased self heating with higher pulse widths or increased device degradation with increasing pulse width, or both. Furthermore, increase in source-to-drain distance (L_{SD}) improves power-to-trigger (Fig. 8b). This is attributed to reduced current density and electric field with increased L_{SD}, which eventually reduces power density (J.E) and therefore requires higher power to trigger snapback. These trends signify role of power density and self heating in triggering the snapback. Finally failure current falls with increase in pulse width, exhibiting a power law behavior under all measured configurations (Fig. 8c). Moreover, the power-to-failure for AlGaN/GaN HEMTs is small compared to that for Si devices. This is because ESD failure in Si based devices occurs either by parasitic BJT triggering (DeMOS) or thermal filament formation (ggNMOS). However, in present study, AlGaN/GaN HEMT failure, apart from filamentation in buffer, is observed to occur due to metal migration and inverse piezoelectric effect due to which HEMTs fail at low power in snapback region itself. Moreover the presence of various material layers in AlGaN/GaN HEMTs leads to phonon scattering at different interfaces resulting in high interface thermal resistance. This enhances device self heating and causes failure of AlGaN/GaN HEMTs at lower power compared to that in Si devices.

V. Drain Current Degradation and Correlation with ESD Fail

Linear drain-to-source current (I_{DS}) was found to be an important parameter for monitoring the health of HEMTs under ESD conditions. A unique device degradation trend with increasing stress level can be noticed (Fig. 5c). It was found that I_{DS} degrades by 15 – 20 % before snapback, however it increases on verge of snapback. Moreover, when

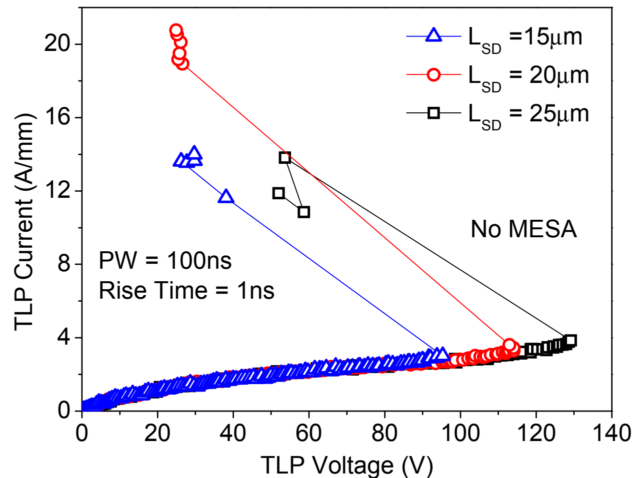
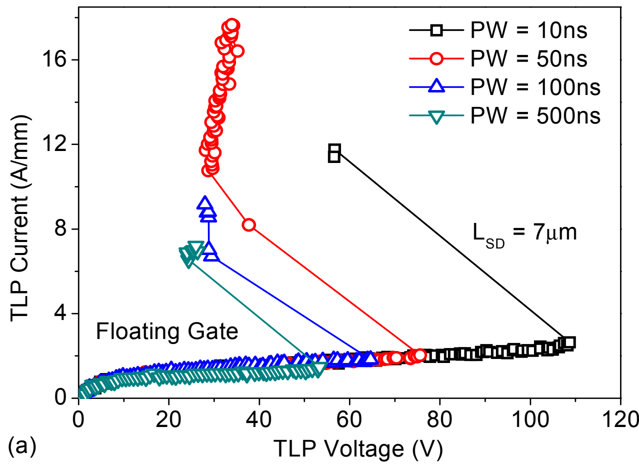
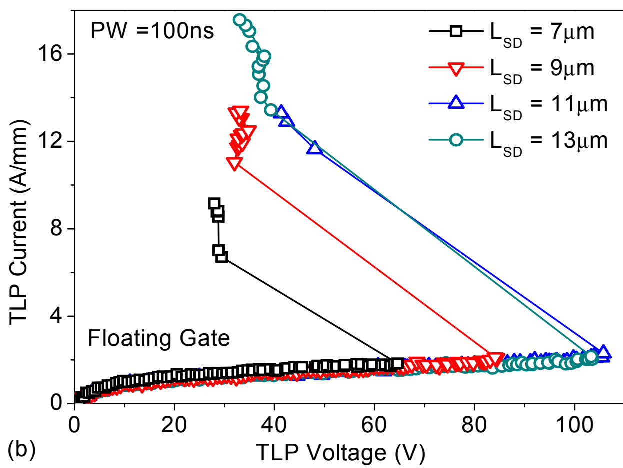


Figure 4: TLP characteristics of 50µm wide HEMTs without gate and MESA isolation with varying L_{SD}. V_{SNAP} increases with L_{SD}.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on November 25,2022 at 10:05:17 UTC from IEEE Xplore. Restrictions apply.





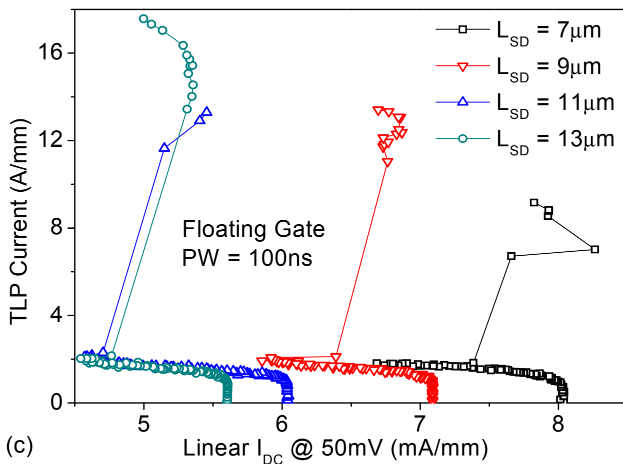


Figure 5: TLP characteristics of 100µm wide HEMTs with gate floating with varying (a) pulse width and (b) L_{SD}. Figure shows (i) decrease in V_{SNAP} and increase in R_{ON} with increase in pulse width due to higher self heating; (ii) increase in V_{SNAP} and I_{FAIL} with L_{SD} (c) leakage (here linear drain current) / spot measurements depicting (i) device failure point and (ii) device degradation after every stress pulse.

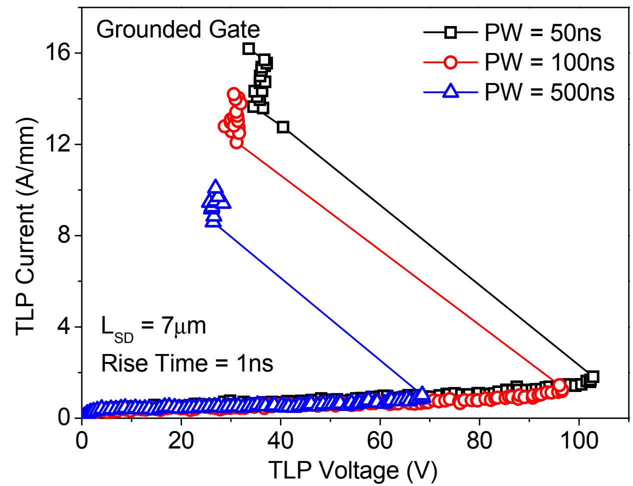


Figure 6: TLP characteristics of 100µm wide HEMTs with varying PW under grounded gate configuration.

device survives the snapback, I_{DS} degrades further with increase in TLP current (Fig. 5c).

Systematic and repeated measurements were performed to gain further insight into the nature of device degradation and its relation with ESD failure. A HEMT device was stressed with 10 consecutive pulses of fixed amplitude and pulse amplitude was increased subsequently. After each pulse linear drain current (I_{DS}) was measured. Systematic degradation in I_{DS} with increase in the number of stress pulse of given amplitude can be noticed (Fig. 9a and 9b). This depicts cumulative nature of the device degradation. A correlation between the snapback depth ($\Delta V = V_{SNAP} - V_{FAIL}$) and the % device degradation can be noticed (Fig. 9c), which reveals role of device degradation in voltage snapback and device failure.

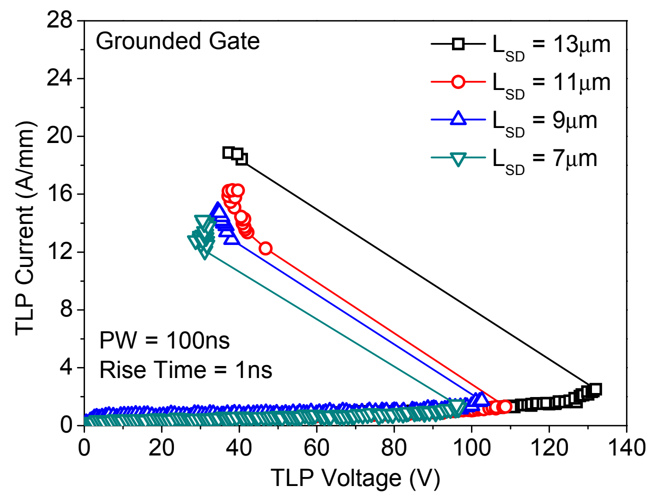


Figure 7: TLP characteristics of 100µm wide HEMTs with different L_{SD} under grounded gate configuration. Note that V_{SNAP} and failure current (I_{T2}) increase with L_{SD}.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on November 25,2022 at 10:05:17 UTC from IEEE Xplore. Restrictions apply.

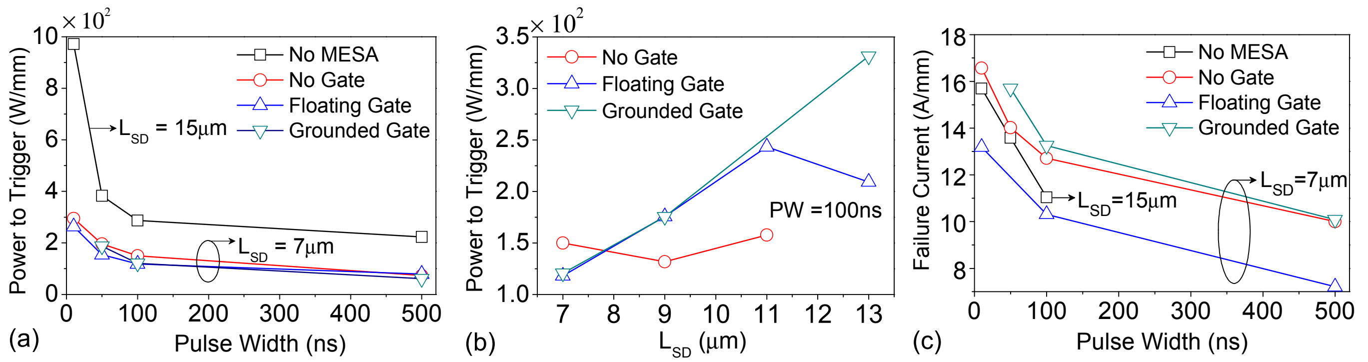


Figure 8: Device triggering behavior (Power-to-trigger and failure current) of the HEMTs stressed under different configurations. (a) Power to Trigger decreases with increase in pulse width obeying power law like characteristics in all the stress configurations; (b) Power-to-Trigger increases with increased source-drain spacing; (c) Failure current decreases with increase in pulse width depicting a power law like characteristics in all the stress configurations.

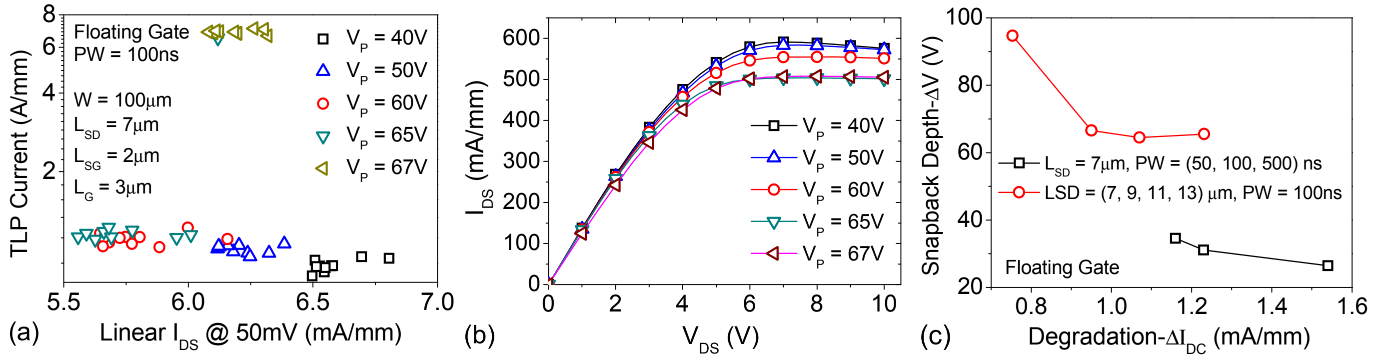


Figure 9: (a) Linear drain current (I_{DS}) measured after each pulse while stressing the device with 10 consecutive pulses of fixed amplitude and increasing the pulse amplitude (V_P) after 10 stress pulses. I_{DS} decreases with increase in number of stress pulse of a given amplitude. This depicts cumulative nature of the device degradation. (b) I_{DS} - V_{DS} characteristic measured after every 10 pulses of fixed amplitude depicting device degradation. (c) Relation between the snapback depth ($\Delta V = V_{SNAP} - V_{FAIL}$) and the extent of device degradation.

VI. Unique Modes of Device Failure

Distinct ESD failure modes were observed in HEMT devices with a dependence on device geometries and ESD stress conditions (Fig. 10-11). Devices without gate metal and MESA isolation are observed to fail due to migration of S/D metal from drain to source. Metal migration is very prominent at the contact corners where the field crowding is highest. At very high ESD currents, the lattice temperature across HEMT S/D contact pads is expected to be extremely high, which can melt the S/D metal(s). (Note: GaN melting temperature is 1.5× to 4× of S/D metals). Under the influence of fringing electric field, the molten metal flows from drain to source following curved path and creates an electrical short leading to device failure (Fig. 10a). MESA isolated HEMT w/o gate metal fails too due to metal migration induced source-to-drain short; however, the short path, unlike w/o MESA isolation case, typically forms along the channel (Fig. 10b). In this study, since devices were not passivated, metal migration got enhanced in presence of surface states which provide low energy path for metal diffusion. Presence of passivation would quench the surface states and reduce migration however; it will also induce stress in the AlGaN/GaN system therefore, the failure threshold of GaN HEMTs will be altered.

Devices stressed under grounded gate using very fast TLP (PW<10ns), which do not experience snapback, lead to multiple damages along the gate finger edge towards the drain. This can be explained as follows. Due to absence of snapback, these devices develop cracks underneath the gate finger, which is attributed to very high electric field induced inverse piezoelectric effect (Fig. 10c). The same under 100ns TLP stress experiences complete gate metal melting with massive crack running from drain to source (Fig. 11a). Premature breakdown of the parasitic Schottky diode between gate track and the MESA edge is also one of the root causes for ESD failure. In this case gate finger gets damaged due to melting of gate metal, which migrates to S/D pads and creates a short (Fig. 11b). Further insight into the failure physics can be gained through TCAD simulation of these devices. However, DC simulation of AlGaN/GaN HEMTs using commercially available TCAD tools itself is not trivial and still needs lots of work before their ESD behavior can be captured.

VII. Conclusion

The drain to source dc current was found to be a crucial parameter to monitor the device degradation under ESD stress. A correlation between % device degradation and snapback depth / failure threshold was discovered. Moreover, a cumulative device degradation behavior was revealed under ESD stress conditions. ESD failure current of GaN HEMTs was found to follow power law characteristics. Interestingly, a unique power law like behavior was observed for trigger

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on November 25,2022 at 10:05:17 UTC from IEEE Xplore. Restrictions apply.

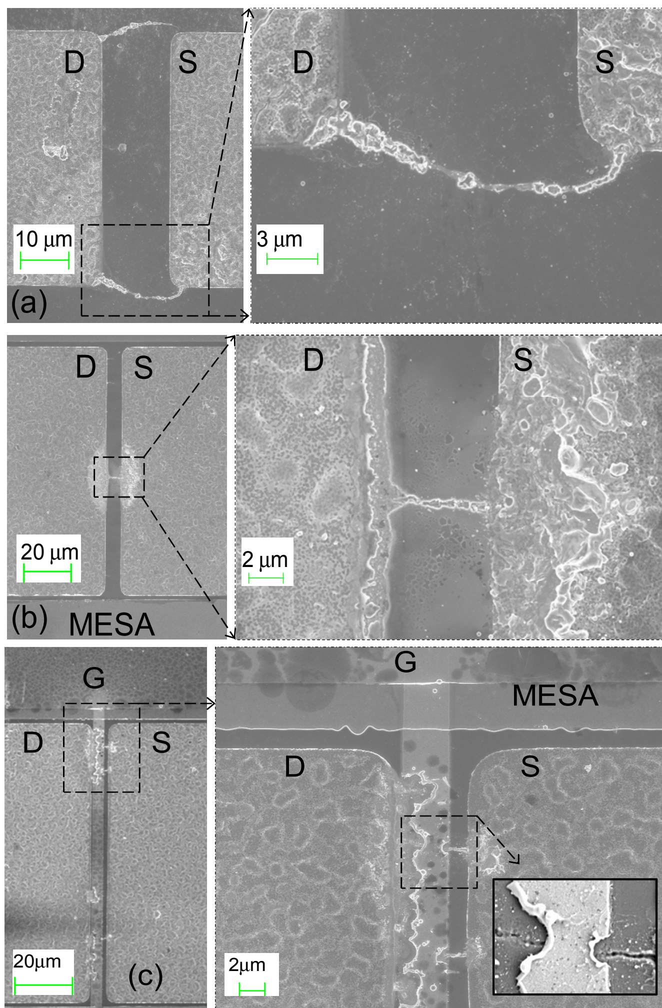


Figure 10: Post failure SEM images depicting different failure modes in HEMT devices. **(a)** HEMT without MESA and gate, failed after 50ns TLP stress. Figure shows the curved short paths between drain and source. EDX analysis of short portion confirms Ni (7.27%). SEM image reveals that Ni has melted from the edge of Ti/Al/Ni/Au stack of drain and migrated to source under the influence of fringing electric field. In all cases no short path was observed in the channel region. **(b)** MESA isolated HEMT with no gate, failed after 100ns TLP stress. Figure shows a short path between drain and source in the channel region. EDX analysis of short portion confirms Al (8.7%) and SEM image reveals that Al has melted from the edge of Ti/Al/Ni/Au stack of drain and has migrated and accumulated on source pad. **(c)** MESA isolated HEMT failed after 10ns grounded gate TLP stress. Figure shows damaged gate finger with crack underneath.

voltage as well. It was found that ESD robustness of HEMTs is also suffered due to premature breakdown of parasitic Schottky diode at MESA edge. Finally, this work highlighted that apart from filamentation in buffer, there are other factors like inverse piezoelectric effect, fringing field and Schottky junction at MESA edge, which can cause catastrophic failure of AlGaN/GaN HEMTs under ESD conditions. For example, it was found that ESD stress on non isolated HEMTs, while involving source – to – drain fringing field, causes metal migration along the edges of S/D contact pads. Similar migration also occurs in MESA isolated HEMT, however is confined to channel region.

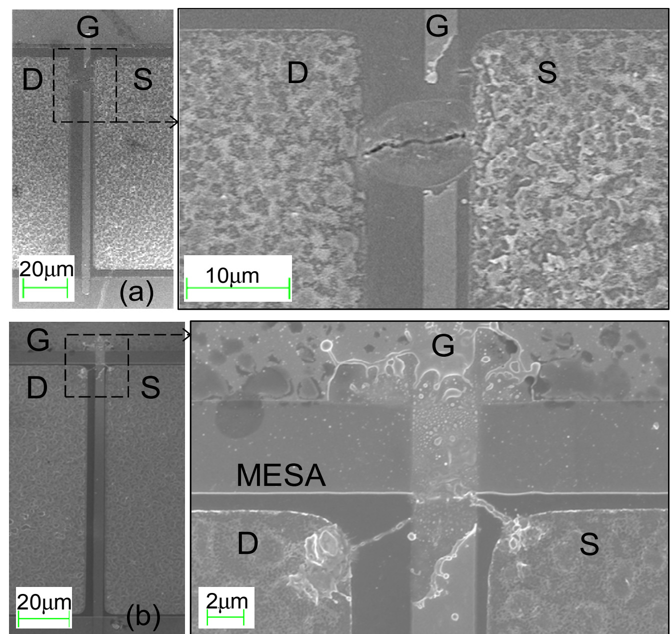


Figure 11: Post failure SEM images of **(a)** MESA isolated HEMT failed after 100ns grounded gate TLP stress. Figure shows a crack between drain and source with damaged gate finger. **(b)** MESA isolated HEMT failed after 100ns TLP stress between gate and drain (source floating). Figure shows HEMT fail occurs at the MESA edge with gate to S/D short and metal removal from the gate pad. EDX analysis of shorted path reveals Au (15.77%) which has possibly migrated from gate finger to source/drain pads creating gate to S/D short.

ACKNOWLEDGMENT

The authors would like to acknowledge Prof. Srinivasan Raghavan (CeNSE, IISc) for fruitful discussions on GaN material aspects. IISc GaN team is acknowledged for hardware/device processing support. Department of Electronics and Information Technology (DeitY), Govt. of India is acknowledged for financial support from the project no. NaMPET-Ph-II/SP13/Ex05, under National Mission on Power Electronic Technology (NaMPET).

REFERENCES

[1] J. Kuzmık, D. Pogány, E. Gornik, P. Javorka, and P. Kordoš, "Electrostatic discharge effects in AlGaN/GaN high-electron-mobility transistors," *Applied Physics Letters* 83, vol. 22, pp. 4655-4657, 2003.

[2] SC LEE, Jin-Cherl HER, Sang-Myeon HAN, Kwang-Seok SEO, and Min-Koo HAN, "Electrostatic discharge effects on AlGaN/GaN high electron mobility transistors on Sapphire substrates," *Japanese Journal of Applied Physics*, vol. 43(4B), pp. 1941–1943, 2004.

[3] Rossetto, I., Meneghini, M., Barbato, M., et al. "Demonstration of Field-and Power-Dependent ESD Failure in AlGaN/GaN RF HEMTs," *IEEE Tran. Electron Devices*, vol.62(9), pp. 2830-2836, 2015

[4] J. Kuzmik, D. Pogány, E. Gornik, P. Javorka, and P. Kordoš, "Electrical overstress in AlGaN/GaN HEMTs: study of degradation processes," *Solid-State Electronics*, vol. 48(2), pp.271-276, 2004.

[5] A.Tazzoli, F. Danesin, E. Zanoni, and G. Meneghesso, "ESD robustness of AlGaN/GaN HEMT devices," in Proc. 2007 *Electrical Overstress/Electrostatic Discharge Symposium*, pp. 4A1-4.

[6] S-H Chen, A. Griffoni, P. Srivastava, et al, "HBM ESD robustness of GaN-on-Si Schottky diodes," *IEEE Trans. Device and Materials Reliability*, vol. 12(4), pp.589-598, 2012.

[7] V.A. Vashchenko, and V.F. Sinkevitch, "Current Instability and Burnout of HEMT structures," *Solid State Electronics*, vol. 39(6), pp.851-856, 1996

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on November 25,2022 at 10:05:17 UTC from IEEE Xplore. Restrictions apply.