ESD Behavior of AlGaN/GaN Schottky Diodes

Bhawani Shankar, Sayak Dutta Gupta, Ankit Soni, Srinivasan Raghavan, and Mayank Shrivastava, *Senior Member, IEEE*

***Abstract*—This experimental study reports behavior of Ni/Au-based AlGaN/GaN Schottky diodes under ESD conditions. A comparative study of diodes with/without recessed Schottky contact unfolds different degradation physics in each case. The impact of different current conduction mechanisms, device degradation and trap generation on its robustness are analyzed. The role of interface traps under ESD failure of the GaN Schottky diode is investigated. The transition from soft-to-hard failure, which is found to depend on the presence of traps, and diode design is discussed. New insights into degradation trends, cumulative nature of degradation, and trap-assisted failure modes are discovered.**

***Index Terms*—Electrostatic discharge, gallium nitride (GaN), Schottky diode, trapping, failure modes.**

I. Introduction

RAPID emergence of Gallium Nitride (GaN) HEMT in the power electronics applications has tremendously increased the demand for GaN based diodes as well. This is due to the fact that the intrinsic body diode which offers reverse protection in Si MOSFET [1], is missing in AlGaN/GaN HEMT. Therefore, for a complete GaN based power electronic circuit design, GaN based diodes are required. Keeping this in mind, GaN Schottky diode has recently attracted attention for can be monolithically integrated with GaN HEMT [2]–[5]. Despite its high demand, while limited discussion on long term reliability of GaN Schottky diode is present in the literature [6], [7]; the same however, on its ESD reliability is missing. Moreover, with rapidly emerging GaN based power devices, there is an urgent need to realize ESD or short-circuit protection schemes for GaN technology. GaN Schottky diode can be used in antiparallel to the power switch to shunt the ESD or short-circuit current [8]. A combinition of it with HEMT can be used as ESD clamp for protection of I/O pads in RF amplifiers [9] and in electric vehicles [10]. Considering these applications, the study of ESD or short-circuit behaviour of GaN Schottky diode and its trigger mechanism are indispensable to design and realize robust ESD protection in GaN technology. With this as a motivation, this work reports ESD reliability of AlGaN/GaN Schottky diodes, which is an extension of our earlier work [11].

This manuscript is arranged as following: details of diode design, current conduction mechanisms, process details and devices under test are presented in Section II. Section III covers the details of device characterization under DC and ESD conditions along with ESD characterization set-up. The experimental observations are presented in Section IV. Failure mechanisms under different designs and test structures are discussed in Section V, whereas failure analysis presented in Section VI. Finally, this work has been summarized in Section VII.

Manuscript received April 2, 2019; revised May 4, 2019; accepted May 10, 2019. Date of publication May 14, 2019; date of current version June 5, 2019. This work was supported by the Department of Science and Technology (DST), Govt. of India, under Grant DST/TSG/AMT/2015/294. *(Corresponding author: Bhawani Shankar.)*

B. Shankar, S. D. Gupta, A. Soni, and M. Shrivastava are with the Advanced Nanoelectronics Device and Circuit Research Laboratory, Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: bhawani@iisc.ac.in).

S. Raghavan is with the Center for Nano Science and Engineering, Indian Institute of Science, Bengaluru 560012, India.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2019.2916846

II. GaN Diodes Under Test

Two types of AlGaN/GaN Schottky diode structure are studied in this work; (i) conventional diode with non-recessed Schottky contact and (ii) diode with recessed Schottky contact. In non-recessed structure, the Schottky contact directly sits on top of GaN cap, as depicted in Fig. 1(a), whereas in recessed structure, Schottky contact is placed over the GaN buffer, making sideways contact with 2DEG. This is shown in Fig. 1(b).

First, the representative diode structures are simulated using device TCAD, with and without recess to understand the current conduction mechanism in each case. Details of the TCAD setup and the used physical models are elaborated in our earlier work [12]. TCAD analysis in forward regime shows a significant difference in the way current flows in the two structures. In non-recessed diode conduction is primarily vertical where the entire anode area participates in carrier tunnelling as depicted in Fig. 1(a). Here presence of high current density underneath anode confirms area conduction in non-recessed diode. In recessed diode, current injection takes place from anode to 2DEG via anode side walls as depicted in Fig. 1(b). Keeping the conduction mechanism in mind, the recessed diode is optimized for following design parameters: (i) recess depth to maximize forward current, (ii) Schottky barrier height (SBH) to reduce cut-in voltage without compromising reverse leakage and (iii) anode-to-cathode spacing to maximize reverse breakdown voltage. The optimum test structures realized from TCAD simulation are realized using process explained below, which are used for ESD stress investigations.

For device fabrication, AlGaN/GaN material stack, as shown in Figure 1(c)-(d), is grown on a 2-inch Si (111) wafer using MOCVD. 150 nm thick AlN nucleation layer is grown on

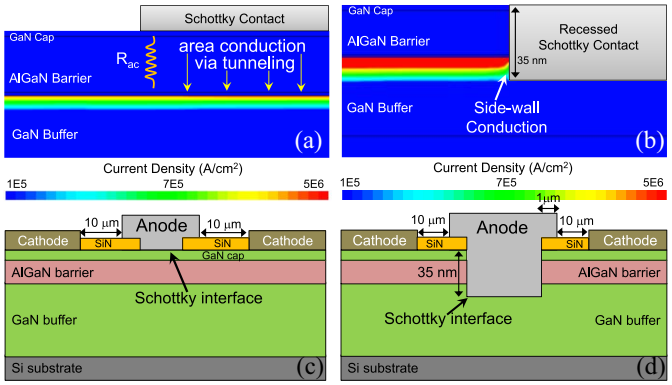

Fig. 1. (a) TCAD contours showing current density distribution in non-recessed diode and (b) recessed diode at 10V DC forward bias. Please note its a zoomed view of the region in anode vicinity. Schematic of AlGaN/GaN diodes under test (c) without recessed Schottky contact and (d) with recessed Schottky contact, depicting stack of various layers grown on Si.

Si substrate followed by 1 μm linearly graded AlGaN transition region. Then 650 nm GaN buffer layer is grown with unintentional background doping of $\sim 10^{15}$ cm^{-3}. 1 nm AlN spacer separates buffer from a 25 nm undoped $Al_{0.25}Ga_{0.75}N$ donor layer. Finally the stack is capped with a 3 nm GaN cap. 50 nm SiN is used for surface passivation. Structures are MESA isolated on wafer, by etching down to 180 nm GaN buffer using Cl_2/BCl_3 chemistry in Inductively Coupled Plasma-RIE system. Ti/Al/Ni/Au stack with 20/120/30/50 nm thickness respectively is deposited by e-beam evaporation, followed by a high temperature (850°C) anneal cycle to realize Ohmic contact to 2DEG. Ni/Au based Schottky (anode) contact is deposited, followed by a low temperature annealing in presence of forming gas. In non-recessed diode, the Schottky contact made on GaN cap offers lower surface roughness and improves Schottky barrier height [13]. In recessed structure, the GaN capping and AlGaN barrier layers are etched by O_2/BCl_3 based atomic layer etching (ALE) in a RIE system. Before anode metal deposition, appropriate organic and HF and HCl surface treatments are done to lower the surface roughness post ALE. Low surface roughness has following advantages; (i) It minimizes variation in SBH (Schottky Barrier Height) which improves uniform current injection across the barrier. (ii) Smaller interface roughness leads to lower interface defect density (D_{it}) which minimizes interface carrier scattering underneath Schottky contact. Diodes are fabricated with three different anode footprints (75 × 75, 150 × 150, 200 × 200 μm^2) and a fixed anode to cathode spacing (L_{AC}) of 10 μm.

III. Diode Characterization

A. DC Characterization

Before, conducting ESD investigations, it is worth evaluating the DC performance of pristine devices. The two types of diodes are DC characterized using Keithley 4200 semiconductor parameter analyser. The anode voltage is swept from −5 V to 2 V in steps of 0.1 V. The as recorded IV characteristics, for GaN Schottky diodes without/with recess, are shown in Fig. 2(a) and Fig. 2(b) respectively for different anode area. It reveals the following; (i) Lower cut-in voltage (V_{CUT-IN}) in recessed diode compared to non-recessed diode. This is due to; (a) absence of vertical access resistance (R_{AC}) in anode region as shown in Fig. 1(b) and (b) its low Schottky barrier height. This results in six times higher ON state current (I_{ON}) compared to non-recessed structure. (ii) One order lower reverse leakage (I_{OFF}) in recessed diode compared to non-recessed structure. It is possibly due to suppressed tunnelling via recessed side-walls [6]. (iii) Higher I_{ON}/I_{OFF} ratio for recessed structure because of improved I_{ON} and reduced I_{OFF} under same bias conditions as in non-recessed diode. Reverse breakdown measurements were also performed for these diodes. Recessed diode exhibits a higher breakdown voltage (330V) when compared with non-recessed diode (150V).

B. ESD Characterization

Next, the diode behaviour is studied under ESD conditions. Transmission Line Pulsing (TLP) method is used to generate rectangular ESD pulses with different pulse width (PW), and fixed rise time (1 ns). At TLP pulser with 50 Ω loadline is used to stress the anode while keeping cathode grounded in diodes with different anode area. Voltage across and current through the diode are recorded using a digital storage oscilloscope (DSO) at 25 Gps sampling rate. Captured voltage and current waveforms are averaged over the 60%−90% window of the pulse width. After each voltage stress pulse, anode current is spot measured under forward bias of 10 mV DC to monitor degradation and capture diode failure. Here, low DC bias is used to avoid degradation if any during the spot measurement. It is worth highlighting that presence of traps and carrier trapping at Schottky interface which is Ni/GaN junction depicted in Fig. 1(c)-(d), is often a serious reliability concern in GaN HEMT and diode. Given that sub-bandgap UV ($\lambda = 365$nm) light assists in de-trapping majority of the traps present within the GaN bandgap, devices are stressed both under dark and UV conditions to investigate the role of traps on the diode ESD behaviour and characteristics. It should be noted that in UV experiments, UV light is kept continuously ON throughout the experiment including spot current measurement. This is to ensure that if any field dependent trapping occurs, that is immediately de-trapped by UV light. A comparative study of diode behavior in the dark and in presence of UV light can help to understand the influence of surface/or buffer traps on device reliability. To record change in trap density, if any, during the stress, On the fly C-V measurements are performed during the test. Diodes depletion capacitance is measured at reverse bias of −2 V and at low frequency, i.e., 20 kHz. It is also worth studying the variation in the interface trap density (D_{it}) as function of ESD stress. D_{it} at anode is determined using the capacitance-conductance technique and is estimated using the following approximate relation [15];

$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \quad (1)$$

where D_{it} is density of interface defects, G_p is conductance, ω is the frequency of applied ac signal. All measurements are done at room temperature.

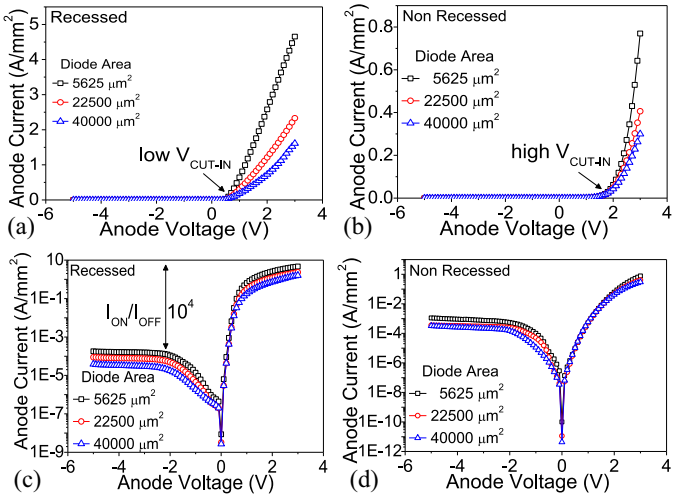

Fig. 2. DC I-V characteristics of (a) Recessed and (b) Non-Recessed Schottky diodes. I-V characteristics on Log scale for (c) Recessed and (d) Non-Recessed diodes.

IV. Experimental Results and Observations

TLP characteristics of recessed/ non-recessed Schottky diodes vary linearly in low voltage regime (<20V) and saturate at higher voltages. In both the cases, the diodes failed immediately after snapback. A closer look to low voltage region of their TLP curves in Fig. 3(a)-(b) shows an initial pinch-off faced by non-recessed diode while same is missing in recessed structure as seen in Fig. 3(a). Pinch-off originates from the additional voltage drop across the parasitic vertical access resistance (R_{acc}) offered by AlGaN region underneath the Schottky junction in non-recessed structure as illustrated in Fig. 1(a). To understand the cause of saturation in diode TLP characteristics, the Schottky diode equation is differentiated as;

$$\frac{dV}{dI} = \frac{\eta kT + qIR_s}{qI} \tag{2}$$

where, η is ideality factor and R_s is series resistance of diode.

According to Eq. (2), at high current, since $IR_s >> \eta kT/q$, the slope of TLP I-V characteristic saturates to series resistance R_s. Here the diode current is limited by R_s, which is composed of;

$$R_s = R_{sh} + R_c + R_{acc} \tag{3}$$

where R_{sh} is sheet resistance, R_c is contact resistance and R_{acc} is access region resistance, as illustrated in Fig. 1(a).

Similar to the gate-drain region in HEMT, the field-dependent charge-trapping in diode can occur via point-defects present in GaN buffer and increase R_{sh} [16]. Importantly, the deep buffer traps on virtue of slow de-trapping will induce charge accumulation and can cumulatively degrade R_{sh} with increasing stress. Further, the poor thermal conductivity of Ti/Al/Ni/Au [17] stack is expected to increase contact self-heating at high currents and increase R_c. Also, the additional R_{acc} present in non-recessed structure limits I_{TLP} and result in saturated TLP I-V characteristics. The spot leakage increases by three to four orders at the verge of snapback in both the diode types, as depicted in Fig. 3(c)-(d). Unique degradation trends are noticed in non-recessed and recessed diodes, which indicates unique failure physics in each case. This is discussed in detail in later sections.

A. Effect of Pulse Width

For both, recessed and non-recessed diodes, snapback voltage (V_{SNAP}) and failure current (I_{t2}) fall with increase in pulse width as shown in Fig. 3(a)-(b). The device gets stressed for longer duration at higher pulse width which can lead to enhanced degradation due to, (i) increased carrier scattering and mobility degradation which leads to increment in R_{ON} (ii) at high electric field at anode, hot carriers collision with lattice generates optical phonons which have longer lifetime in GaN. With increase in stress duration, phonon population increases at anode and creates hotspots which ultimately causes device failure, (iii) Electrons drifted from the cathode get accelerated, by high drift field, towards anode, which gain momentum and become hot-electrons. These hot-electrons can get trapped on either side of the heterojunction or generate new defects via dehydrogenation of point defects in the GaN epi-layer [18]. This further degrade the diode performance. Defects generated with each stress pulse accumulate and are responsible for cumulative nature of degradation as discussed in next section. The forward saturation current is found to drop significantly at high pulse width. This also confirms role of lattice heating at higher voltages. The drop was found to be significant in case of diode with recess. Pulse to pulse instability is observed close to snapback point at shorter pulse duration, which possibly originates from electrical instability in presence of minimal self-heating at short stress duration and leads to soft breakdown. However, longer stress pulses show hard breakdown due to electrothermal failure. Finally, diode without recess faces a gradual degradation, whereas the same in case of recessed diode was abrupt in nature. It should be noted that the term *soft failure* is used when device experiences a gradual degradation with increasing stress voltage, whereas term *hard failure* is used when device fails/degrades abruptly.

B. Effect of Traps

To understand, the role of surface and buffer traps on ESD behavior of GaN diode, devices are stressed under sub-bandgap UV (365nm). Figure 4 shows that for recessed and non-recessed structures, the saturation current increases, snapback failure voltage stays unchanged and ON-resistance lowers in presence of UV exposure as compared to that in dark as seen in Fig. 3. Spot measurement results shown in Figs. 4(c)-(d) exhibit softer degradation when compared to dark condition. Such gradual degradation of device in presence of UV points to trap assisted device degradation/failure. Traps can limit the diode current through phenomena like current collapse in HEMT. These results indicate that significant carrier trapping which occurs at diode surface and in buffer region of device under dark deteriorates the spot leakage, hence the diode performance. Exposure of sub-bandgap UV ($\lambda = 365$nm) is expected to de-trap carriers from both shallow and deep levels present within bandgap of GaN. Hence, it recovers the trap

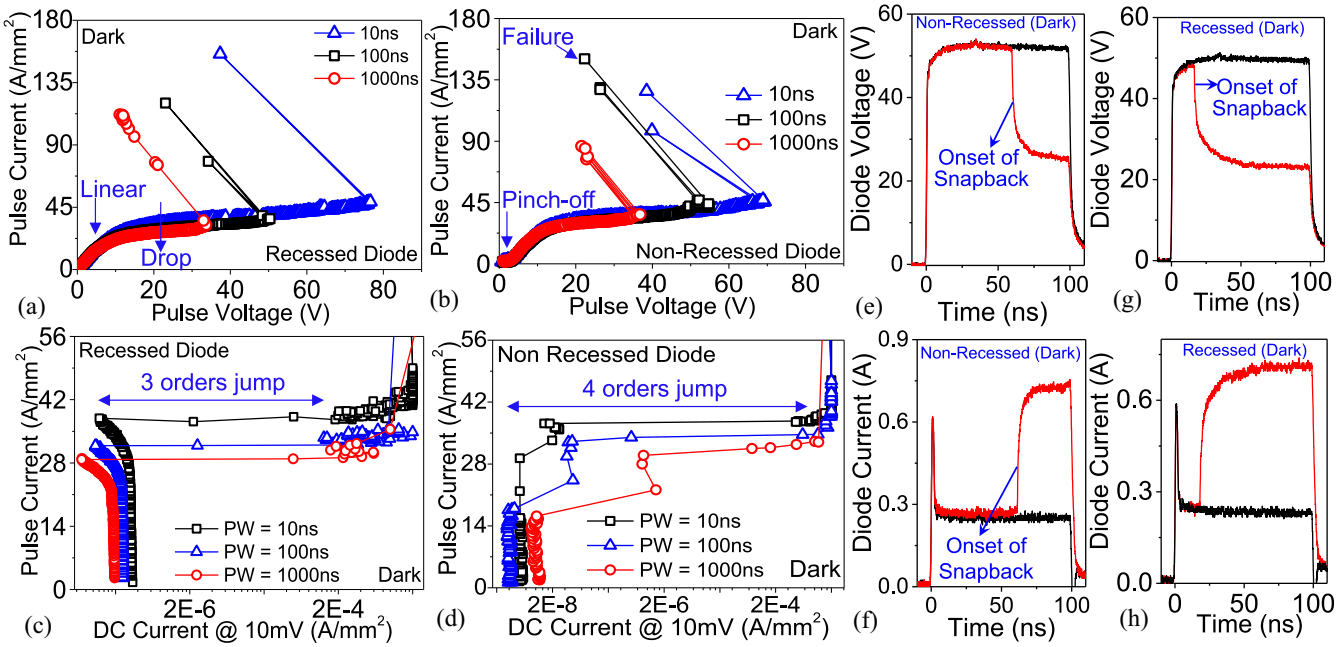

Fig. 3. Pulsed IV characteristics of (a) recessed diode (b) non-recessed diode measured at different pulse width under dark condition. Degradation in spot measured DC current of (c) recessed diode and (d) non-recessed diode exhibiting abrupt degradation and soft / gradual degradation, respectively. The variation recorded in (e),(g) diode voltage and (f),(h) current waveforms before and at the verge of snapback, in (e)-(f) non-recessed and (g)-(h) recessed diodes, tested under dark condition.

limited current which gets reflected as improvement in saturation current. The unchanged snapback voltage points to field driven failure. Possibly, the inverse peizoelectric stress which is field driven and is native to a AlGaN/GaN material system, plays role in device snapback.

C. Effect of Recess

Recently, AlGaN/GaN fully recessed Schottky diode, where the Schottky metal directly contacts a high-density 2DEG, has drawn a great attention for its low V_{CUT-IN}. Recessed anode offers significantly lower leakage and smaller V_{CUT-IN} as seen in Fig. 2. Therefore, one may be curious to understand the influence of anode recess on diode reliability. Pulse I-V characterization of recessed diode reveal the following key learnings: (i) Recessed diodes exhibit higher snapback voltage than its non-recessed counterpart. (ii) Recessed diode degrades gradually with increasing PW whereas non-recessed diodes suffer hard degradation when stressed at different PWs under dark condition. This difference in degradation mechanism is attributed to different electric field distribution in the channel and in vicinity of Schottky contact as show in Fig. 5(a). As depicted in Fig. 5(a), high field exists at anode in non-recessed diode. Peak field at anode triggers field driven degradation phenomena like carrier trapping, hot-electron effect and inverse piezoelectric effect. Additional defects generated by piezoelectric strain, further participate in carrier trapping whereas the newly developed cracks provide low energy path for leakage current. This leads to abrupt increase in drain current at the verge of failure, which manifests as sharp snapback in TLP I-V characteristics as well as transient waveforms of the device under test. On the other hand, with recessed anode, the electric field in diode gets suppressed in anode vicinity as evident from Fig. 5(a) which retards the field dependent degradation. Due to this, recessed diode exhibits higher ESD robustness than non-recessed diode.

V. Analysis and Discussion

A. Power-to-Fail vs Pulse Width

Maximum power handled by a device prior to failure, reflects the devices robustness and marks its SOA boundary. In present study, as diodes failed soon after few pulses, within snapback region itself, so power-to-fail (P_{FAIL}), is same as power-to-trigger device into snapback ($P_{FAIL} = P_{TRIG} = I_{SNAP} \times V_{SNAP}$). Recessed and non-recessed diodes are stressed under different stress time (pulse width) and a variation in P_{FAIL} with pulse width (PW) is determined as shown in Fig. 5(b). As depicted in figure, a consistent fall in P_{FAIL} is observed with increasing PW, for both recessed and non-recessed structures under dark and UV conditions. This can be attributed to increased self-heating at higher PW which causes temperature increase at Schottky junction due to current crowding in anode region. Higher junction temperature enhances thermionic injection across the Schottky barrier into the 2DEG which further increases temperature in junction area and channel region via enhancement in optical phonon density and ultimately causes thermal runaway like failure as revealed in post failure analysis of devices. In addition to this under longer stress time, defect generation and trapping at Schottky interface accelerates, as described in detail in subsequent section, which invokes early failure in device. This is verified by the fact that sub-bandgap UV light assists in carrier de-trapping and consequently a higher P_{FAIL} is

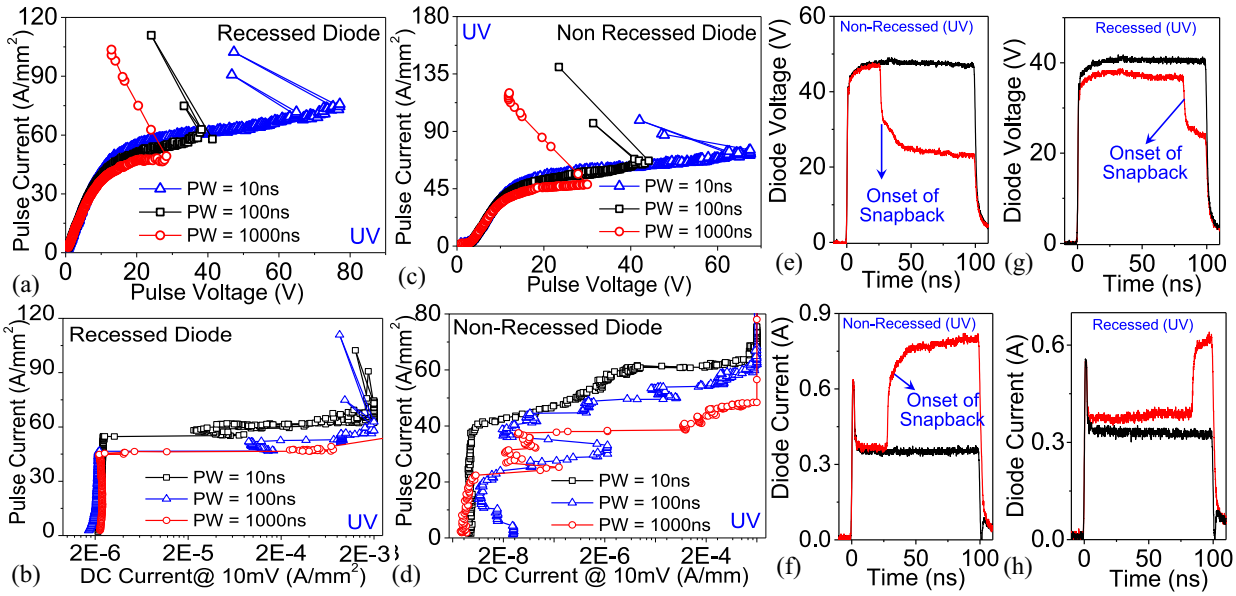

Fig. 4. Pulsed IV characteristics of (a) recessed diode (b) non-recessed diode measured at different pulse width under UV condition. Degradation in spot measured DC current of (c) recessed diode and (d) non-recessed diode. The variation recorded in (e),(g) diode voltage and (f),(h) current waveforms before and at the verge of snapback, in (e)-(f) non-recessed and (g)-(h) recessed diodes, tested under UV condition.

observed in presence of UV than in dark, for both recessed and non-recessed diodes.

B. Interface Trap Generation Under ESD Failure

As discussed so far, UV exposure showed significant effect on the pulsed IV characteristics of GaN diodes, as sub-bandgap UV (365 nm) de-trap charges from shallow and deep levels in GaN. Also, it is observed that spot measured forward DC current in diode increases beyond a certain critical stress current value, as in Fig. 3(c)-(d). To understand the root cause of this, capacitance-voltage measurements are done in different regimes of IV characteristics of recessed and non-recessed diode to capture change if any in the device stored charge due to carrier trapping under stress. To probe the fundamental nature and behavior of GaN/metal Schottky interface, variation in defect density (D_{it}) is measured at anode interface, at regular intervals during stress. Depletion capacitance is measured at -2V reverse bias and at low frequency (20 kHz) to capture maximum trap response. D_{it} evolution is studied as a function of (i) pulse width and (ii) UV exposure.

1) Influence of Pulse Width: Figure 6 shows the evolution of interface trap density (D_{it}) with stress of different pulse widths applied under dark condition, in recessed and non-recessed structures. It reveals the following; (i) beyond a certain stress current, called safe operating stress current (I_{SO}), interface trap density increases exponentially (ii) At low pulse width (10 ns), D_{it} increases by four orders before the device sees permanent failure. With increases in pulse width, defect generation occurs at slower rate and D_{it} changes only by an order of magnitude in both types of structures. Possibly the thermal annealing of the interface defects occurs at high self-heating [19], associated with larger PW.

2) Influence of UV Exposure: D_{it} variation is also studied in presence of UV light. Figure 7 presents a comparison of trap

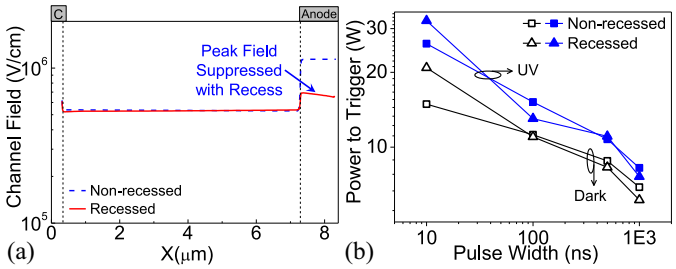

Fig. 5. (a) Electric field profile extracted in channel at 3nm from AlGaN/GaN interface in recessed and non-recessed diodes. Non-recess diode has higher electric field in the channel. (b) Triggering behavior (power to trigger) of diode under all stress configurations for recessed and non-recessed structures.

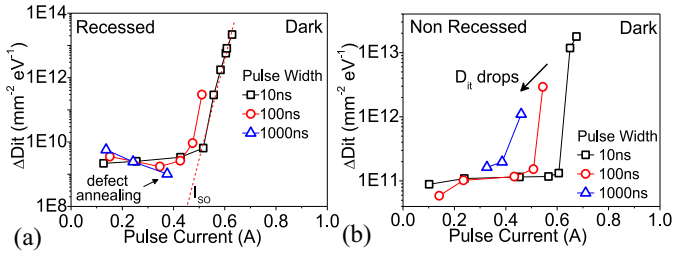

Fig. 6. Change in interface trap density (Dit) in (a) recessed and (b) non-recessed diode with pulse current, during voltage stress of different PWs under dark condition.

density evolution, in dark and UV conditions, in recessed and non-recessed structures. As clear, D_{it} increment in presence of UV occurs at much higher safe operating stress current (I_{SO}). For example, in recessed diode, D_{it} increment happens from 0.45A under dark while in UV it occurs beyond 0.75A. This study shows that UV exposure de-traps charges trapped at the interface and suppresses interface degradation.

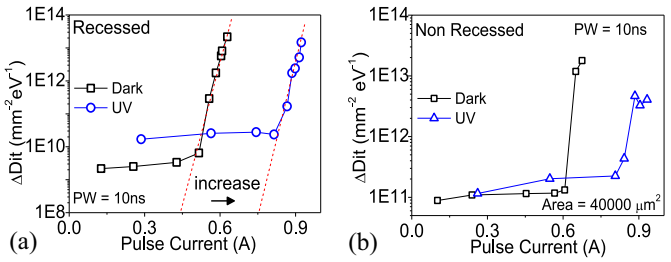

Fig. 7. Change in interface trap density (Dit) in (a) recessed diode and (b) non-recessed diode extracted as a function of stress current, compared under dark and UV conditions.

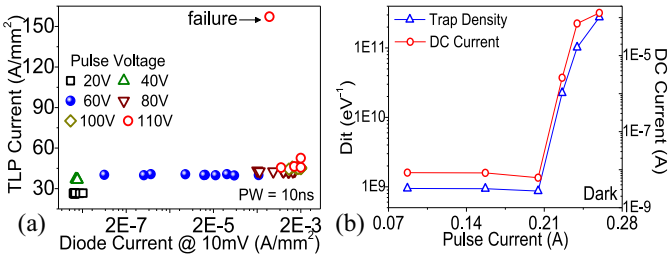

Fig. 8. (a) Diode spot DC current measured after each pulse while stressing the device with ten consecutive pulses. (b) Correlation between interface trap density (Dit) and spot measured DC current.

C. Trap Induced Interface Degradation and Correlation With Diode Failure

As highlighted and discussed above, trap density at GaN/metal Schottky interface increases with stress. To further explore the degradation physics and its nature, a diode is stressed at anode with a set of ten consecutive pulses of 10 ns each, of same amplitude. Then pulse amplitude is increased in subsequent sets as shown in Fig. 8(a). After every set of ten pulses, DC characterization of diode is done. Figure 8(a) shows that the spot measured diode current increases with each stress pulse. For example, when ten pulses of 60V are applied, the spot current gradually increases with each pulse and at the end of tenth pulse a total increment of three orders is recorded. This observation depicts that degradation is cumulative in nature, as reported earlier for HEMTs in [20] and is attributed to increased carrier trapping at Schottky interface with stress. Also, D_{it} is extracted after each set of pulses. The spot current and trap density are found to change together, that is they increase at the same stress level, as depicted in Fig. 8(b). Therefore, a strong correlation is discovered between device degradation and interface trap density. Also, Schottky barrier height (SBH) is determined from DC I-V characteristic measured at regular intervals during stress. Figure 9(a) shows variation in SBH with stress and reveals that beyond a critical stress level, SBH falls abruptly and continues to gradually degrade thereafter. The lowering of SHB can be due to physical change at the interface or can be manifestation of increased trap density and it highlights soft failure of Schottky junction under stress. DC I-V characteristic of diode measured on the fly during stress, as shown in Fig. 9(b), corroborate well with the finding. It reveals that diode leakage abruptly increases beyond a certain stress level and the Schottky junction turns

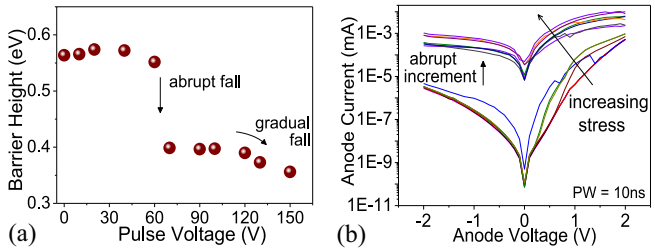

Fig. 9. (a) Change in Schottky Barrier Height with stress voltage. (b) DC I-V characteristics of non-recessed diode measured at regular intervals during a 10ns voltage stress applied at anode.

into Ohmic. From the above discussion, it can be summarized that; the GaN/metal Schottky degrades with stress due to increased interface defect density, and lowered Schottky barrier height, both of which increase the diode leakage and turn the Schottky contact into Ohmic.

VI. Failure Analysis

Damaged regions of failed devices are analysed to gain physical insight into the underlying failure mechanism(s). Diodes without recess exhibit failure close to the surface whereas recessed diodes failed with damages reaching down to GaN buffer. These differences in failure modes, is associated to the unique diode physics in each case. However, the defect density at Schottky interface increases with stress in both the cases as depicted in Fig. 7 and makes the junction leaky as evident from Fig. 8(b). In non-recessed structure, the Schottky contact is present at the device surface, so the traps are generated in top AlGaN region, which is closest to the Schottky interface. Hence, the failure occurs close to the surface as seen in Fig. 10(a). It shows multiple fine cracks propagated and merged together to cause massive failure in region between anode-cathode contacts. However, with recessed anode, Schottky contact touches the GaN buffer, therefore failure occurs deep in GaN buffer as depicted in Fig. 10(b).

A close examination of non-recessed diodes which failed under same stress, in dark and UV conditions unveils an interesting observation. As depicted in Fig. 11(a), the diode in dark, failed with more damage at corners with extra metal peeling. And the diode under UV exposure failed with lesser damaged corners as shown in Fig. 11(b). This can be explained as follows; the field enhancement at corners, leads to Schottky barrier lowering due to image force and localizes the current flow to the corners. In presence of high current density (J), thermal stress at corners increases which peels-off the anode metal due to coefficient of thermal expansion (CTE) mismatch between GaN and anode metals. Now, carrier trapping at Schottky interface further lowers the barrier as shown in Fig. 9(a) which damages larger anode region. UV exposure, de-traps the carrier and minimizes the damage as seen in Fig. 11(b). SEM micrograph of another diode which failed at 1000ns pulse stress is shown in Fig. 11(c). It shows, anode metal migrated to cathode. EDX analysis confirmed Au migration from Ni/Au Schottky contact. At high pulse width, the lattice temperature in AlGaN/GaN diode is expected to be

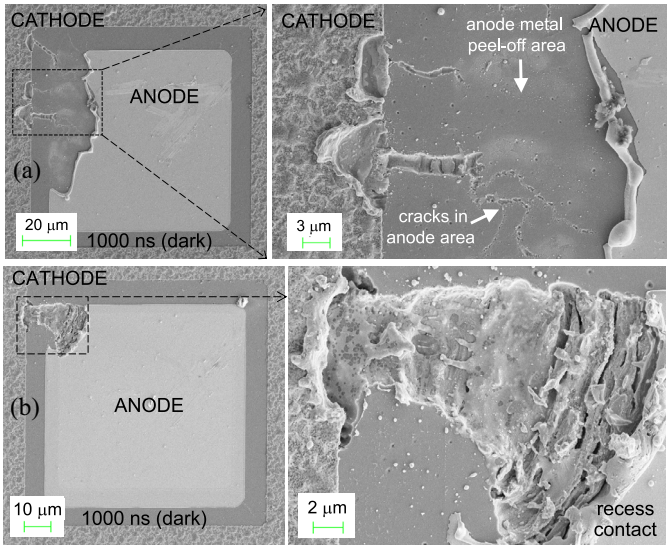

Fig. 10. SEM image of GaN Schottky diodes failed at 1000 ns voltage stress at under dark condition. (a) In non-recessed structure, failure occurred at surface with multiple cracks underneath the anode pad and metal peel-off. (b) Recessed diode failed with deep damage under the anode pad and in region between anode-cathode.

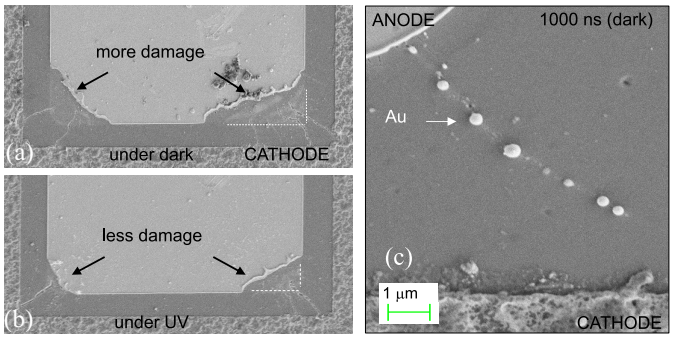

Fig. 11. SEM image of non-recessed Schottky diode failed (a) under dark and (b) in UV exposure at 100 ns voltage stress. (c) Diode failure at 1000 ns stress due to anode metal migration to cathode. EDX analysis revealed Au (14%) had migrated from Ni/Au anode contact.

high enough to melt the contact metals like Au. Then possibly, surface defects like pits assisted in Au migration as discussed next. Figure 12 shows magnified images of damaged anode-cathode regions of diode. There are two striking observations; (i) pits present along the cracked region as shown in Fig. 12(a)-(b). (ii) Presence of anode metals like Au in cracked region. Possibly, the network of pits locally weakened the material and made it prone to early cracking. Then at high fields, anode metals migrate across anode-cathode gap, preferably via cracks, as defects provide low energy path for material diffusion [21] as shown in Fig. 12(c). Figure 13 shows the recessed diodes failed at different pulse width. The device failed with multiple cracks between anode and cathode due to inverse piezoelectric effect, at low pulse width (10 ns) as seen in Fig. 13(a). At low pulse width, self-heating is minimal and the failure is electrical in nature. With increase in pulse width, self-heating and carrier trapping increase which induce severe damage as seen Fig. 13(c). Therefore, at high pulse width electrothermal/thermal failure dominates.

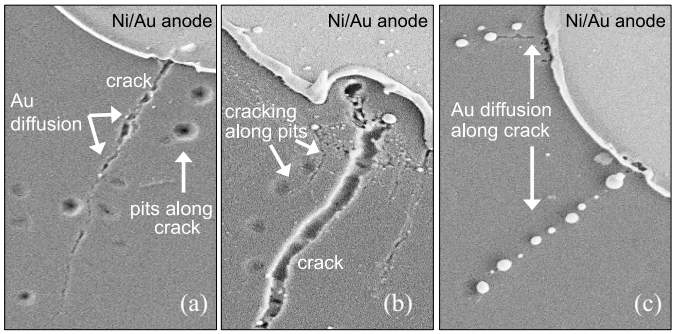

Fig. 12. Magnified SEM image of damaged regions of a failed diode highlighting material migration and pit formation along the freshly formed crack(s).

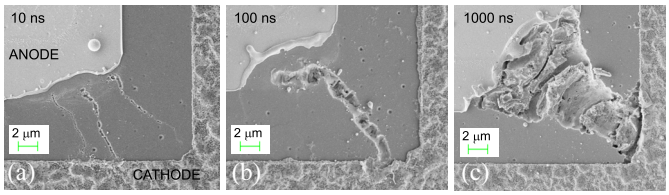

Fig. 13. SEM image of a recessed Schottky diode failed under dark at (a) 10 ns , (b) 100 ns and (c) 1000 ns voltage stress.

VII. Conclusion

Recessed diode was found to offer better current conduction and higher failure current compared to non-recessed diode. Failure in each case was discovered to be assisted by generation of traps at the metal GaN Schottky interface at anode and interface defect density was found to increase with ESD stress. Such defect assisted failure observed in these diodes, was cumulative in nature. In case of recessed diode trap generation and failure was found to be abrupt with damage occurring deep in GaN buffer. Non-recessed diode degraded in gradual manner and failure was confined to the device surface. The stress induced trap generation was found to slow down when UV light was exposed, which caused fast de-trapping of trapped charge from Schottky interface.

References

[1] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 1st ed. New York, NY, USA: Springer, 2008.

[2] S. Chen *et al.*, "HBM ESD robustness of GaN-on-Si Schottky diodes," *IEEE Trans. Device Mater. Rel.*, vol. 12, no. 4, pp. 589–598, Dec. 2012.

[3] H.-S. Lee *et al.*, "0.34 V_T AlGaN/GaN-on-Si large Schottky barrier diode with recessed dual anode metal," *IEEE Electron Device Lett.*, vol. 36, no. 11, pp. 1132–1134, Nov. 2015.

[4] Q. Zhou *et al.*, "High reverse blocking and low onset voltage AlGaN/GaN-on-Si lateral power diode with MIS-gated hybrid anode," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 660–662, Jul. 2015.

[5] W. Chen, K.-Y. Wong, and K. J. Chen, "Single-chip boost converter using monolithically integrated AlGaN/GaN lateral field-effect rectifier and normally off HEMT," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 430–432, May 2009.

[6] Y. Yao *et al.*, "Current transport mechanism of AlGaN/GaN Schottky barrier diode with fully recessed Schottky anode," *Jpn. J. Appl. Phys.*, vol. 54, no. 1, 2014, Art. no. 011001.

[7] A. Tazzoli, F. Danesin, E. Zanoni, and G. Meneghesso, "ESD robustness of AlGaN/GaN HEMT devices," in *Proc. 29th Elect. Overstress Electrostatic Discharge Symp. (EOS/ESD)*, 2007, pp. 4A.4-1–4A.4-9.

[8] S.-C. Shei, J.-K. Sheu, and C.-F. Shen, "Improved reliability and ESD characteristics of flip-chip GaN-based LEDs with internal inverse-parallel protection diodes," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 346–349, May 2007.

[9] Z. Wang, J. J. Liou, K.-L. Cho, and H.-C. Chiu, "Development of an electrostatic discharge protection solution in GaN technology," *IEEE Electron Device Lett.*, vol. 34, no. 12, pp. 1491–1493, Dec. 2013.

[10] H.-C. Chiu, K.-L. Cho, and S.-W. Peng, "A high protection voltage dual-gate GaN HEMT clamp for electric vehicle application," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits*, Nov. 2011, pp. 1–2.

[11] B. Shankar *et al.*, "On the ESD behavior of AlGaN/GaN Schottky diodes and trap assisted failure mechanism," in *Proc. 39th Elect. Overstress Electrostatic Discharge Symp. (EOS/ESD)*, Sep. 2017, pp. 1–6.

[12] V. Joshi, A. Soni, S. P. Tiwari, and M. Shrivastava, "A comprehensive computational modeling approach for AlGaN/GaN HEMTs," *IEEE Trans. Nanotechnol.*, vol. 15, no. 6, pp. 947–955, Nov. 2016.

[13] S. Arulkumaran, T. Egawa, and H. Ishikawa, "Studies on the influences of i-GaN, n-GaN, p-GaN and InGaN cap layers in AlGaN/GaN high-electron-mobility transistors," *Jpn. J. Appl. Phys.*, vol. 44, no. 5R, p. 2953, 2005.

[14] X. A. Cao, S. J. Pearton, G. Dang, A. P. Zhang, F. Ren, and J. M. Van Hove, "Effects of interfacial oxides on Schottky barrier contacts to n- and p-type GaN," *Appl. Phys. Lett.*, vol. 75, no. 26, pp. 4130–4132, 1999. [Online]. Available: https://doi.org/10.1063/1.125559

[15] D. K. Schroder, *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: Wiley, 2006.

[16] D. Bisi *et al.*, "Kinetics of buffer-related R_{ON}-increase in GaN-on-silicon MIS-HEMTs," *IEEE Electron Device Lett.*, vol. 35, no. 10, pp. 1004–1006, Oct. 2014.

[17] H. Morkoç, *Handbook of Nitride Semiconductors and Devices, Electronic and Optical Processes in Nitride*, vol. 2. Weinheim, Germany: Wiley, Aug. 2009. doi: 10.1002/9783527628414.

[18] Y. S. Puzyrev *et al.*, "Dehydrogenation of defects and hot-electron degradation in GaN high-electron-mobility transistors," *J. Appl. Phys.*, vol. 109, no. 3, 2011, Art. no. 034501. [Online]. Available: https://doi.org/10.1063/1.3524185

[19] S. Singhal *et al.*, "GaN-ON-Si failure mechanisms and reliability improvements," in *Proc. 44th Annu. IEEE Int. Rel. Phys. Symp.*, 2006, pp. 95–98.

[20] B. Shankar *et al.*, "ESD behavior of AlGaN/GaN HEMT on Si: Physical insights, design aspects, cumulative degradation and failure analysis," in *Proc. 30th Int. Conf. VLSI Design 16th Int. Conf. Embedded Syst. (VLSID)*, Jan. 2017, pp. 361–365.

[21] M. Kuball, M. Ťapajna, R. J. T. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes," *Microelectron. Rel.*, vol. 51, no. 2, pp. 195–200, 2011. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271410004786