Positive Threshold Voltage Shift in AlGaN/GaN HEMTs and E-Mode Operation By $Al_xTi_{1-x}O$ Based Gate Stack Engineering

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***Abstract*—In this paper, for the first time, we have experimentally demonstrated enhancement mode (e-mode) AlGaN/GaN high-electron-mobility transistor (HEMT) operation by integrating p-type high-κ $Al_xTi_{1-x}O$ based gate stack. Concentration of Al in Al-Ti-O system was found to be a tuning parameter for the threshold voltage of GaN HEMTs. The high-κ properties of $Al_xTi_{1-x}O$ as a function of Al % are studied. Superiority of AlTiO over other p-oxides such as CuO and NiO_x is proven statistically. Using the high-κ and p-type AlTiO, in conjunction with a thinner AlGaN barrier under gate, 600-V e-mode GaN HEMTs are demonstrated with superior ON-state performance ($I_{ON} \sim 400$ mA/mm and $R_{ON} = 8.9\ \Omega$-mm) and gate control over channel ($I_{ON}/I_{OFF} = 10^7$, SS = 73 mV/dec, and gate leakage < 200 nA/mm), beside improved safe operating area reliability.**

***Index Terms*—AlTiO gate, enhancement mode (e-mode) AlGaN/GaN high-electron-mobility transistors (HEMTs), energy band engineering, p-type metal oxide, ternary oxide.**

I. Introduction

GALLIUM NITRIDE (GaN)-based high-electron-mobility transistors (HEMTs) have gained prominence as high power switches [1] in the emerging power semiconductor industry due to their high breakdown field, superior electron mobility as well as saturation velocity, and higher temperature stability. AlGaN/GaN HEMTs are, in principle, depletion mode (d-mode) devices, which is due to inherent 2-dimensional electron gas (2DEG) at the heterointerface formed by piezoelectric and spontaneous polarization. However, for reliable and low loss power switching systems, enhancement mode (e-mode) HEMTs are a must. There are several techniques to achieve e-mode operation, such as recessed gate [2]–[15], F^- ion implantation under gate [16], [17], and p-GaN gate [18], [19]. F^- ion under gate is unstable under high-field stress or temperature conditions [20], whereas use of a thick p-GaN layer under gate [18] to deplete 2DEG can effectively weaken the gate drive and hence, compromises on the device performance. In this endeavor of better and reliable e-mode GaN HEMTs, the development of gate dielectrics such as Al_2O_3, SiN, SiO_2, HfO_2, HfAlO, and $HfSiO_x$ has gained prominence as it reduces gate leakage and allows larger gate swing, both being imperative for power applications [2], [3], [6], [21]. However, conventional dielectric, such as Al_2O_3, SiN, and SiO_2, based HEMTs require complete recessing of barrier layer under gate stack to achieve the e-mode operation [6], [8], [15]. This has detrimental impact on channel mobility and device performance [15]. Another approach toward e-mode HEMTs is to use p-type oxides, such as CuO and NiO_x, which have been recently shown to positively shift threshold voltage (V_{TH}) in GaN HEMTs [22]. They, however, do not offer a tunable control over V_{TH}, have relatively lower-κ (11–18) and lower bandgap ($E_g = 1.36$ eV) resulting in higher leakage current. Recently ternary oxides, such as Ti-Hf-O and Ti-Al-O, have emerged as promising gate oxide for GaN HEMTs as they offer higher dielectric constants while retaining a high bandgap [23]. A preliminary work presented by Le *et al.* [24] has shown AlTiO-based gate stack in AlGaN/GaN MIS-capacitor and have demonstrated V_{TH} shift from −7 V (Al_2O_3) to −6 V ($Al_{0.73}Ti_{0.27}O$).

Keeping these issues in mind and limited work available on gate stack for the e-mode operation, the idea behind this paper is to develop a tunable, p-type, high-κ, and stable oxide system for the e-mode GaN HEMT operation without the need to completely recess the AlGaN barrier. Here, tunability of p-type behavior offers a control knob over V_{TH}, high-κ improves gate's control over channel, stability of developed oxide improves statistical variation, and avoiding full

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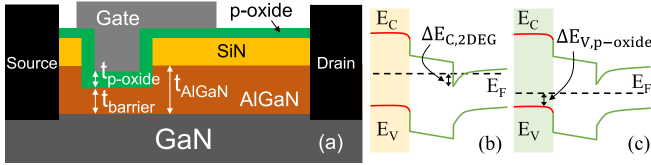


Fig. 1. (a) Cross-sectional view of the HEMT with p-type metal oxide gate and partially recessed AlGaN barrier under the gate for e-mode operation. Energy-band diagram of AlGaN/GaN HEMTs with (b) conventional dielectric and (c) p-type oxide. The p-type oxide shifts E_F below E_C in the channel.

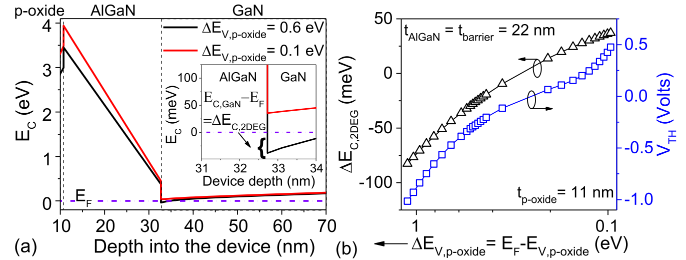
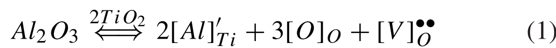


Fig. 2. Impact of energy difference between oxide's Fermi energy level (E_F) and valence band energy ($E_{V,\text{p-oxide}}$) on (a) conduction band energy extracted along a vertical cut line under the gate electrode and (b) shift in E_F away from conduction band in the channel ($\Delta E_{C,2\text{ DEG}}$) and resulting shift in threshold voltage of the device.

recess keeps the oxide-semiconductor interface away from channel, which greatly improves the channel and hot carrier performance. Hence, a ternary system, which offers the capability to tune oxide properties such as, dielectric constant, crystallization temperature, and bandgap by independently engineering individual components, has been utilized in this paper. Section II deals with developing design guidelines and physical insights, using TCAD simulations, to demonstrate promise of p-oxide, which can potentially enable e-mode operation in AlGaN/GaN HEMTs. Section III describes the processing of the HEMTs using AlTiO-based gate stack whose V_{TH} tunability and superiority over other p-oxides is examined in Section IV. Section V deals with the performance of the e-mode HEMTs realized using an optimized ternary oxide system and AlGaN barrier thinning under gate. This paper is finally concluded in Section VI.

II. Genesis: P-Oxides and Energy Band Engineering

Al_2O_3, a widely used gate dielectric in GaN HEMTs, has a wider E_g ($\sim$ 6.5–9 eV), very high crystallization temperature (900 °C) and an offset of 2–2.25 eV with GaN conduction band (E_C). However, it has a lower κ ($\sim$9). TiO_2, on the other hand, has advantage of being high-κ (> 60) oxide, but suffers from a lower E_g ($\sim$ 3.4 eV), lower crystallization temperature (370 °C), and very low band offset with GaN E_C [23]. An improved band offset with GaN and higher crystallization temperature while maintaining a high-κ can be achieved by designing a ternary system of Al-Ti-O by introducing Al_2O_3 in TiO_2. Its reaction dynamics can be described by Kröger and Vink [25] notation as



$$Al_2O_3 \overset{2TiO_2}{\Longleftrightarrow} 2[Al]'_{Ti} + 3[O]_O + [V]_O^{\bullet\bullet} \quad (1)$$

$$[V]_O^{\bullet\bullet} \Longleftrightarrow [V]_O + h^{\bullet\bullet}. \quad (2)$$

According to the defect chemistry discussed in (2), Al_2O_3 introduction in TiO_2 creates positively charged oxygen vacancies and negatively charged Al fixed charges occupying Ti sites. The positively charged oxygen vacancies result in neutral oxygen vacancies and introduce holes in the Al-Ti-O system infusing p-type character to the oxide, as shown in (2). The extent of p-type nature of the oxide is thus a function of Al% incorporated in the oxide.

Fig. 1(a) depicts the AlGaN/GaN HEMT structure with p-type gate oxide. Unlike conventional dielectrics, introduction of p-type oxide in the HEMT gate stack should shift the Fermi energy (E_F) in the channel away from conduction band edge (E_C), as depicted in Fig. 1(b) and (c). Detailed TCAD simulations were carried out to evaluate the impact of p-type nature of the gate oxide on the shift in Fermi energy level from the conduction band energy in the channel ($\Delta E_{C,2-\text{DEG}}$). A well calibrated simulation setup [26] was used with oxide bandgap taken similar to that of TiO_2 ($\sim$ 3.4 eV) [27]. Incorporation of Al was considered as a p-type dopant in this gate oxide, which results in a reduction in $\Delta E_{V,p-\text{oxide}}$ ($= E_F - E_{V,p-\text{oxide}}$) as Al% is increased.

Simulation results, as shown in Fig. 2(a), further quantify the argument that by increasing p-type doping in the gate oxide, the Fermi energy level in the channel region can be modulated to result in channel depletion. Fig. 2(b) depicts that Fermi energy in the channel shifts below the GaN conduction band energy level ($\Delta E_{C,2\text{ DEG}} > 0$ eV) when the oxide valence band to Fermi energy gap ($\Delta E_{V,p-\text{oxide}}$) falls below $\sim$0.2 eV. In this case, the 2DEG under the p-oxide gate stack was found to be depleted, which lead to a positive shift in V_{TH} as depicted in Fig. 2(b). This signifies that V_{TH} of the HEMTs can be controlled by $\Delta E_{V,p-\text{oxide}}$, which can be engineered by tuning Al% in AlTiO. The same is experimentally demonstrated in the subsequent section where Al% in AlTiO is shown to be a parameter to control V_{TH} of AlGaN/GaN HEMTs.

III. Experimentation and Device Fabrication

HEMTs were processed over a commercial grade AlGaN/GaN heterojunction grown heteroepitaxially on 6″ Si (111) by metalorganic chemical vapor deposition (MOCVD). A 3-μm GaN was grown on Si by using 150-nm AlN and 1-μm graded AlGaN transition layers. A 22-nm $Al_{0.25}Ga_{0.75}N$ was epitaxially grown on GaN. The epistack was covered by a 40-nm thick *in situ* grown SiN cap.

Transistors were processed on the stack following the steps shown in Fig. 3. Source–drain contact formation started with partial etching of AlGaN barrier followed by Ti/Al/Ni/Au evaporation. Ohmic contacts were obtained by 820 °C 30 s N_2 annealing of the stack. MESA isolation was then carried out using Cl_2-based plasma etching. To achieve precise control over etch rate, atomic layer etching (ALE) was carried out for devices with reduced AlGaN barrier under gate using O_2-BCl_3 plasma. The ALE process helped achieve a controlled etch rate

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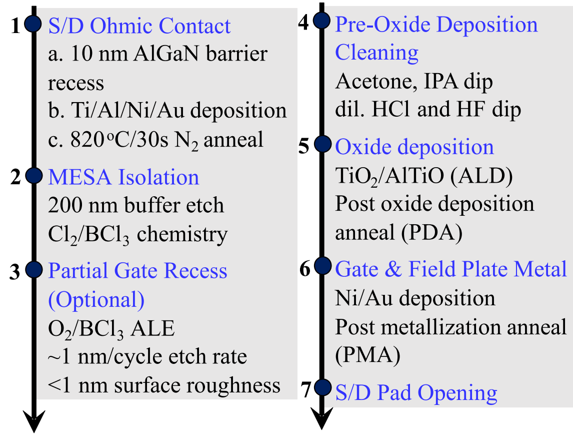
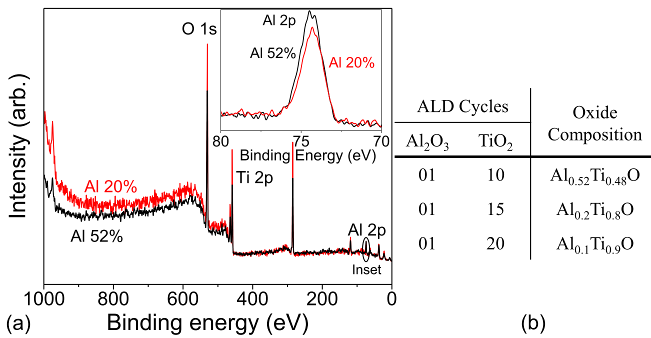


Fig. 3. Fabrication procedure adopted for demonstrating AlGaN/GaN HEMTs designed for e-mode operation with the proposed AlTiO-based gate stack.



ALD Cycles		Oxide Composition
Al_2O_3	TiO_2	
01	10	$Al_{0.52}Ti_{0.48}O$
01	15	$Al_{0.2}Ti_{0.8}O$
01	20	$Al_{0.1}Ti_{0.9}O$

Fig. 4. (a) XPS spectra of ALD grown AlTiO validating incorporation of Al in TiO_2, represented by the presence of Al (2p) peak (as depicted in the inset). Increased Al 2p peak intensity shows higher Al% in grown AlTiO. (b) Oxide composition extracted from XPS spectra shows Al% in AlTiO is controlled by number of Al_2O_3 and TiO_2 deposition cycles in the ALD chamber.

of ∼1 nm/cycle with an etched AlGaN surface roughness ∼ 0.6 nm. In addition to controlled etch rate, ALE also leads to reduced plasma damage. Ample surface treatments were carried out before gate oxide deposition to ensure high-quality oxide-semiconductor interface. Finally, Ni/Au deposited by metallization followed by liftoff process was subjected to a low temperature anneal to form the gate.

Introduction of Al in TiO_2 to study its V_{TH} tunability in AlGaN/GaN HEMTs was carried out in a BENEQ thermal atomic layer deposition (ALD) system. Al_2O_3 was deposited in the ALD chamber using trimethylaluminum (TMA) and H_2O precursor, whereas titanium tetraisopropoxide (TTIP) and H_2O was used for TiO_2. The number of TiO_2 deposition cycles in between each Al_2O_3 cycle was varied to control respective metal concentrations [Fig. 4(b)] in the $Al_xTi_{1-x}O$ system, which was validated from the Al 2p, Ti 2p, and O 1 s peaks in the x-Ray Photoelectron Spectroscopy XPS spectra shown in Fig. 4(a). Hall measurements confirm p-type nature of developed AlTiO with a majority hole concentration of 1.4×10^{14} cm^{-3} obtained in $Al_{0.52}Ti_{0.48}O$. This designed ternary oxide was deposited as a gate oxide for AlGaN/GaN HEMTs. HEMTs with high-κ TiO_2 as gate oxide

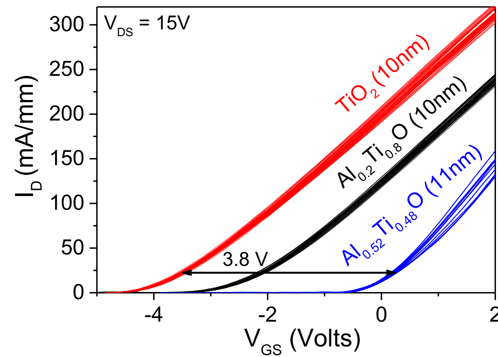


Fig. 5. Transfer characteristics of AlTiO- and TiO_2-based HEMTs depicting positive shift in V_{TH} with Al introduction. AlTiO with 52% Al resulted in a ∼3.8 V V_{TH} shift as compared to TiO_2-based HEMTs. Data shown are for unrecessed AlGaN barrier with $t_{barrier} = t_{AlGaN} = 22$ nm.

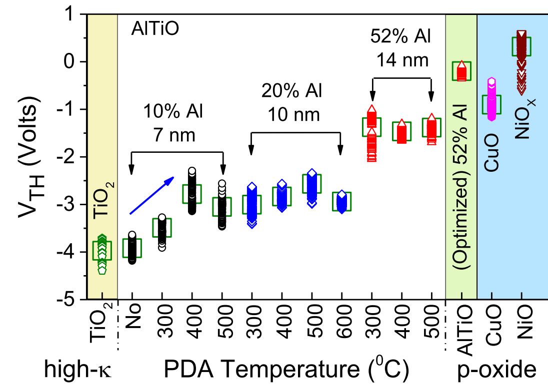


Fig. 6. Threshold voltage (extracted using peak transconductance method) as a function of PDA temperatures, Al% and oxide thickness. The same is compared with V_{TH} extracted from HEMTs using TiO_2-, CuO-, and NiO_x-based gate stacks. PDA was carried out in N_2 ambient for 1 min. Data shown are for un-recessed AlGaN barrier with $t_{barrier} = t_{AlGaN} = 22$ nm.

were also realized on the same epistack for comparison. In addition, standard p-oxides, namely, CuO (sputtering) and NiO_x (e-beam evaporation)-based HEMTs were realized too, to benchmark the developed p-type AlTiO-based gate stack. Over 100 post-oxide deposition anneal (PDA) and post-gate metallization anneal (PMA) splits were carried out to optimize the ternary $Al_xTi_{1-x}O$ system.

IV. V_{TH} Tuning With AlTiO and Its Superiority

AlGaN/GaN HEMTs with ALD grown high-κ TiO_2 gate oxide exhibited a deep seated V_{TH} of ∼ −4 V (extracted using maximum transconductance method), leading to a typical d-mode operation as observed in Figs. 5 and 6. They also show a permanent shift in HEMT V_{TH} when the proposed AlTiO was used in the gate stack. A ∼ 1 V shift in V_{TH} was observed for 20% Al, whereas AlTiO with 52% Al resulted in a ∼3.8 V shift ($V_{TH} = -0.2$ V). This definitive positive V_{TH} shift in AlGaN/GaN HEMTs clearly shows the potential of p-type AlTiO where Al is a control knob to tune V_{TH}. It is worth mentioning that data for more than 150 transistors per process lot has been analyzed to demonstrate a stable gate oxide with least statistical variability.

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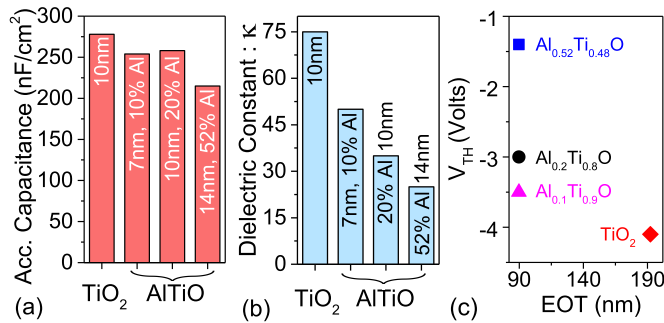

Fig. 7. (a) Accumulation capacitance of AlTiO- and TiO_2-based HEMTs. (b) Relative dielectric constant (κ) of the oxides extracted from respective accumulation capacitances, which is a series connection of the capacitance of the gate oxide, 3-nm GaN cap, 25-nm AlGaN barrier, 1-nm AlN spacer, and 2-DEG. The 2-DEG has been considered to be formed 2 nm from the AlGaN/GaN heterointerface [7]. (c) V_{TH} of the HEMTs as a function of their EOT showing positive shift in V_{TH} with increasing Al% for similar EOT.

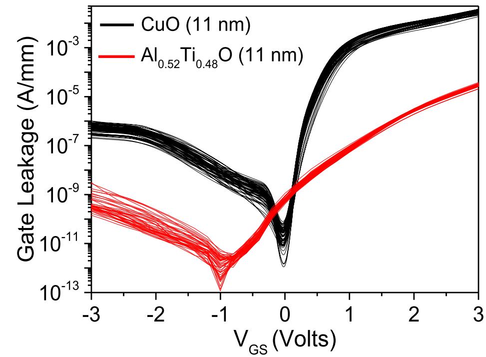

Fig. 8. Gate leakage in AlTiO- and CuO-based HEMTs shows higher gate leakage in CuO as compared to HEMTs with similar thickness of AlTiO.

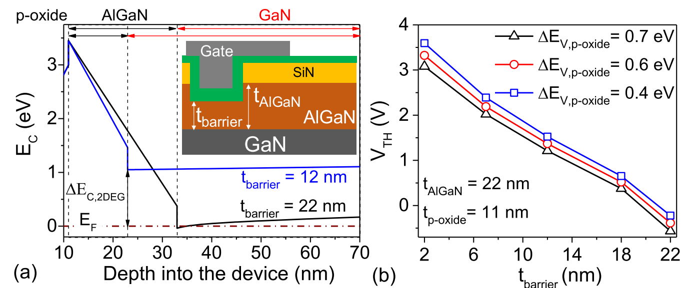

Fig. 9. (a) Shift in conduction band energy as a function of $t_{barrier}$ for a constant $\Delta E_{V,p\text{-oxide}} = 0.58$ eV and $t_{AlGaN} = 22$ nm. (b) Resulting shift in threshold voltage as a function of $t_{barrier}$ for different $\Delta E_{V,p\text{-oxide}}$. Computations were carried out for a constant p-oxide thickness of 11 nm.

Besides Al%, the V_{TH} of the HEMTs was found to be a function of PDA temperature, when carried out for an optimized PMA of 300 °C 10 min in forming gas ambient as shown in Fig. 6. It is worth highlighting that the impact of PDA temperature on V_{TH} is a function of Al% in AlTiO. For lower Al% (10%), V_{TH} shows a strong dependence on PDA temperature, whereas for higher Al% (52%), V_{TH} is independent of PDA temperature. This can be attributed to the activation of Al incorporated within TiO_2, which is a function of Al% as well as PDA temperature. As depicted in Fig. 6, an increase in Al% results in a higher V_{TH} for similar PDA temperature, thereby indicating a higher concentration of activated Al. Temperature also aids in increasing the concentration of activated Al, i.e., Al replacing Ti in the oxide, thereby resulting in positive V_{TH} shift. V_{TH}, however, becomes temperature independent at high Al concentration (52%) as the number of Ti sites available to activate Al becomes limited. A maximum positive $V_{TH} \sim -0.2$ V could be achieved in $Al_{0.52}Ti_{0.48}O$ under optimized growth conditions. As shown in Fig. 7(c), it is worth highlighting, here, that increased Al% in AlTiO led to higher positive shift in V_{TH} while keeping the effective oxide thickness (EOT) of $Al_xTi_{1-x}O$ fixed. The EOT was calculated from the relative dielectric constant of the oxides [Fig. 7(b)] extracted from accumulation capacitance [Fig. 7(a)] of the HEMTs. A relative dielectric constant as high as 75 was obtained for TiO_2. Increase in Al% in TiO_2 results in a reduction of κ. However, a relatively high-κ of ~25 was achieved for the optimized $Al_{0.52}Ti_{0.48}O$ system, which confirms high-κ nature of the proposed oxide.

Standard p-type oxides such as CuO- and NiO_x-based GaN HEMTs also resulted in positive shift in V_{TH} as shown in Fig. 6. However, these oxides can be claimed to be inferior to the designed AlTiO as: 1) CuO offers a lower V_{TH} shift when compared to AlTiO; 2) CuO as gate oxide resulted in a ~4 order (~2 order) higher leakage current under accumulation (inversion) condition when compared to AlTiO for the same thickness [Fig. 8]; and 3) NiO_x-based HEMTs were found to suffer from very high gate leakage compared to AlTiO and CuO, with large variability (data not shown).

V. AlTiO-Based E-Mode HEMT

A V_{TH} of −0.2 V was achieved under optimized PDA and PMA conditions for $Al_{0.52}Ti_{0.48}O$-based GaN HEMTs as seen in the previous section. However, for normally-OFF operation, the 2DEG must be completely depleted under the gate at $V_{GS} = 0$ V. This can be achieved by bringing the gate stack closer to the channel by partial removal of the AlGaN barrier under gate ($t_{barrier}$) before depositing the p-oxide as shown in Fig. 9(a). Furthermore, Fig. 9(b) indicates that with an increase in p-type doping in the gate oxide (lower $\Delta E_{V,p-\text{oxide}}$), the effective barrier thickness required to achieve e-mode operation can be increased. This keeps the channel away from the etched surface thereby causing minimal damage to channel transport properties. AlGaN/GaN HEMTs realized with the optimized AlTiO gate stack show a clear V_{TH} shift from −0.2 to 0.5 V, when barrier thickness was reduced from 22 to 8 nm, as depicted in Fig. 10. Reducing barrier thickness ($t_{barrier} = 8$ nm) under the gate in conjunction with 11-nm p-type AlTiO resulted in e-mode GaN HEMTs [Fig. 10(a)] without compromising ON-state performance. The thinner AlGaN barrier also resulted in an improved channel control, which has resulted in a lower OFF-state leakage and improved subthreshold swing (SS) as depicted in Fig. 10(c). The OFF-state leakage was found to reduce by 100×, whereas SS for e-mode HEMT was found to improve from 101 to 73 mV/dec when $t_{barrier}$ was scaled from 22 to 8 nm. At this point, it is worth highlighting that the channel is still 8 nm away from the oxide-semiconductor interface, which helps

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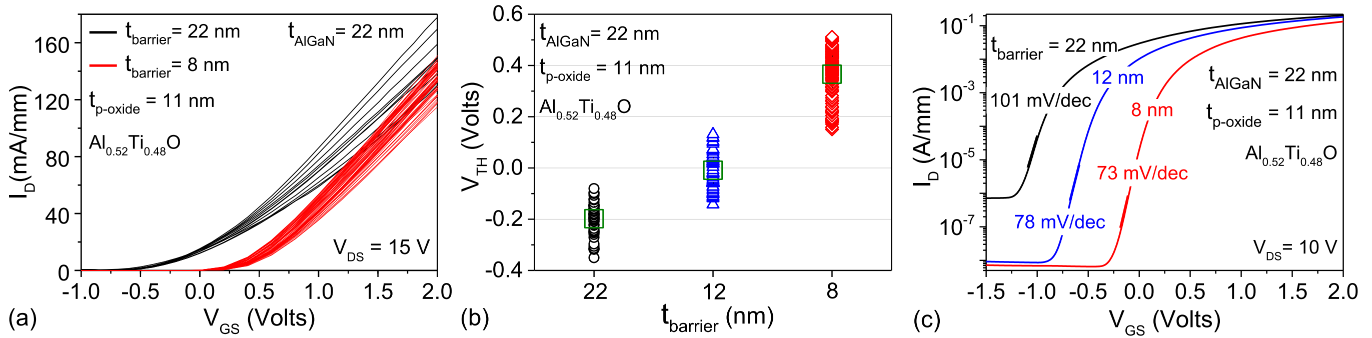

Fig. 10. (a) Transfer characteristics of HEMTs realized using optimized p-oxide with different t_{barrier}. AlTiO devices with reduced AlGaN barrier under gate show an e-mode operation with positive V_{TH}. (b) Linear shift in V_{TH} from negative to positive is observed when barrier thickness under the gate was scaled. (c) Significant improvement in OFF-state leakage and SS, beside V_{TH} shift, for reduced t_{barrier} depicts an improved gate control over channel.

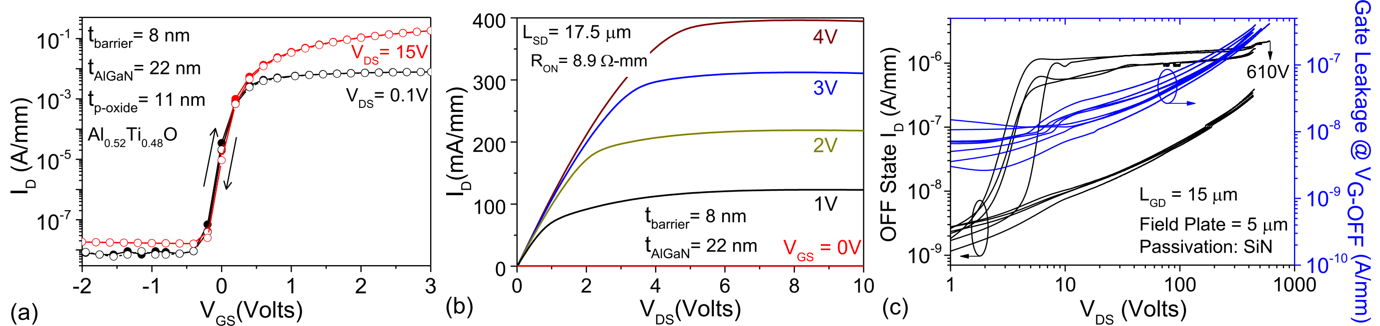

Fig. 11. (a) Dual sweep $I_D - V_{\text{GS}}$ characteristic of the p-type oxide (11-nm-thick $Al_{0.52}Ti_{0.48}O$)-based e-mode HEMTs with reduced barrier thickness under gate shows negligible hysteresis. (b) $I_D - V_{\text{DS}}$ characteristics of the 11-nm-thick $Al_{0.52}Ti_{0.48}O$-based e-mode HEMTs depicting superior ON-current and ON-resistance performance. (c) OFF-state three terminal breakdown characteristic of the device measured at $V_{\text{GS}} = -1$ V with substrate grounded.

mitigating detrimental effects of plasma damage on 2DEG induced during O_2-BCl_3 ALE of AlGaN. This is manifested in Fig. 11(a), which shows an extremely low V_{TH} hysteresis of ∼ 30 and ∼ 40 mV during I_D–V_{GS} dual sweep, for V_{DS} of 0.1 and 15 V, respectively. V_{TH} hysteresis of ∼ 24 and ∼ 10 mV was found under pulsed I_D–V_{GS} dual sweep, for V_{DS} of 0.1 and 1 V. respectively (data not shown).

Furthermore, Fig. 11(a) and (b) shows the superior ON-state performance of the e-mode HEMTs (L_G =3 μm and L_{SD} =17.5 μm) with a drain current of ∼ 400 mA/mm at V_{GS} = 4 V, R_{on} =8.9 Ω-mm and I_{on}/I_{off} = 10^7. Moreover, Fig. 11(c) depicts the three-terminal breakdown voltage (substrate grounded) > 600 V for the HEMTs measured in OFF-state. Low OFF-state drain and gate leakage under high drain stress conditions highlight the usability of these devices. Catastrophic failure was observed for the devices along MESA and not along gate–drain region. Breakdown voltage is expected to improve further with appropriate MESA isolation which will be pursued in our future work.

In this context, it is worth mentioning that though there is an initial jump in the drain leakage, it, however, saturates until the stack fails catastrophically. No such trend is observed for gate leakage. Since the substrate was grounded for these measurements, this increase in drain leakage can be attributed to vertical leakage through dislocations, a common defect in GaN on Si stack. It should be noted that the focus of this paper is to demonstrate a novel p-type oxide as a potential contender for e-mode HEMT's gate stack. V_{TH} > 1 V can be achieved by further optimizing the p-oxide, which will be pursued in our future works. Finally, Fig. 12 shows that reducing AlGaN barrier thickness under gate stack led to an improved safe operating area (SOA) reliability which is attributed to improved electric field distribution with thinner barrier under the gate [28]. Owing to field-induced carrier trapping in the drift region, SOA for unrecessed devices was found to be limited by electric field peak at the drain edge [28]. A thinner barrier under the gate relaxes this field near the drain edge by redistributing it between two peaks, one near gate edge and another near drain edge, thereby improving SOA

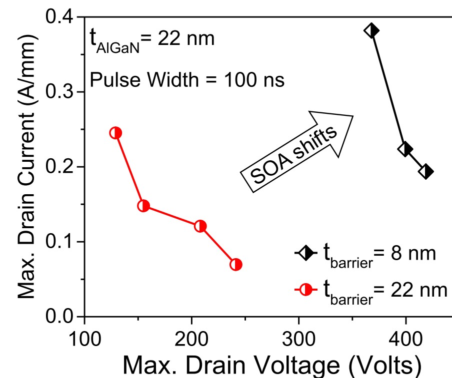

Fig. 12. Increased SOA boundary observed for HEMTs with thinner AlGaN barrier under gate.

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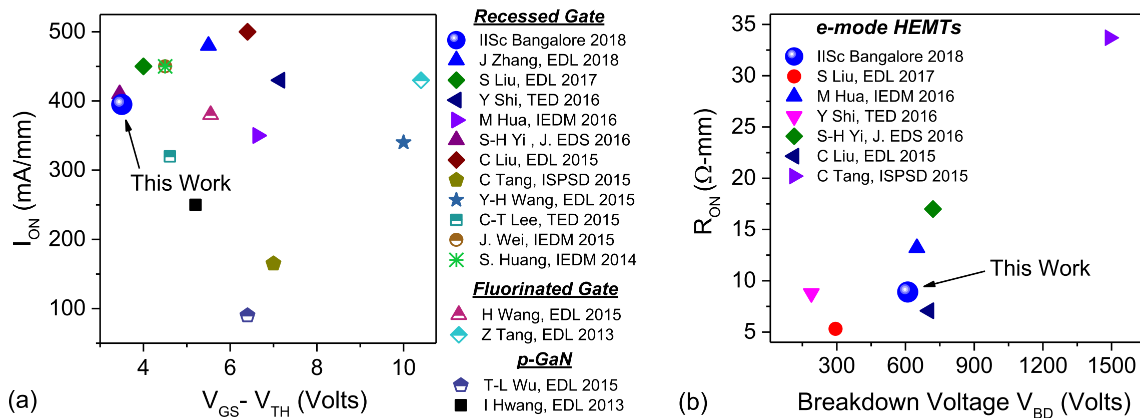

Fig. 13. (a) State-of-the art of AlGaN/GaN e-mode HEMT's reported ON-state performance, compared for various techniques to achieve the e-mode operation. (b) R_{ON} - V_{BD} performance of the e-mode devices reported in this paper, when compared to the reported works till date. The three-terminal breakdown voltage was measured for an OFF-state source–drain leakage of 1 μA/mm. The e-mode HEMTs developed by partially recessed AlGaN barrier and p-type AlTiO gate oxide result in ON-state performance on par with best reported numbers.

of the device. A uniform field redistribution between the two peaks is achieved for an optimum barrier thickness, leading to maximized SOA boundary. The ON-state performance of e-mode HEMTs in this paper with p-type AlTiO was found to be on par with the best reports till date, as depicted in Fig. 13.

VI. Conclusion

$Al_xTi_{1-x}O$ was shown to have p-type behavior, which when integrated in HEMT gate stack resulted in positive V_{TH} shift where Al% (x) can be used as a control knob to tune V_{TH}. The proposed p-oxide was found to be superior when compared with p-oxides such as CuO and NiO_x in terms of gate leakage and variability. Using the proposed p-type oxide, e-mode HEMTs with $V_{TH} \sim 0.5$ V were demonstrated for the first time. Channel being away from dielectric-semiconductor interface, realized HEMTs resulted in negligible hysteresis. Thinner barrier and high-κ nature of AlTiO resulted in superior gate control over channel and ON-state performance on par with best reported till date ($I_{on} \sim 400$ mA/mm, $I_{on}/I_{off} = 10^7$, SS $= 73$ mV/dec, $R_{on} = 8.9$ Ω-mm, gate leakage $<$ 200 nA/mm), besides high breakdown and improved SOA reliability.

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