Safe Operating Area of Polarization Super-junction GaN HEMTs and Diodes

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***Abstract*— This article reports safe operating area (SOA) assessment in polarization super-junction (PSJ)-based GaN high-electron mobility transistor (HEMT) and Schottky diode. The degradation physics, which limits SOA in these devices under high-voltage and high-current-injection conditions is presented. Trap-induced SOA degradation and the role of PSJ in SOA improvement are unveiled. In PSJ-field-effect transistor (FET), the impact of PSJ length and its position on SOA robustness are studied. The role of self-heating and substrate effect on degradation are discussed. PSJ diodes with different configurations of Schottky contact are investigated. The correlation between PSJ length and failure threshold is discovered, besides power and field dependence of SOA boundary. Compared with their conventional counterparts, unique failure modes are discovered in PSJ-based GaN HEMT and diode.**

***Index Terms*— GaN field-effect transistor (FET), polarization super-junction (PSJ), reliability, safe operating area (SOA).**

I. Introduction

GALLIUM nitride has clearly emerged as the next-generation material for power semiconductor devices. Figures-of-merit (FOM) calculations highlight a need for GaN-based power devices to achieve cost-effective, high-frequency, and high-efficiency power electronics compared with Si devices [1]. AlGaN/GaN heterojunction-based high-electron mobility transistor (HEMT) has shown superior switching performance with higher power efficiency when compared with Si or SiC-based systems. Given the early stage of development, there is an increasing thrust that it will only get better. While the conventional AlGaN/GaN power HEMTs are around for more than 25 years [2], polarization super-junction (PSJ) concept is recently introduced in the GaN HEMT family [3]–[6]. It can potentially improve the $R_{ON} - V_{BD}$ tradeoff in GaN HEMT beyond its 1-D limit [4], [5]. Recently, it has been demonstrated that the addition of PSJ to existing GaN MOS-HEMT improves its short-circuit performance [7], [8]. However, before PSJ-based GaN HEMTs and diodes are deployed for widespread usage, it is crucial to understand their failure mechanisms and degradation phenomena under high fields and/or high-current-injection scenarios, which can potentially limit their safe operating area (SOA). While early works highlight the superiority of PSJ-based GaN devices over conventional devices, the physics governing the SOA of PSJ-based GaN devices is not well understood. This article, which reports an extension of our earlier work [9], evaluates SOA of PSJ-based GaN HEMTs and Schottky diodes. Device degradation and failure physics, under high-voltage stress and high-current-injection conditions, encountered at SOA boundary, are investigated while considering the key design and technology parameters.

This article is structured as follows. Device architecture and experimental characterization setup are described in Section II. SOA boundary of PSJ-GaN HEMT [PSJ-FET] and the impact of various device parameters on SOA robustness is presented in Sections III and IV, respectively. Section V reports trap-induced effects under stress at SOA boundary. Physical insights into degradation mechanisms governing SOA are derived in Section VI, while failure modes unique to PSJ-FET are disclosed in Section VII. Results and discussion related to SOA assessment of PSJ-GaN diode are covered in Section VIII. Finally, key findings and conclusive remarks are drawn in Section XI.

II. Device Architectures and Test Setup

PSJ consists on a double heterojunction GaN/AlGaN/GaN, and enjoys coexistence of positive and negative polarization charges at AlGaN/GaN and GaN/AlGaN interfaces with perfect charge balance [4]. Under OFF-state, two-dimensional hole gas (2DHG) and two-dimensional electron gas (2DEG) discharge via gate and drain respectively, to offer a nearly uniform box-like field profile [6] from the uncompensated polarization charges in PSJ drift region, as illustrated in Fig. 1. Hence, breakdown voltage (V_{BD}) of PSJ-GaN FET is significantly higher than conventional GaN HEMT and scales with PSJ length [5]. In ON-state, PSJ offers ultradense 2DEG and 2DHG with high carrier mobility which drastically reduce device's R_{ON}. PSJ-GaN FET and conventional GaN HEMT used in this study show R_{ON} of 12 and 19.7 Ω mm,

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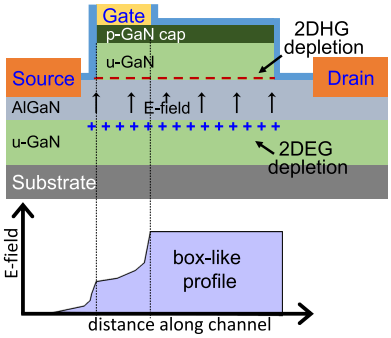

Fig. 1. Device schematic of PSJ-FET exhibiting a uniform field distribution in drift region under OFF-state.

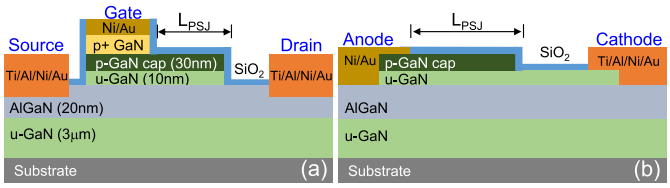

Fig. 2. Cross-sectional schematic of (a) PSJ-GaN FET and (b) PSJ-GaN Schottky diode with details of layer stack under study.

respectively, and V_{BD} of 641 and 503 V, respectively. As seen, $R_{ON\text{-}PSJ} < R_{ON\text{-}HEMT}$ and $V_{BD\text{-}PSJ} > V_{BD\text{-}HEMT}$, which indicate higher FOM of PSJ-GaN FET. Therefore, PSJ concept promises to overcome R_{ON} versus V_{BD} tradeoff in GaN HEMT as reported earlier [4], [5].

Normally-ON PSJ-based FETs and Schottky barrier diodes (PSJ-SBD) as shown in Fig. 2, were realized over a GaN/AlGaN/GaN stack. The material stack was grown on two different substrates namely, Si and sapphire using metal–organic chemical vapor deposition (MOCVD). The epitaxial stack consisted of 3-μm thick unintentionally doped GaN buffer, 20 nm undoped $Al_{0.23}Ga_{0.77}N$ barrier, 10 nm unintentionally doped GaN, 30 nm p-GaN layer doped with Mg (3×10^{19} cm^{-3}) and thin p^+ GaN layer with high Mg doping (1×10^{20} cm^{-3}) as shown in Fig. 2. Ti/Al/Ni/Au metal stack was deposited to realize Ohmic contact at source/drain in FETs and cathode in diodes. Ni/Au-based metal stack formed Ohmic contact with p-GaN and Schottky with AlGaN and 2DEG. Finally, devices were passivated with 500-nm-thick SiO_2. Conventional HEMTs and SBD were also realized in the same flow by selective plasma etching of p-GaN and u-GaN layers over the same wafer. The 100-μm-wide normally ON transistors with different super-junction lengths (L_{PSJ}), with and without u-GaN in source–gate and gate–drain regions, were studied in this article.

High voltage–high current pulse characterization of devices under test was performed to determine the SOA boundary and failure threshold of devices. Ultrafast rectangular pulses of 100-ns pulsewidth (PW) and 1 ns rise time/fall-time were generated using transmission line pulsing (TLP) method and were used to stress the device under test. A time gap of 200 ms was introduced between two consecutive pulses to ensure device relaxation before the next pulse is applied. In transistors, the voltage pulses were applied at drain while the gate was DC biased using an source measure unit whereas in diodes, the anode was pulsed with respect to the cathode. Device voltage and current waveforms were captured using a digital storage oscilloscope at 25-Gps sampling rate. Recorded waveforms were averaged over 70%–90% window of PW to generate a family of I–V characteristics of the device under test. DC I–V and capacitance–voltage (C–V) characteristics of the devices were measured at regular intervals during the stress, to probe their degradation physics and failure mechanisms. C–V characteristics were measured at low frequency to capture maximum trap response. All measurements were done at room temperature.

III. SOA Boundary of PSJ-FET

Pulsed I–V characteristics of PSJ-FET were measured by applying pulse voltage at the drain and gate DC biased. Voltage pulse amplitude was increased in steps of 1 V until the device faced permanent failure. The locus of device failure points on I–V plane defines the SOA boundary. SOA of conventional GaN HEMT was also measured. Fig. 3 depicts the SOA of PSJ-FET and HEMT tested under similar conditions. PSJ-FET shows ~40% larger SOA than a conventional HEMT. Higher SOA in PSJ roots from, first, a higher breakdown voltage of PSJ-FET. For instance, in the present case, PSJ-FET exhibited V_{BD} of 641V whereas conventional HEMT failed at 503V in OFF-state for the same gate to drain spacing. In PSJ-FET, the 2DHG and 2DEG get depleted in PSJ region under OFF-state to generate a box-like uniform field distribution [5] as discussed later. This leads to improvement in breakdown voltage. Second, no current collapse is seen in PSJ-FETs unlike in conventional HEMT as shown in Fig. 3. In HEMT, the peak field that is present at the gate edge (drain side) enhances electron injection from the gate to the device surface and barrier layer present in the gate–drain region. These electrons get trapped at the trap sites present in the gate–drain region and are reported to cause current collapse in HEMT [10]. However, in PSJ-FET, the hole gas present in PSJ region, acts as gate connected field plate and suppresses the peak field at the gate edge [5]. Field reduction in gate vicinity suppresses tunneling across gate [11] and curtails electron injection into trap states present at passivation/GaN interface [12] and in AlGaN barrier in the gate–drain region [10]. Hence, PSJ-FET carries higher failure current I_{FAIL} at larger V_{DS} than in conventional HEMT.

IV. SOA Robustness and Power To Fail

SOA robustness is an important parameter for power semiconductor devices. It is evaluated as the maximum power sustained by the device before its permanent failure at the SOA boundary and is termed as power-to-fail (P_{FAIL}). P_{FAIL} is a product of breakdown voltage (V_{BD}) and failure current (I_{FAIL}).

A. Effect of Super-Junction Position

Three variants of PSJ-FETs were realized where super-junction was present: 1) all over source to drain

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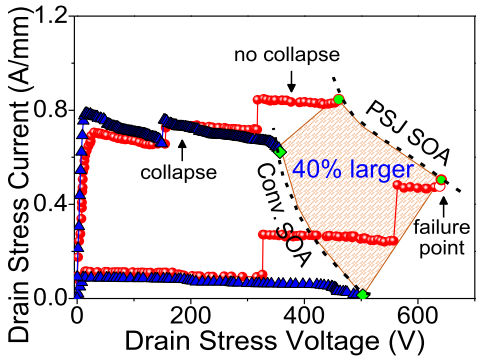

Fig. 3. Comparison of pulsed I–V characteristics of PSJ-GaN FET and conventional GaN HEMT depicting respective SOA boundaries.

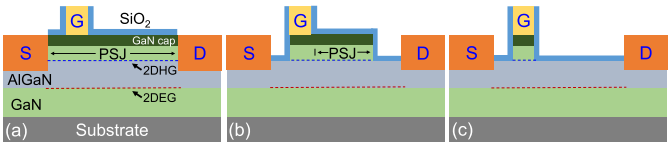

Fig. 4. Cross-sectional schematic of GaN FET (a) with PSJ in source–drain region, (b) PSJ only in gate–drain region, and (c) without PSJ.

region; 2) in gate–drain region; and 3) no PSJ as shown in Fig. 4. P_{FAIL} was recorded for each device type and the result is plotted in Fig. 5(a). Among the three device variations, highest P_{FAIL} was observed in the case where super-junction was present in gate–drain region.

B. Effect of Super-Junction Length (L_{PSJ})

As seen, PSJ in the gate–drain region offered the highest P_{FAIL}. Therefore, in the device type with PSJ in the gate–drain region P_{FAIL} was further determined for 10, 15, and 20 μm of PSJ lengths (L_{PSJ}) as shown in Fig. 5(b). P_{FAIL} is observed to decrease with increase in L_{PSJ}. It can be explained as follows; PSJ acts as field plate [5] and shifts the peak field away from the gate edge to the drain-side PSJ edge. The increase in PSJ length pushes the peak field toward the drain. At larger L_{PSJ}, the following effects are observed: 1) peak electric field localizes closer to the drain edge [7], which enhances impact ionization rate and triggers early avalanche causing premature breakdown in the device; 2) higher R_{ON} and higher thermal resistance from longer drift region which increases self-heating in device; and 3) the presence of a larger drift area is believed to enhance carrier trapping and accelerate trap driven degradation as discussed in Section V.

To summarize the learnings so far, the u-GaN/AlGaN/GaN material stack gives rise to a lateral polarization super-junction in PSJ-FET. PSJ-FET exhibited the following advantages over conventional GaN HEMT.

1) It offers linear potential distribution and "box-like" field profile in drift region that enhances device breakdown voltage.
2) It suppresses current collapse which is a severe issue in conventional GaN HEMT.

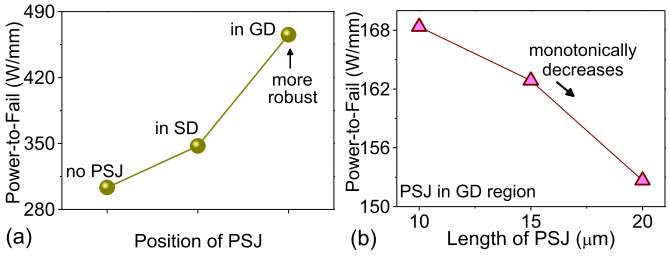

Fig. 5. (a) Power-to-fail in devices with and w/o PSJ. Device with PSJ in gate–drain (GD) region shows maximum ruggedness. (b) In the device with PSJ in GD region, P_{FAIL} decreases with the increase in length of PSJ region.

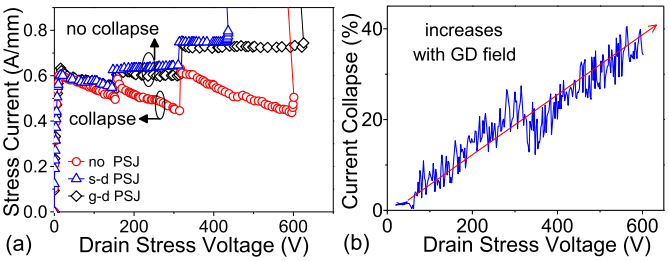

Fig. 6. (a) Pulse I–V characteristics of different variants of PSJ-FET. (b) Variation in current collapse in FET w/o PSJ with the increase in pulse drain stress.

3) Position of PSJ influences device robustness and the device with PSJ in the gate–drain region showed the highest power-to-fail.
4) P_{FAIL} reduces with increase in PSJ length beyond an optimum value.
5) The improved device robustness with PSJ results in 40% wider SOA boundary in PSJ-FET than in conventional HEMT.

V. Trap-Induced Effects Under SOA Stress

The pulse stress during switching operation can potentially degrade a device's performance over the period [13], [14]. Hence, it is important to understand the degradation mechanism active in different operating regimes of the device under pulse condition. Fig. 6(a) shows pulse I–V characteristics of three variants of PSJ-FET.

A. Trapping Induced Current Collapse

Pulse I–V characteristic of a HEMT without PSJ, was measured at $V_{GS} = 2$ V. Beyond V_{DS} 170 V, I_{DS} begins to drop from its saturation value of 0.6 A/mm and continues to collapse until it reaches ~0.4 A/mm at the device failure point (595 V). Current collapse in GaN HEMT is reported due to electron trapping in the gate–drain region [10] when electron injection occurs from gate to surface and barrier layer. The peak electric field present at the drain-side gate edge facilitates increased injection and current collapse. Current collapse is observed to monotonically increase with V_{DS} as shown in Fig. 6(b) and exhibits strong dependence on the gate–drain electric field. An abrupt kink is observed in I_{DS} at higher V_{DS}. It is believed to originate from field-assisted electron emission

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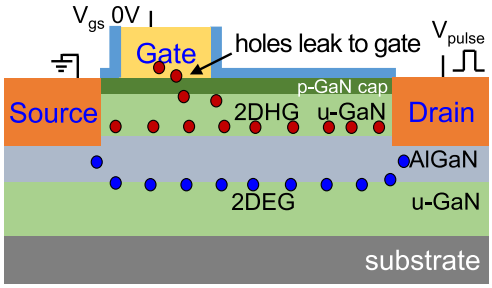

Fig. 7. Schematic of PSJ-FET with super-junction in entire region between source and drain. Under ON-state, holes from 2DHG leak to Ohmic p-GaN gate.

from deep traps present in buffer and barrier region at high electric field [15], [16].

B. Super-Junction to Mitigate Current Collapse

PSJ acts like a field plate [5] and relaxes field crowding at the drain-side gate edge. Therefore, electron injection from gate to surface and barrier region reduces and the associated current collapse gets suppressed in PSJ-FET. Fig. 6(a) depicts the I–V characteristic of PSJ-FET (blue and back curves), which shows no significant current collapse. From this observation, it can be inferred that the presence of PSJ in the gate–drain drift region suppresses current collapse. To further explore the benefits of PSJ, another device variation was tested where PSJ is present all over between the source and the drain region. Fig. 6(a) shows the I–V characteristic (blue curve) of the corresponding device, which depicts missing current collapse in the presence of PSJ; however, it suffered premature failure at 430 V. This can be explained as follows: the presence of PSJ all over source to drain region forms dual channel with 2DHG present at top u-GaN/AlGaN and 2DEG present at bottom AlGaN/u-GaN heterojunction. Under ON-state, holes from 2DHG leak to gate electrode since gate forms an Ohmic contact with 2DHG as illustrated in Fig. 7. Due to high gate leakage, the device faces early thermal failure at the gate. This is elaborated in subsequent sections.

C. Trap-Induced Degradation

To monitor degradation caused by pulse stress, a PSJ-FET was tested with voltage pulse of 100-ns PW and 1 ns rise time applied at drain and gate DC biased at 2 V. Open channel (no gate bias applied) linear drain-to-source DC current (I_{dc}) was spot measured at 50-mV DC bias, after each voltage pulse to monitor degradation caused by pulse stress. Here, low DC bias is used to minimize device degradation if any during spot measurement. Fig. 8(a) shows the variation in I_{dc} with pulse stress current for devices on Si substrate with and without PSJ in the gate–drain region. As seen, the devices degraded with each stress pulse. In the absence of PSJ, device degraded rapidly up to 30%, whereas with PSJ, degradation impeded and ~15% change is I_{dc} is noticed. PSJ-FETs realized on sapphire, degraded in a different manner. Fig. 8(b) shows the I_{dc} degradation trends in devices with different L_{PSJ}. The following observations are worth mentioning: 1) in all

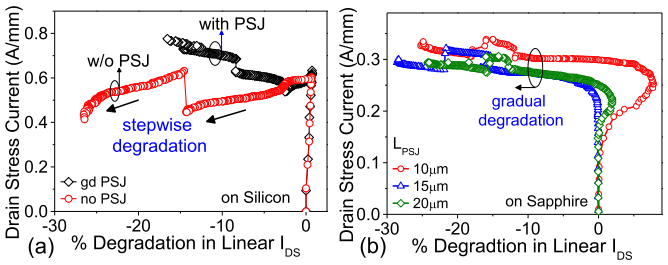

Fig. 8. Degradation in drain current, spot measured after each stress pulse applied across devices while conducting pulsed I–V-based SOA measurements. (a) Trap-induced degradation appears dominant in PSJ-FET on Si. (b) Degradation trends in linear I_{DS} in PSJ-on-sapphire with different L_{PSJ}. In all cases, device undergoes gradual degradation unlike in PSJ-on-Si.

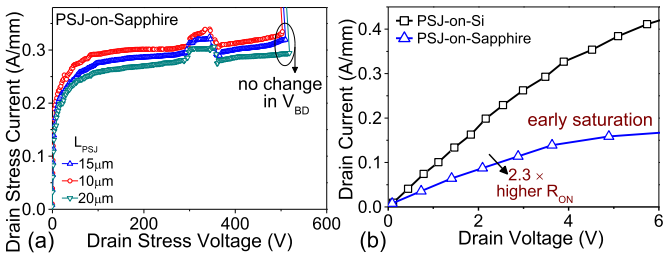

Fig. 9. (a) Pulse I–V characteristics of PSJ-FET on sapphire with different length of PSJ region. PSJ length shows minimal impact on breakdown voltage unlike in PSJ-on-Si. (b) PSJ-on-sapphire shows higher R_{ON} and early current saturation than PSJ-on-Si.

the cases, a gradual degradation in I_{dc} is noticed unlike in PSJ-on-Si where changes occurred in stepwise fashion; 2) moreover, the degradation remained independent of L_{PSJ} and I_{dc} degraded up to 30% in all the cases; 3) PSJ-on-sapphire suffered higher degradation (~30%) than PSJ-on-Si (~15%). These observations point to the presence of effects other than trapping, which dominate degradation in PSJ-on-sapphire as discussed next.

D. Role of Self-Heating and Substrate

Similar devices with PSJ-on-Si and PSJ-on-sapphire were tested under the same conditions and their P_{FAIL} values were compared. PSJ-on-Si exhibited higher P_{FAIL} than PSJ-on-sapphire. Fig. 9(a) shows pulse I–V characteristics of PSJ-on-sapphire FETs. No breakdown voltage scaling is observed with an increase in L_{PSJ}. A comparison of I–V characteristics in linear region with PSJ-on-Si FETs, as in Fig. 9(b), reveals 2.3 times higher R_{ON} and early saturation in current in PSJ-on-sapphire despite having similar 2DEG density and low field mobility in PSJ-on-Si and PSJ-on-sapphire FETs. However, a drastic difference was observed in high field mobility under high-voltage and high current stress which is attributed to the low thermal conductivity of the sapphire substrate. Poor thermal diffusivity of sapphire leads to ~8× higher thermal time constant in GaN-on-sapphire than GaN-on-Si epi-stack [17]. This results in serious self-heating in HEMT on sapphire and retains higher temperature in the channel region [18] and expedites electron-phonon scattering and reduces 2DEG mobility. This observation highlights

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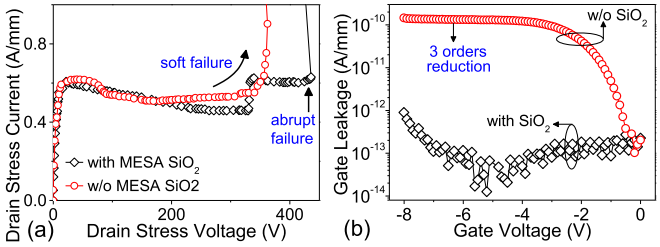

Fig. 10. (a) Comparison of breakdown behavior of PSJ-FET with and without SiO_2 at the MESA edge. In the absence of SiO_2, the high gate leakage current induces premature failure. (b) Presence of SiO_2 at the MESA edge suppressed the gate leakage by three orders and improved the breakdown voltage as seen in (a).

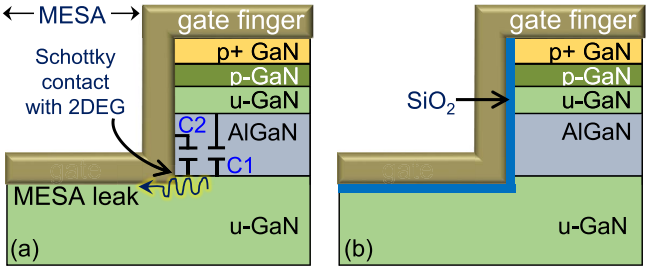

Fig. 11. (a) Cross section schematic of PSJ-FET (a) without SiO_2 at the MESA edge, illustrating parasitic capacitances in device and leakage from 2DEG to gate finger at the MESA edge. (b) Presence of SiO_2 at the MESA edge suppresses the gate-to-MESA leakage component.

that substrate can also limit device performance. It is worth mentioning that, influence of intrinsic defects/trap originating from buffer/substrate mismatch also play significant role here. Degraded mobility also resulted in R_{ON} increase and increment in the associated self-heating. Ultimately, at high stress current, the device sees thermal runaway like failure as confirmed by postfailure analysis. It is possible to reduce the thickness of the sapphire to achieve effective thermal management.

E. Impact of MESA Robustness

Robustness of PSJ-FET in a high-voltage regime can also be limited by improper design of isolation techniques like MESA. Devices with/without SiO_2 at the MESA edge were tested under same stress conditions. Fig. 10(a) shows the I–V characteristics of the corresponding devices. Device without SiO_2 at MESA exhibited a gradual increase in I_{DS} beyond 200 V_{DS} and suffered soft failure around 350 V. Another device with SiO_2 at the MESA edge showed an improvement in breakdown voltage (420 V) and faced abrupt failure. Based on this observation, it is quite possible that the MESA edge too plays a hidden role in the failure mechanism of PSJ-FET; hence, it is worth investigating. DC characterization of devices with and without MESA-SiO_2 was done. It was interesting to find that the two devices although with same geometry except the SiO_2 at the MESA edge, had very different gate leakage characteristic as shown in Fig. 10(b). Device without MESA-SiO_2 possessed three orders higher gate leakage than device with MESA-SiO_2. Fig. 11 shows the cross section schematic of device's MESA edge. A portion of the gate finger

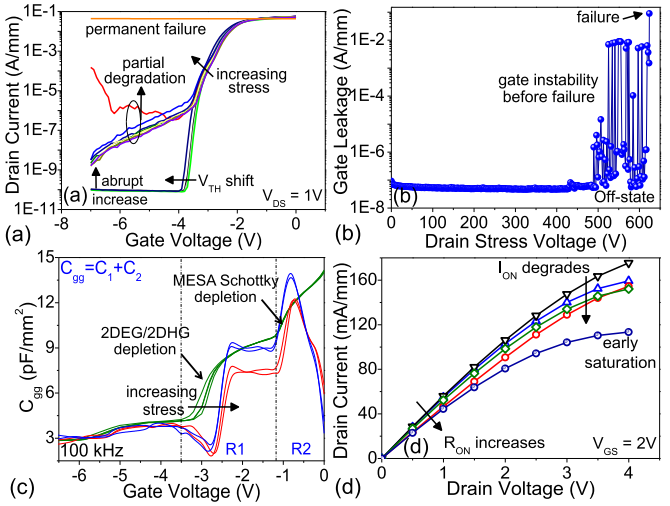

Fig. 12. Variation in DC characteristics of PSJ-FET under OFF-state stress. (a) Partial increase in drain-to-source leakage with negative shift in threshold voltage, highlighting deteriorated gate control. (b) Increase in gate leakage with instability on the verge of failure. (c) Change in gate capacitance–voltage characteristic. (d) Drop in DC ON-current under OFF-state drain stress.

running over the MESA sidewall forms a parasitic Schottky contact with 2DEG. A component of 2DEG leaks to the gate finger via the MESA edge as illustrated in Fig. 11(a) and results in high gate leakage as shown in Fig. 10(b). At high V_{DS}, premature breakdown of this parasitic MESA Schottky diode limits the lifetime of PSJ-FET. When SiO_2 is introduced at the MESA edge as in Fig. 11(b), the parasitic MESA Schottky diode ceased to exist and consequently, the gate leakage suppressed by three orders, improving device's breakdown voltage [Fig. 10(a)].

VI. Physical Insights Into Degradation and SOA

To understand the failure mechanisms under ON- and OFF-state, complete DC characterization of the device was done at regular intervals during the test.

A. Failure Under OFF-State

To begin with, a device was stressed under pinch-OFF conditions at 100-ns PW and its DC I–V and C–V characteristics were recorded at different stress levels. Fig. 12 shows the corresponding results from intermediate DC characterization. As depicted in Fig. 12(a), device failure under OFF-state stress occurred with partial increase in drain–source leakage current accompanied with negative threshold voltage shift. These observations point to an interesting failure physics and can be explained as follows: In PSJ-FET, there exists an inherent P-N body diode formed by 2DHG/2DEG as shown in Fig. 13. The voltage stress at the drain, reverse biases the inherent P-N diode and depletes the AlGaN drift region. At higher stress voltage, the holes generated at drain from impact ionization are swept toward the lowest potential at source as illustrated in Fig. 13. Under the influence of the gate field, some excess holes are collected by the gate and constitute gate leakage [Fig. 12(b)]. Few holes get trapped at p-GaN/u-GaN interface

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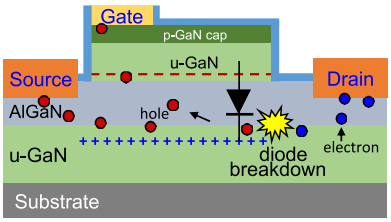

Fig. 13. Schematic of breakdown mechanism of parasitic P-N-junction, which is formed by 2DHG and 2DEG in a PSJ-FET.

underneath gate and cause V_{TH} shift [Fig. 12(a)]. Fig. 12(c) presents the variation in the total gate capacitance (C_{gg}) at different drain stress. C_{gg} consists of two parallel capacitances, namely: 1) Capacitance-C_1 from PSJ layer formed by 2DHG and 2DEG and 2) Capacitance-C_2 of parasitic MESA Schottky diode where gate-finger contacts 2DEG at MESA sidewall as depicted in Fig. 11(a). Under low stress condition [green curves in Fig. 12(c)], C–V profile shows two-stage depletion, as marked by two distinct slopes in regions R1 and R2, and is related to capacitances C_1 and C_2. At $V_{gs} = -1$ V, Schottky depletion causes drop in C_{gg}. Then, at $V_{gs} = -3$ V, 2DEG and 2DHG deplete, which decreases C_{gg} further. At higher drain stress level, a significant change in C–V profile is noticed [blue and red curves in Fig. 12(c)]. Possibly, the hot holes from impact ionization, on their way to the gate, also create crystallographic defects in AlGaN/GaN regions and eventually create percolation paths in GaN [19] under the gate. This modifies C_1 and eventually C_{gg} profile in region-R1. Postfailure scanning electron microscopy (SEM) image of the tested device in Fig. 14(a) shows multiple damages along the gate finger, which corroborates well with the C–V measurement result. Furthermore, the leaky MESA Schottky invokes progressive failure in the device as discussed in the previous section and evident from Fig. 10(a). This gradually pushes MESA Schottky junction to premature breakdown as confirmed by damaged gate at the MESA edge in the failed device [Fig. 14(a)]. Degradation of MESA Schottky diode alters C_2, which reflects as modified C_{gg} in region-R2 of the C–V characteristic. Fig. 12(b) shows the variation in gate leakage with drain stress. Instability in gate leakage is observed on the verge of breakdown and gate leakage increases to the same order as OFF-state drain–source current. This affirms the formation of defects at high drain stress, in and underneath gate-stack and reveals that the gate current beside the MESA leakage, increases due to the introduction of drain-to-gate leakage via the percolation path(s), which are formed by randomly generated defects in GaN under stress [19]. Fig. 12(d) shows degraded output characteristics of the device. The reduced I_{ON} is the manifestation of increased R_{ON} due to carrier trapping in the AlGaN barrier and at the AlGaN/GaN interface.

B. Failure Under ON-State

Under ON-state, the voltage drop across the channel lowers the potential underneath JFET region, formed by PSJ. This increases the strength of reverse bias and depletion width across JFET [7], which shrinks the effective conduction area

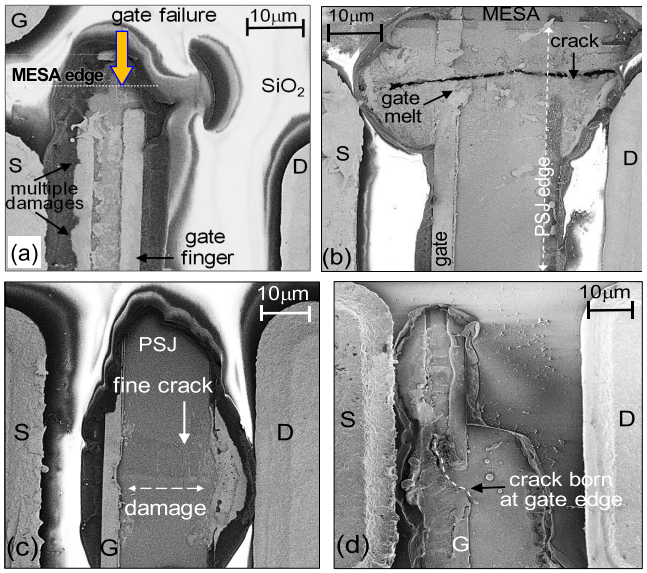

Fig. 14. SEM micrograph of PSJ-FETs that failed under (a) OFF-state and (b)–(c) ON-state. (d) SEM micrograph of conventional HEMT that failed under ON-state.

to enhance local current density at the PSJ edge. High current density with peak electric field enhances power density and causes hotspot formation at the PSJ edge, which leads to thermal failure as confirmed by postfailure analysis. Therefore, ON-state failure is thermally driven and exhibits power dependence while OFF-state failure involves impact ionization and shows field dependence. Unlike in OFF-state stress, under ON-state, gate and drain–source leakage remained intact until the device failed abruptly, which is another signature of the thermal failure [8]. It was found that the vertical buffer leakage did not change both under ON- and OFF-state stress, which implies the absence of buffer degradation, unlike in conventional HEMT [13], where dominant avalanche-injection mechanism triggers impact ionization in buffer causing failure.

VII. Unique Failure Modes in PSJ-FET

To gain physical insight into the underlying failure mechanism, failure analysis of damaged devices was done using SEM and energy dispersive X-Ray (EDX) spectroscopy. In all the devices, the top SiO_2 passivation was blown off from the damaged area. Fig. 14(a) shows SEM micrograph of PSJ-FET which failed when stressed under OFF-state. Multiple damages can be seen along the gate edge. EDX analysis confirmed the presence of Au in damage location. A portion of gate finger was blown off at the MESA edge. The gate failure with multiple damages corroborates well with the degradation mechanism proposed in Section VI, where hot holes generated from impact ionization degraded the gate-stack. SEM micrograph in Fig. 14(b) shows the device that failed under ON-state stress. It shows a massive crack present in the source–drain region. Another device failed in ON-state with bulging of GaN film with folding/curling of gate metal at damage spot, as depicted in Fig. 14(c). These observations indicate the thermal nature of the failure. This can be verified from the fact that gate finger melted exclusively at the damaged locations

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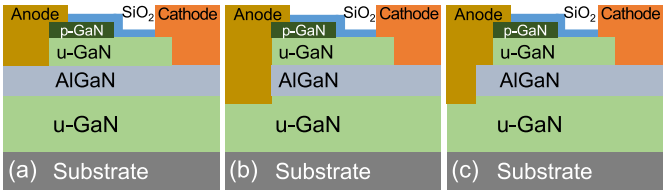

Fig. 15. (a) Cross section schematic of PSJ diode with Schottky contact on (a) AlGaN (b) 2DEG, and (c) AlGaN and 2DEG.

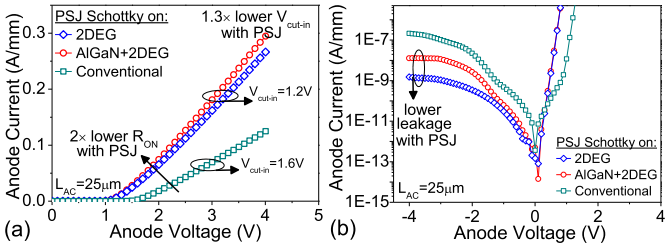

Fig. 16. (a) Comparison of DC characteristics of PSJ diodes with the conventional GaN Schottky diode in (a) forward bias region and (b) reverse bias region. PSJ diodes outperform the conventional Schottky diode.

as seen in Fig. 14(b) and (c) and highlights the thermal stress-driven failure in PSJ-FET under high current stress in ON-state. The failure analysis of PSJ-FET reveals that failure occurs in the gate region under OFF-state and in the gate–drain region under ON-state stress. Moreover, failure under OFF-state is field-driven, whereas ON-state failure is thermally driven. Fig. 14(d) shows postfailure SEM micrograph of conventional HEMT that failed under ON-state. It reveals the presence of crack, which originated from the drain-side gate edge. In AlGaN/GaN HEMT, under ON-state the hotspot and peak field residing at the drain-side gate edge induces thermal and piezoelectric strain, respectively, in gate vicinity [20] which possibly damaged the gate finger and created defects in the gate–drain region. At high drain voltage, the hot electrons get trapped in these freshly formed defects [21] and eventually caused HEMT failure.

VIII. SOA of PSJ-Schottky Diode

A. SOA Characterization PSJ-GaN Diode

Three types of diode variations were realized with 25-μm anode-cathode spacing: 1) Schottky-on AlGaN; 2) Schottky-on 2DEG; and 3) Schottky-on both AlGaN and 2DEG as depicted in schematics in Fig. 15. Cathode contact sits on AlGaN in each case. First, DC I–V and C–V characterization of diodes was done, and device parameters were extracted. Fig. 16 depicts the measured diode I–V characteristics which show the following: 1) 1.3 times lower cut-in voltage; 2) 2 times lower R_{ON}; 3) 1.5 times higher ON current; and 4) 2 orders lower leakage when compared with the conventional GaN Schottky diode. The high current capability of PSJ diode originates from the simultaneous presence of 2DHG and 2DEG unlike in conventional diode which has one 2DEG channel. The higher leakage in conventional SBD is possibly due to increased defects density during reactive ion etching of p-GaN and u-GaN layers to realize conventional SBD on the same wafer.

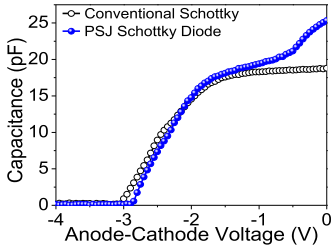

Fig. 17. Comparison of capacitance–voltage profiles of conventional Schottky diode and PSJ diode.

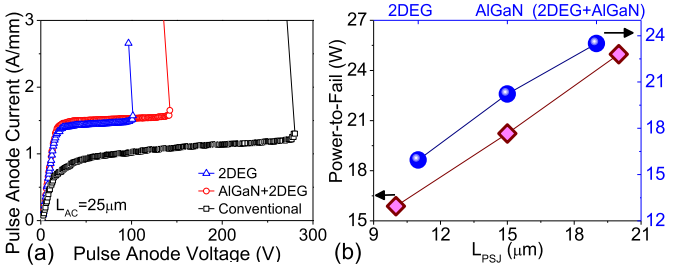

Fig. 18. (a) Comparison of pulse I–V characteristics of PSJ diode with Schottky contact on (i) 2DEG and (ii) AlGaN + 2DEG with (iii) the conventional GaN Schottky diode. (b) Variation in power-to-fail of PSJ diode with (i) the length of super-junction (red curve) and placement of Schottky contact on 2DEG or AlGaN or on both (2DEG + AlGaN).

Capacitance–voltage (C–V) characteristics of 100-μm-wide conventional Schottky and PSJ diode with the same L_{ac}, are measured at 20-kHz frequency as shown in Fig. 17. The diode depletion capacitance is integrated over voltage to determine the charge stored in the diodes during OFF-state. PSJ diode showed slightly higher stored charge (4.8×10^{-11} C) than the conventional Schottky diode (4.3×10^{-11} C). Higher charge storage in PSJ diode is attributed to the additional capacitance of the PSJ region (formed by 2DEG and 2DHG), which is present in parallel to Schottky junction capacitance.

Pulse I–V characterization of PSJ-SBD was accomplished with stress voltage applied at the anode while the cathode was grounded. Fig. 18(a) shows the pulse I–V characteristics of diodes under test. PSJ diodes showed 1.5× higher ON-current than conventional GaN Schottky diode. However, Schottky-on-2DEG diode failed around 100 V, whereas Schottky-on AlGaN/2DEG exhibited a breakdown voltage of 140 V. Conventional Schottky diode was found to offer the highest ON-state breakdown voltage (280 V). High current in PSJ diodes is attributed to the presence of dual channel (2DHG and 2DEG) in them. Next, power-to-fail (P_{FAIL}) was determined in each case and is shown in Fig. 18(b). P_{FAIL} scaled linearly with L_{PSJ}. PSJ diode with Schottky-on AlGaN/2DEG showed highest P_{FAIL} among all three diode variants. These observations highlight that SOA robustness of PSJ diode depends on the Schottky contact design and the length of super-junction in the diode drift region. However, it should be noted that the improved SOA in PSJ diode comes at the cost of higher stored charge during OFF-state (Fig. 17) as discussed earlier.

B. Trap-Induced PSJ-GaN Diode Degradation

The DC I–V and C–V characteristics were measured at regular intervals during the pulse stress test to capture the evolu-

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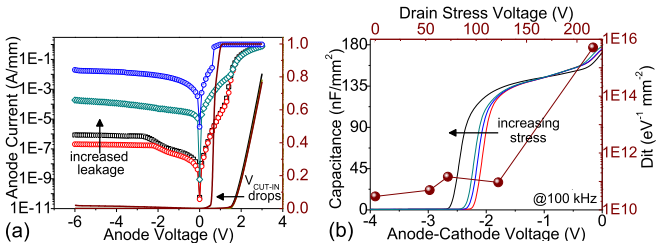

Fig. 19. (a) DC I–V characteristic of PSJ diode on log scale (left axis) and linear scale (right-axis), measured at regular interval during pulse stress. (b) Variation in diode depletion capacitance measured at 100 kHz (on left axis) and change in trap density (D_{it}) at the Schottky interface (right-axis) during stress.

tion of diode degradation. Fig. 19(a) shows the variation in DC I–V characteristic of PSJ diode with increasing stress at anode. Due to the consistent increase in reverse leakage, the Schottky junction gradually turns Ohmic. Further, the diode cut-in voltage also decreased under stress, which points to a modified Schottky interface. To verify this, depletion capacitance was measured at 100 kHz at different stress levels as shown in Fig. 19(b). A gradual change in diode capacitance with stress was observed, which possibly originates from the degraded Schottky interface. The defect density (D_{it}) at the Schottky interface increased by five orders as depicted in Fig. 19(b). These observations confirm that the Schottky interface of PSJ diode degrades under pulse stress and limits its reliability.

IX. Conclusion

SOA of PSJ-based GaN HEMT and Schottky diodes was studied. PSJ-GaN HEMT exhibited broader SOA boundary than conventional GaN HEMT. SOA robustness (power-to-fail) showed linear dependence on PSJ length. The presence of PSJ, in the drift region, mitigated current collapse and improved SOA. Unique device degradation trends and their implications on device failure, both under ON- and OFF-states, were studied. Low thermal conductivity of substrate enhanced self-heating and limited SOA boundary. OFF-state failure was attributed to gate-stack degradation while ON-state failure was thermally driven via hotspot formation at the PSJ edge. Conventional HEMT like buffer degradation was missing in PSJ-GaN HEMT. PSJ-Schottky diode outperformed conventional GaN Schottky diode in the high current regime. SOA robustness of PSJ diode nicely scaled with PSJ length. Schottky interface degraded under stress and limited the device lifetime.

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