Drain-Extended FinFET With Embedded SCR (DeFinFET-SCR) for High-Voltage ESD Protection and Self-Protected Designs

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***Abstract*— This article presents device design insights and design challenges for drain-extended FinFET devices with embedded silicon-controlled rectifier (SCR) (DeFinFET-SCR), which can be used as an electrostatic discharge (ESD) protection device and a self-protected high-voltage switch/driver for system-on-chip applications. The tradeoff between maximizing ESD robustness without hindering the transistor's operation is discussed in detail. An interplay between parasitic p-n-p turn-on and space charge modulation (SCM) is revealed, which strongly influences the strength of parasitic SCR and its turn-on efficiency during ESD and DC operations. Developed physical insights show that engineering p-n-p turn-on and onset of SCM are the key to maximize ESD robustness without causing early SCR turn-on during transistor operation. Based on new findings and developed physical insights, design guidelines have been derived for ESD robust DeFinFET-SCR.**

***Index Terms*— Drain-extended FinFET (DeFinFET), electrostatic discharge (ESD), silicon-controlled rectifier (SCR), technology computer-aided design (TCAD).**

I. Introduction

FinFET has become the driving technology in sub-22-nm nodes for low-to medium-voltage system-on-chip (SoC) applications [1]. SoCs, however, also require high-voltage (HV) device solutions for applications, such as level shifters, dc–dc converters, RF power amplifiers, line drivers, and so on, which at present is not feasible by baseline FinFET process, and require adaptation of cascoded-stacked FinFETs or newly introduced drain-extended FinFET (DeFinFET) architectures [2], [3]. While stacked designs offer a simple and effective solution for functionalities operating up to 3.3 V [4], due to numerous parasitic paths present, this approach, however, adds serious design complexities in terms of well-isolation schemes if operating voltages are required to be scaled above 3.3 V. Therefore, its extension beyond 3.3-V operation in FinFET nodes is a challenge. DeFinFETs, on the other hand, provide an easy knob to engineer its voltage handling capability well above 3.3 V. DeFinFETs, however, are highly susceptible to electrostatic discharge (ESD) like events than the stacked FinFET counterparts. In planar nodes this challenge was addressed by introducing a silicon-controlled rectifier (SCR) path in intrinsic LDMOS/DeMOS devices. This concept was named LDMOS-SCR [5], which not only can be used as HV ESD protection element but can also enable self-protected HV designs. A similar approach can also be extended to DeFinFET architectures, which, however, is missing in the literature. The extension of DeFinFET to LDMOS-SCR like concept (DeFinFET-SCR), however, is not straightforward and requires detailed explorations of issues pertaining to 1) early SCR turn-on, which potentially affects the transistor action and safe operating area [6]–[8] and 2) early DeMOS/LDMOS like failure before SCR turn-on takes place [9]. Besides, careful device engineering for optimum holding voltage and snapback current is required to enable its usage in HV circuits in self-protected fashion [10]–[12]. While addressing these conflicting design issues, for the first time, this article demonstrates ESD behavior and design guidelines for efficient DeFinFET-SCR, proposed to be used for HV ESD protection, and HV transistor in self-protected designs.

In this article, design guidelines and fundamental explorations related to inherent challenges in designing efficient DeFinFET-SCR are studied using well-calibrated 3-D technology computer-aided design (TCAD) simulations. Section II discloses the device architecture and TCAD framework used in this article. Sections III and IV present physical insights into the device operation and DeFinFET-SCR design challenges. Section V presents an interplay between space charge modulation (SCM) and parasitic p-n-p turn-on, which were found to be the key to engineer DeFinFET-SCR. These insights are used in Section VI, where device engineering guidelines to design ESD robust

Manuscript received July 15, 2019; revised September 26, 2019; accepted October 19, 2019. Date of publication November 8, 2019; date of current version November 27, 2019. This work was supported by the IMPRINT Program through the Ministry of Human Resource and Development and Department of Science and Technology, Government of India. The review of this article was arranged by Editor C. Duvvury. *(Corresponding author: Milova Paul.)*

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Digital Object Identifier 10.1109/TED.2019.2949126

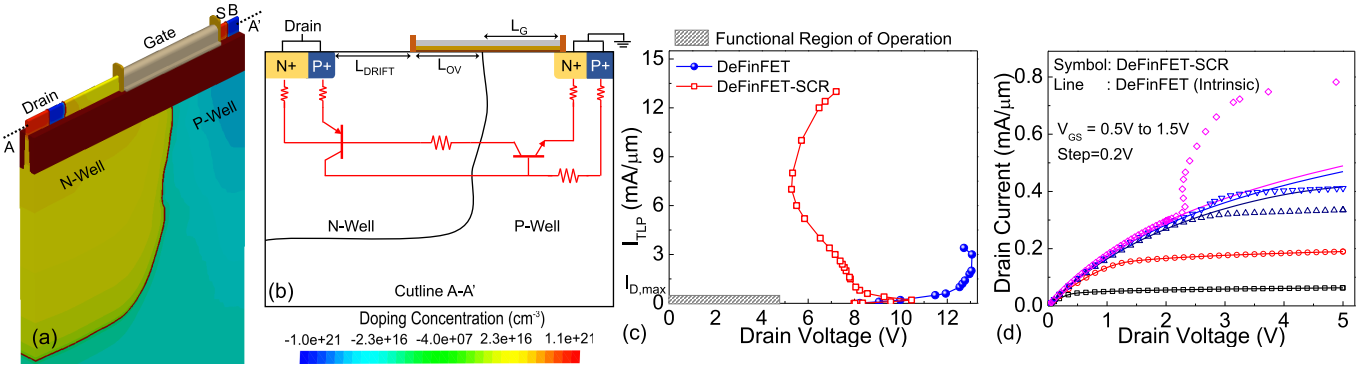

Fig. 1. (a) Isometric view of DeFinFET-SCR and (b) its cross-sectional view along the fin, showing the parasitic embedded SCR and key design parameters. (c) TLP *I–V* and (d) output characteristics of DeFinFET and DeFinFET-SCR. Here, ESD current is normalized with fin-to-fin pitch (transistor's footprint).

DeFinFET-SCRs, without causing early SCR turn-on during transistor operation are presented. The design margin for ESD robust and self-protected DeFinFET-SCR is discussed. The impact of STI placement at various locations in the drift region on the ESD robustness and dc operation of DeFinFET-SCR is discussed in Section VII. Finally, Section VIII concludes the developed findings and insights.

II. Device Architecture and TCAD Approach

Fig. 1(a) and (b) shows the isometric view of a drain-extended Fin-based SCR design and its cross-sectional view showing the parasitic SCR path, respectively. The DeFinFET-SCR design consists of cathode and anode contact regions, where the anode region consists of the drain N^+ (base of the parasitic p-n-p) and P^+ tap region (emitter of parasitic p-n-p), both diffused in N^- well. Here, the P^+ region is closer to the gate edge. The N^+ source (emitter of parasitic n-p-n) and the P^+ body (base of the parasitic n-p-n) contact constitutes the cathode region of the DeFinFET-SCR. It is worth highlighting that the explorations performed in this article are based on 3-D TCAD simulations. The simulation setup used is well calibrated with experimental results, using appropriate TCAD models and sub-14-nm-node FinFET technology parameters, as reported in our recent articles [3], [13]–[15]. Under ESD stress conditions, to account for transient self-heating effects in the device, thermal boundary conditions are taken into consideration as reported in [1] and [16]. Thermal resistances equivalent to back-end metal interconnect, and interlayer dielectric was incorporated. Transmission Line Pulse (TLP) simulations were performed using a 100-ns-wide pulse, with increasing pulse amplitude, while keeping rise time fixed to 10 ns. The same was averaged from 60 to 90 ns to extract quasi-static *I–V* characteristics.

III. Transistor Action and ESD Behavior

Fig. 1(c) compares TLP *I–V* characteristics of DeFinFET and DeFinFET-SCR. It also highlights the transistor's operational region. To enable efficient ESD protection and self-protection capabilities in the HV DeFinFET-SCR, the desired ESD characteristics need to have the following two main attributes: 1) avoiding parasitic conduction within transistor's operational window, i.e., false triggering of parasitic SCR should be strictly avoided under any given operational circumstances; and 2) DeFinFET-SCR must conduct as high as possible ESD current beyond transistor's operating window. Fig. 1(c) shows that intrinsic DeFinFET suffer from very low failure current (It2$\sim$3 mA/μm). On the other hand, DeFinFET-SCR, due to presence of embedded SCR, offers low resistive conduction path during ESD operation, which results in relatively higher It2 ($\sim$12 mA/μm). As a tradeoff, the SCR turn-on was found to affect the transistor's operation, in the form of early SCR turn-on at drain voltage below the maximum operating point when the channel was in complete inversion condition. This is shown in the dc output characteristics shown in Fig. 1(d). The abrupt increase in drain current at lower drain voltages, when channel was in complete inversion, is the signature of early SCR turn-on, which must be avoided for its usability as a self-protected transistor. The early SCR turn-on during dc operation can be attributed to conventional style of P^+ anode placement between drain N^+ region and well junction, which results in electron accumulation under P^+ region before it is collected by N^+ drain. The accumulation of electrons under P^+ region (emitter contact of parasitic p-n-p), causes early p-n-p turn-on by lowering local N-well potential, which results in an early SCR turn-on. This will be explained in detail in Sections IV and V. To understand the impact of P^+ anode placement on SCR's turn-on, a flipped version of DeFinFET-SCR has also been studied, as shown in Fig. 2(a). Here, the position of anode P^+ and the drain N^+ are swapped. This is found to suppress the early SCR turn-on, which recovers the transistor action during the operational window, as shown in the output characteristics shown in Fig. 2(b). Absence of early SCR turn-on in a flipped DeFinFET-SCR can also be seen in its transfer characteristics, which has been compared with conventional DeFinFET-SCR's transfer characteristics in Fig. 2(c). Here, for a conventional DeFinFET-SCR, a drain current collapse (i.e., gate loses channel control at the onset of parasitic conduction) is evident, which indeed is missing in a flipped DeFinFET-SCR. This, however, comes with a compromise in It2. Fig. 3 compares TLP *I–V* and temperature characteristics of both the DeFinFET-SCR variants. Here, due to compromised SCR action, a flipped DeFinFET-SCR was found to offer lower It2 and high holding voltage when compared with a conventional DeFinFET-SCR. The physics of operation under ESD

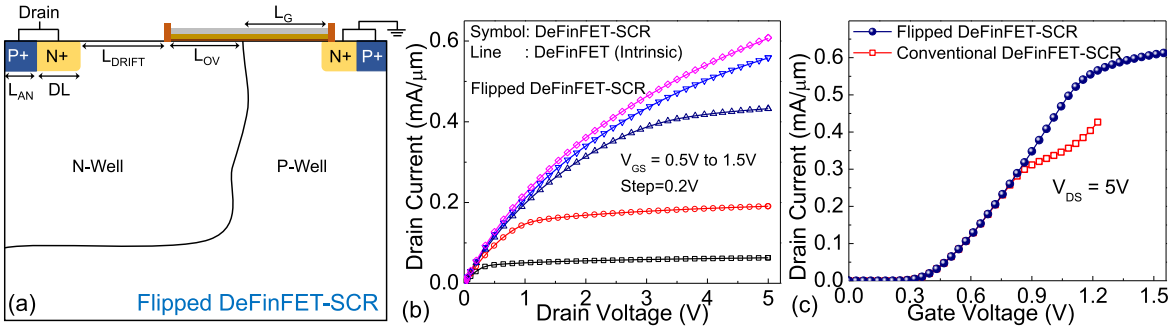

Fig. 2. (a) Cross-sectional view of the flipped variant of DeFinFET-SCR, where the drain N^+ and anode P^+ regions are swapped. Here, L_{AN} is anode's P^+ tap length, and DL is the drain N^+ length. (b) Output characteristics of flipped DeFinFET-SCR compared with intrinsic DeFinFET (of flipped DeFinFET-SCR). (c) Transfer characteristics of flipped DeFinFET-SCR compared with the conventional DeFinFET-SCR [shown in Fig. 1(a)], showing a drain current collapse in conventional DeFinFET-SCR, at higher gate voltage, which is missing in its flipped counterpart.

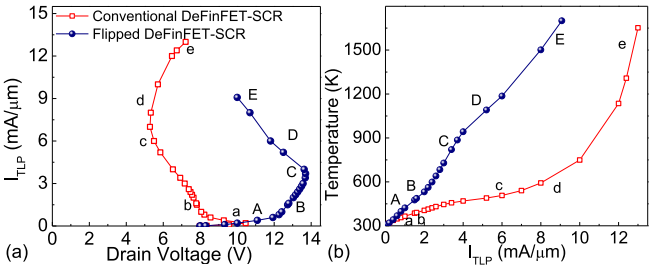

Fig. 3. (a) TLP *I–V* characteristics and (b) lattice temperature versus TLP current, compared for conventional and flipped DeFinFET-SCRs. Distinct current/injection levels (a/A–e/E) in the TLP *I–V* characteristics are marked. These levels will be used later to explain different physical events, which take place under different injection conditions.

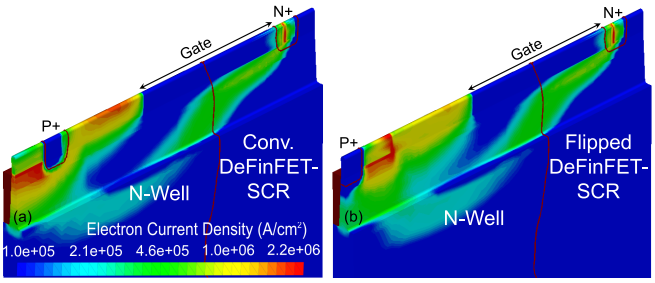

Fig. 4. Electron current density contour of (a) conventional and (b) flipped DeFinFET-SCR, for injected current (I_{TLP} = 0.4 mA/μm) marked as point "a" in the TLP *I–V* curve of Fig. 3. It shows electron accumulation under the P^+ anode region of conventional DeFinFET-SCR, which results in early p-n-p turn-on leading to early SCR turn-on. The same, however, was missing in flipped design.

condition and respective differences in the TLP characteristics will be explained in detail in subsequent sections.

IV. Physical Insights Into ESD Behavior

A. Avalanche Breakdown and Parasitic n-p-n Turn-on

With the increase in TLP stress current, the N/P-well junction gets reverse biased, which results in generation of impact ionization carriers due to high e-fields. The generated holes migrate toward the P^+ body region in the P-well. This locally increases the body potential, which triggers the parasitic n-p-n. This is shown by electron conduction through the N^+ source contact, as can be seen in Fig. 4. It is worth highlighting that the parasitic n-p-n turn-on for both the conventional and flipped DeFinFET-SCRs occurs at the same current value, i.e., at points "a"/"A" shown in the TLP *I–V* curve of Fig. 3.

B. Parasitic p-n-p and Subsequently SCR Turn-on

The generated impact ionized electrons from the reverse biased well junction flow toward the N^+ drain region, which lowers the N-well potential. This leads to parasitic p-n-p turn-on, shown by the hole conduction through P^+ anode contact, as shown in Fig. 5. The p-n-p triggering post n-p-n turn-on initiates a regenerative feedback action leading to SCR turn-on. It is worth highlighting that, the p-n-p turn-on in a conventional DeFinFET-SCR occurs at a lower stress value (point "a" in Fig. 3), when compared with the flipped DeFinFET-SCR, which requires a higher current (point "B" in Fig. 3). This can be explained as follows: since the N^+ drain region in the conventional DeFinFET-SCR is placed away from the well junction, the injected electrons accumulate under the P^+ anode region before getting collected at the N^+ drain terminal. This lowers the N-well potential without requiring very high avalanche generated excess carrier (electrons) concentration. This results in early p-n-p and subsequently SCR turn-on. This is shown using the excess hole conduction through P^+ anode contact (or the emitter of parasitic p-n-p) in Fig. 5(a). On the other hand, in the case of the flipped DeFinFET-SCR design, since the P^+ anode region is situated away from the well junction, after the drain N^+ region, the injected electrons are collected by positively biased drain terminal, before they accumulate in the N-well region below the P^+ anode region. This in-turn results in reduced excess electron concentration for a given injected ESD current when compared with the conventional DeFinFET-SCR. As a result, the flipped DeFinFET-SCR requires a higher ESD current to acquire enough excess electrons in N-well, required for parasitic p-n-p triggering (point "B" in the TLP *I–V* characteristics of Fig. 3). This is shown in Fig. 6.

C. Space Charge Modulation and Regenerative SCR Action

After the onset of SCR, increasing the TLP stress current results in space charge or conductivity modulation in the N-well region. This results in the peak electric field shift from the well junction/gate edge toward the N^+ drain contact, as shown in Fig. 7. Stronger the SCM, higher the field

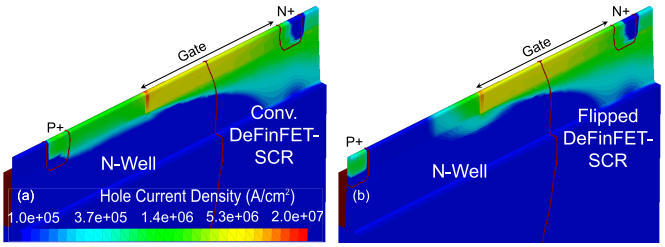

Fig. 5. Hole current density contour of (a) conventional and (b) flipped DeFinFET-SCR, for injected current (I_{TLP} = 0.4 mA/μm) marked as point "a" in the TLP *I–V* curve of Fig. 3. It shows hole current through P^+ anode in conventional DeFinFET-SCR, which validates turn-on of parasitic p-n-p causing early SCR turn-on. The same, however, was missing in flipped design at the same injected current.

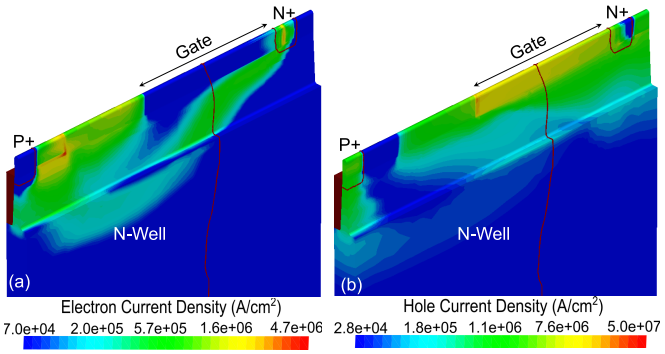

Fig. 6. (a) Electron and (b) hole current density across the flipped DeFinFET-SCR extracted at TLP current corresponding to points "A" (I_{TLP} = 0.4 mA/μm) and "B" (I_{TLP} = 1.6 mA/μm), (Fig. 3), respectively.

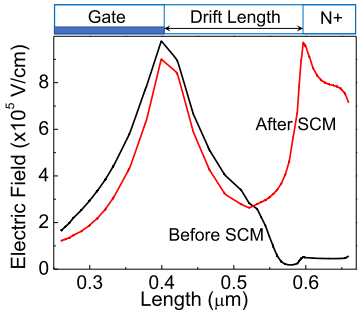

Fig. 7. Electric field profile of DeFinFET-SCR showing SCM.

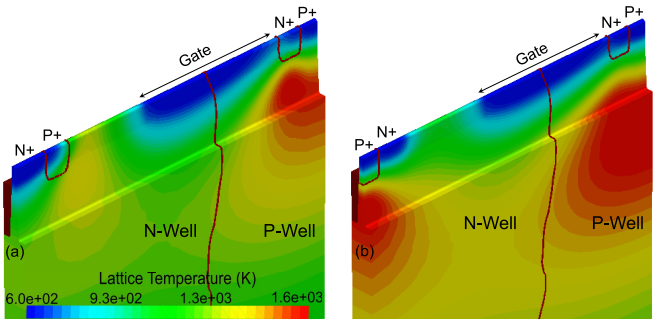

Fig. 8. Lattice temperature profile of (a) conventional and (b) flipped DeFinFET-SCR, extracted at point (e/E), i.e., at I_{TLP} = 13 mA/μm for conventional and I_{TLP} = 9 mA/μm for flipped DeFinFET-SCR, showing two localized hot spots beneath the major current carrying regions (anode P^+ and cathode N^+).

under the drain contact, and therefore, higher the excess carrier generation. This leads to a regenerative action causing stronger SCM or conductivity modulation, where 1) the strength of regenerative action depends on field localization and 2) stronger the regenerative action, deeper the snapback. It is worth noting that in the conventional DeFinFET-SCR, while SCM starts at current marked at point "b" (Fig. 3), the device experiences complete SCM at current marked at point "d" (Fig. 3). On the other hand, in the flipped DeFinFET-SCR, the onset of SCM takes place at point "C" (Fig. 3), whereas the regenerative actions continues till current at point "E" (Fig. 3). It should be noted that current at point "b" $<$ current at point "C" and current at point "d" $\sim$ current at point "E." The early onset of SCM in the conventional DeFinFET-SCR is due to stronger localization of current under the N^+ drain contact. In the conventional DeFinFET-SCR, since P^+ anode contact, in the drift region, is placed before N^+ drain, it does not experience lateral electron conduction near N^+ drain contact [Fig. 4(a)]. This gives rise to electron concentration under N^+ drain contact, which causes early SCM. On the other hand, since in the flipped DeFinFET-SCR, N^+ drain contact collects carriers both laterally and vertically [Fig. 4(b)], this device experiences lower current density near N^+ drain contact. This delays the onset of SCM and subsequent regenerative action [12], [17], [18] in flipped designs. Besides, weaker SCM in the flipped DeFinFET-SCR results in higher holding voltage, when compared with the conventional DeFinFET-SCR. Moreover, since the onset of SCM strongly depends on the electron current density below drain contact, it is also worth highlighting that onset of SCM strongly depends on placement of drain contact and drain length (DL). It was found that the peak e-field lowers below N^+ drain contact when DL was increased in the conventional DeFinFET-SCR. This delays the onset of SCM, which is attributed to reduced current density, below N^+ drain contact, with increased DL. In the case of the flipped DeFinFET-SCR, the DL does not change onset of SCM significantly due to dominant lateral electron conduction. The implications of DL engineering on the ESD and dc behavior of the flipped and conventional DeFinFET-SCRs are discussed later.

D. Device Failure

Fig. 8 shows self-heating behavior (lattice temperature profile extracted close to It2) of both the conventional and flipped DeFinFET-SCRs. With complete SCR turn-on and conductivity modulation of well, most current flows between P^+ anode and N^+ source. Attributed to SCM, a high-field region exists under these regions. This is due to the accumulation of minority carriers in these regions, which are responsible for SCR turn-on and subsequent high current conduction. As a result, due to the localized high field under N^+ source and P^+ Anode, at high injected currents, device experiences two hot spots, one under the anode region and the other at the source side. These lead to device self-heating and failure. This behavior correlates well with an earlier article [19]. It should be noted that, in the conventional DeFinFET-SCR, as the P^+ anode region is placed before the N^+ drain, it experiences lateral current conduction. This results in relaxed heating under the anode contact [Fig. 8(a)]. On the other hand, due to the

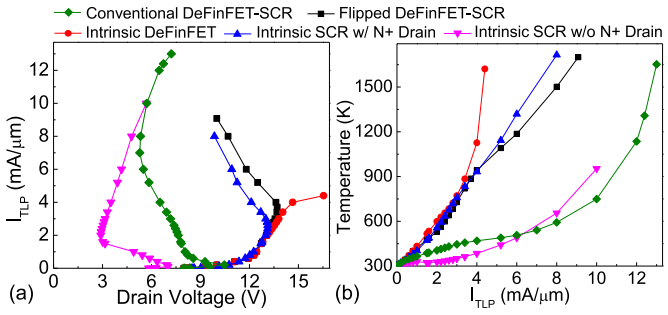

Fig. 9. (a) TLP *I–V* characteristics and (b) lattice temperature profile of DeFinFET-SCR, flipped DeFinFET-SCR, and their unique parasitic counterparts.

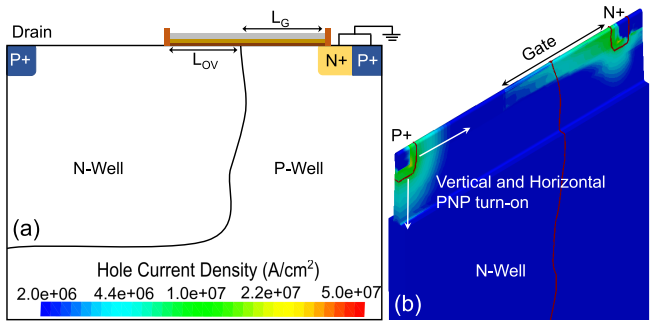

Fig. 10. (a) Cross-sectional view of Intrinsic SCR (without N^+ drain) embedded in DeFinFET-SCR. (b) Hole current density contour showing p-n-p turn-on, which triggers parasitic SCR.

placement of N^+ drain between the drain region and P^+ anode, the flipped DeFinFET-SCR experiences a dominant vertical current conduction. This leads to current localization into the narrow vertical path, which causes hot spot formation and increased lattice heating [Fig. 8(b)] compared with the conventional device.

V. What Else Affects SCM and Regenerative SCR Turn-on?

While on the one hand, the SCR must not trigger early to avoid functional failure in self-protected concepts; it must trigger efficiently at currents higher than the transistor's drive current and offer lower holding voltage and higher It2. Therefore, the device must be engineered to control the SCR strength. As discussedearlier, since SCM plays a strong role in defining the strength of regenerative SCR action, it is worth exploring aspects affecting SCM and resulting regenerative SCR turn-on. Keeping this in mind, following additional variants of the DeFinFET-SCR were studied: 1) the flipped DeFinFET-SCR having P^+ anode floating; 2) the flipped DeFinFET-SCR having N^+ drain floating; and 3) the DeFinFET-SCR without N^+ drain. The same has been compared with TLP *I–V* characteristics of the flipped DeFinFET-SCR and the conventional DeFinFET-SCR, as shown in Fig. 9, which also shows that keeping the P^+ anode in floating condition (Intrinsic DeFinFET) results in TLP characteristics equivalent to DeFinFET's TLP characteristics. The DeFinFET studied in Fig. 1(c) shows SCM assisted snapback. However, in the case of the flipped DeFinFET-SCR, since N^+ drain contact collects carriers both laterally and vertically [Fig. 4(b)], it experiences lower current density near N^+ drain contact, which delays the onset of SCM. Furthermore, keeping the N^+ drain floating (intrinsic SCR w/ N^+ drain) does not make a significant difference in SCR action, as shown by its TLP characteristics, which follows characteristics of flipped DeFinFET-SCR. This could be attributed to excess carrier recombination at the butted N^+/P^+ junction. On the other hand, when N^+ drain contact was removed (intrinsic SCR without N^+ drain), the device shows significantly improved SCR action with the deepest snapback. In this case, the device with N^+ contact has deeper snapback than the conventional DeFinFET-SCR. This is explained in Fig. 10, which shows hole conduction in both the lateral and vertical directions,

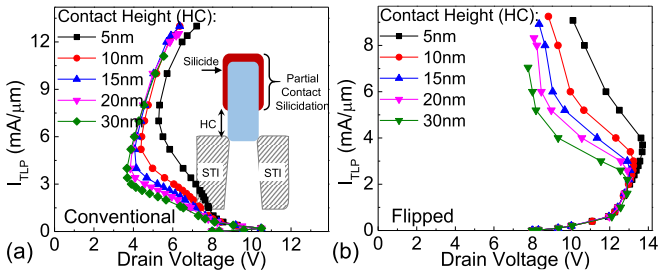

Fig. 11. TLP *I–V* characteristics of (a) conventional and (b) flipped DeFinFET-SCR, as a function of HC. Inset: schematic view of partial contact silicidation, shown by contact height (HC > 0).

i.e., both vertical and lateral p-n-p conductions resulting in additional (vertical) SCR conduction path. It should be noted that in the conventional DeFinFET-SCR hole conduction was predominantly lateral [Fig. 5(a)], whereas in flipped device it followed a vertical path [Fig. 6(b)]. This also affects SCR's current conduction path and thereby the onset of SCM.

VI. DeFinFET-SCRs: Engineering Guidelines

We have seen that parasitic p-n-p turn-on, onset of SCM and their interplay defines the strength of regenerative SCR action. Therefore, the challenge in the DeFinFET-SCR design is to avoid early p-n-p turn-on and engineer device for the right onset of SCM. In the conventional DeFinFET-SCR, it is required to increase the SCR trigger current and holding voltage, whereas in flipped configuration, it is required to lower the SCR trigger current and holding voltage. In this section, we will address this by various device design parameters.

A. Contact Height

Inset of Fig. 11(a) demonstrates a scheme for partial contact silicidation over the fin, which was earlier discussed in detail in [13] and [14]. It was shown that partial contact silicidation (HC > 0) improves the bipolar efficiency by mitigating excess carrier recombination at the junction, which in-turn improves the SCR turn-on. The same can be deployed here. Fig. 11 shows that increasing contact height (HC) improves SCR action (deeper snapback). It should, however, be noted that HC plays no role in defining onset of SCM, and therefore, the onset of SCM does not change as a function of HC. Attributed to

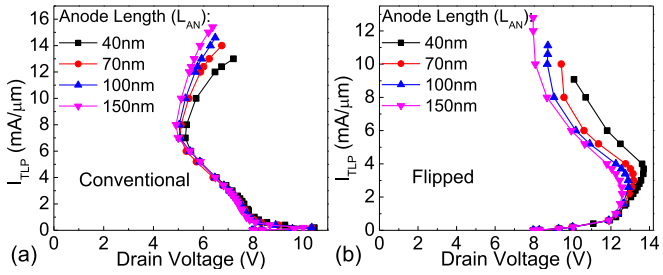

Fig. 12. TLP *I–V* characteristics of (a) conventional and (b) flipped DeFinFET-SCR, as a function of anode P^+ length (L_{AN}).

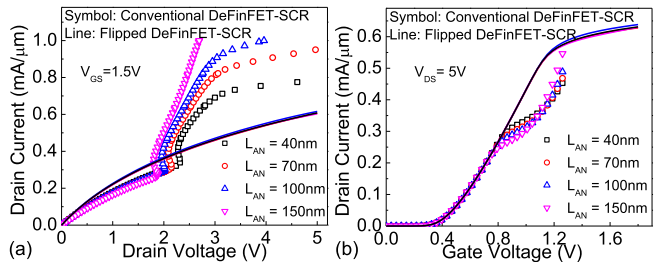

Fig. 13. (a) I_D–V_D and (b) I_D–V_G characteristics conventional (symbol) and flipped DeFinFET-SCR (line), as a function of anode length (L_{AN}).

this, while the snapback depth increases, the current required for snapback does not change.

B. Anode Length (L_{AN})

The turn-on efficiency of p-n-p can also be improved by increasing the p-n-p's emitter junction area, which is the length of the anode P^+ region (L_{AN}). Fig. 12(a) shows that conventional DeFinFET-SCR does not experience any improvement in snapback depth/holding voltage, attributed to dominating lateral p-n-p turn-on, which is independent of L_{AN}. It, however, improves It2 and on-resistance due to relaxed self-heating at the anode side. On the other hand, Fig. 12(b) shows that the flipped DeFinFET-SCR experiences noticeable improvement in SCR turn-on/snapback depth and holding voltage, which is due improved vertical conduction of parasitic p-n-p. Moreover, the It2 was found to improve, which is due to relaxed self-heating at the anode side. It should be noted that the onset of SCM, and therefore, snapback does not change by changing L_{AN}. Moreover, as shown in Fig. 13, early SCR turn-on by increasing L_{AN} further compromises the transistor characteristics of conventional DeFinFET-SCR. However, increasing L_{AN} does not affect the transistor action of the flipped variant, which makes the flipped DeFinFET-SCR a potential option for self-protected HV applications.

C. Drain Length

It was earlier presented that DL significantly affects SCM in HV drain-extended MOS devices [9], [12], [17], [18]. Like DeMOS, in DeFinFET-SCR, increasing DL shifts the onset of SCM to higher currents and weakens the SCR strength. Therefore, it is worth investigating the impact of DL on DeFinFET-SCR's TLP characteristics. As shown in Fig. 14, delayed SCM by increasing DL mitigated the strength of SCR turn-on, and therefore, snapback depth and the holding voltage

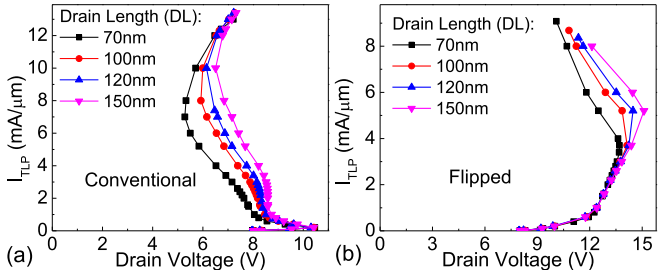

Fig. 14. TLP *I–V* characteristics of (a) conventional and (b) flipped DeFinFET-SCR, as a function of N^+ DL.

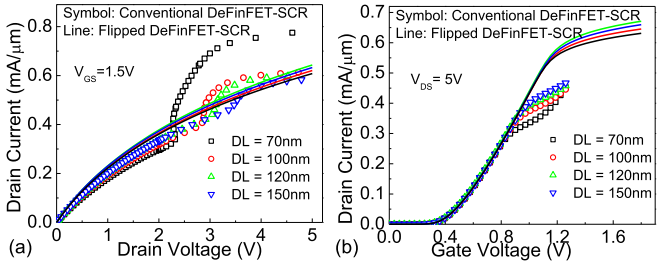

Fig. 15. (a) I_D–V_D and (b) I_D–V_G characteristics of conventional (symbol) and flipped DeFinFET-SCR (line), as a function of DL.

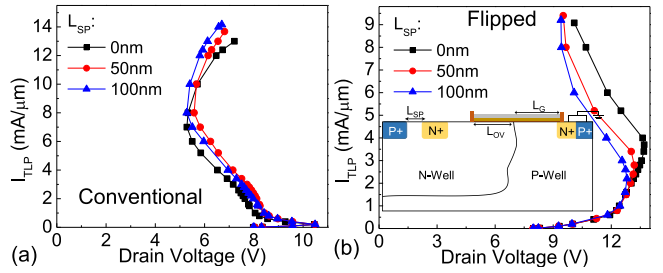

Fig. 16. Inset: TLP *I–V* characteristics plotting the effect of anode-to-drain spacing (L_{SP}), for (a) conventional and (b) flipped DeFinFET-SCRs.

of both the DeFinFET-SCR designs. The impact of DL on SCM is higher in the conventional DeFinFET-SCR due to vertical electron current conduction around N^+ drain, when compared with the flipped DeFinFET-SCR, which experiences primarily lateral current conduction around N^+ drain. This leads to a higher positive shift in holding voltage by increasing DL in conventional DeFinFET-SCR [Fig. 14(a)], when compared with holding voltage shift in the flipped DeFinFET-SCR [Fig. 14(b)]. Furthermore, as shown in Fig. 15, delayed SCM by increasing DL recovers the transistor characteristics of conventional DeFinFET-SCR by delaying SCR turn-on. This makes the conventional DeFinFET-SCR, with DL engineering, a potential option for self-protected HV applications.

D. P^+ Anode to N^+ Drain Spacing (L_{SP})

We have seen earlier that the butted nature of N^+ and P^+ contacts in DeFinFET-SCRs causes weaker SCR action. Therefore, it is worth investigating the impact of spacing between N^+ and P^+ contacts/diffusions. Fig. 16 shows TLP *I–V* characteristics of conventional and flipped DeFinFET-SCRs with increasing N^+ and P^+ contact spacing (L_{SP}). Separating N^+ contact away from P^+ anode in the flipped

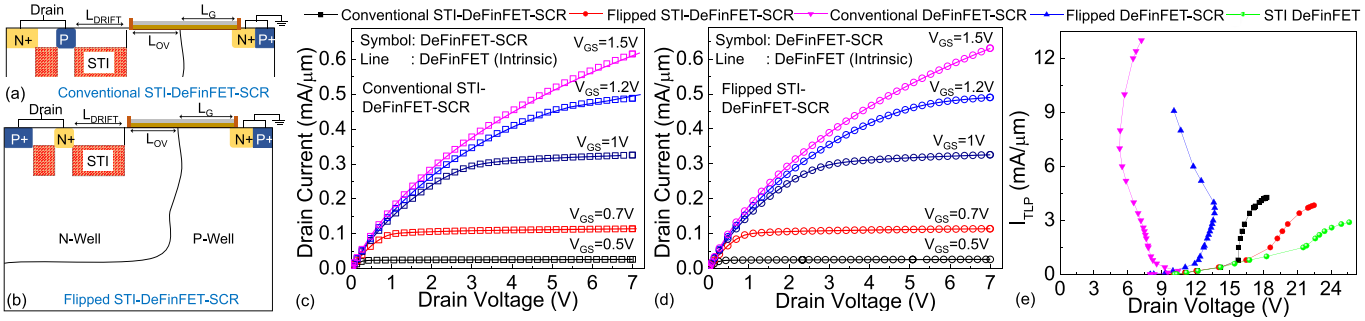

Fig. 17. (a) and (b) Schematic view of STI-based DeFinFET-SCR to enable high operating voltage compared with non-STI variants discussed so far. (c) and (d) Output characteristics of STI DeFinFET-SCR in conventional and flipped configurations, respectively, showing absence of early SCR turn-on within the transistor's operational region. (e) TLP *I*–*V* characteristics of DeFinFET-SCR variants compared with STI DeFinFET-SCR variants.

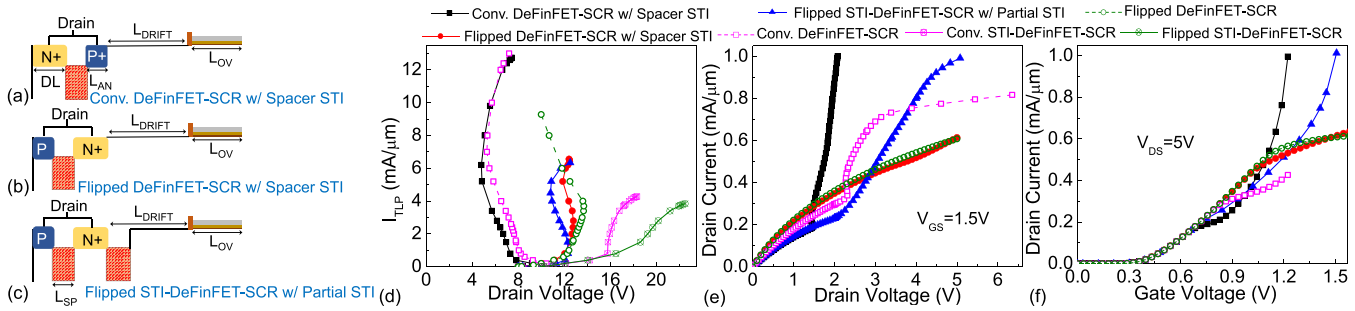

Fig. 18. (a)–(c) Design variants of STI-based DeFinFET-SCR to study impact of STI placement on DeFinFET-SCR's TLP and dc characteristics. (d)–(f) TLP *I*–*V*, output, and input characteristics of various design variants of STI-based DeFinFET-SCRs, respectively.

DeFinFET-SCR, strengthens the p-n-p turn-on, by enabling the lateral p-n-p conduction. This causes early SCR turn-on and relatively deeper snapback/lower holding voltage when compared with butted contact ($L_{SP} = 0$ nm). On the other hand, in the conventional DeFinFET-SCR, due to dominant lateral p-n-p conduction, increasing L_{SP} does not change the p-n-p (and therefore, SCR) turn-on strength, which results in unchanged snapback depth and holding voltage.

VII. STI-Based DeFinFET-SCR

Having explored design possibilities of non-STI variants of DeFinFET-SCRs, it is worth studying the feasibility of STI-based DeFinFET-SCRs too for self-protected HV applications. STI in DeFinFET's drift region is typically used to increase its voltage handling capability, i.e., to increase its avalanche breakdown voltage [9], [12]. In the case of DeFinFET-SCR, various schemes to place STI between N^+ drain and drift region or N^+ drain and P^+ anode, as shown in Fig. 17(a) and (b) and in Fig. 18(a)–(c), are possible. Fig. 17(c) and (d) shows output characteristics of both conventional and flipped variants of STI-DeFinFET-SCR. Clear transistor's saturation characteristics can be observed without any interference from parasitic SCR like action earlier seen for conventional non-STI variants. This is attributed to relatively poor SCR efficiency due to compromised parasitic p-n-p gain after deploying STI in the drift region, which is evident from Fig. 17(e), showing TLP *I*–*V* characteristics of STI variants. TLP characteristics show missing SCR turn-on or snapback, which results in lower It2 when compared with non-STI variants. It should also be noted that placement of STI confines the current conduction into vertical direction, limited by spacing between STI, which results in increased self-heating in the device at drain/anode side, causing further reduction in It2. The It2, however, is relatively better when compared with It2 of intrinsic DeFinFET (without embedded SCR), which shows advantage of integrating parasitic SCR with DeFinFET for self-protected HV applications. The SCR efficiency, and therefore, It2 of STI variants can be improved further, without hindering transistor's intrinsic performance, by using design guidelines presented in previous sections for non-STI variants.

Furthermore, since the placement of STI affects parasitic SCR's turn-on, it is worth studying impact of unique variants of STI placement in the drift region, which are shown in Fig. 18(a)–(c). TLP and dc *I*–*V* characteristics presented in Fig. 18(d)–(f) show the following.

1) Removing STI from the drift region while keeping it in-between N^+ drain and P^+ anode [Fig. 18(a)] improves the SCR turn-on efficiency and makes it relatively better than the conventional non-STI DeFinFET-SCR. This is attributed to isolation created between P^+ anode and N^+ drain, by STI, which improves p-n-p turn-on resulting in a deeper snapback. On the other hand, it results in serious interference with transistor's intrinsic behavior causing early SCR turn-on at very low drain voltages under dc conditions. This can be mitigated by increasing DL and/or partially covering drift region (region between gate edge and drain diffusion) by STI [as used in Fig. 18(c)].

2) The issues related to early SCR turn-on during dc operation, as shown in the previous case, was missing in a flipped configuration having no STI in the drift region while keeping STI in-between N^+ drain and P^+ anode [Fig. 18(b)]. On the other hand, the ESD failure threshold was found to be compromised below It2 of the flipped non-STI DeFinFET-SCR, which is attributed to increased self-heating caused by confined current conduction, under P^+ Anode, through STI. This can be addressed by increasing the anode length (L_{AN}) until it does not hinder the dc operation.
3) Partial insertion of STI in the drift region, in flipped configuration, while keeping STI in-between N^+ drain and P^+ anode [Fig. 18(c)] makes the situation even worse by: 1) increasing transistor's on-resistance; 2) causing early SCR turn-on during dc operation; and 3) without improving It2. Early SCR turn-on is attributed to early onset of SCM caused by confined current flow through STI region below N^+ drain. This can be addressed by increasing DL. Poor It2, when compared with the flipped non-STI DeFinFET-SCR is attributed to increased self-heating caused by confined current conduction, under P^+ Anode, through STI. This can be addressed by increasing the anode length (L_{AN}) until it does not hinder the dc operation.

VIII. Conclusion

Design feasibility for DeFinFET-SCR has been presented, using detailed 3-D TCAD simulations, for HV ESD and self-protected applications. Physical insights into the SCR action during both ESD and transistor operation has been presented. For the first time, guidelines to design ESD robust DeFinFET-SCR, without hindering intrinsic transistor operation, have been presented. An interplay between parasitic p-n-p turn-on and onset of SCM was discussed, which decides the onset of parasitic SCR turn-on. It was found that engineering the onset of SCM and parasitic p-n-p turn-on were the key to design ESD robust DeFinFET-SCR for self-protected applications. This can be engineered by tuning device design/layout parameters such as DL, L_{AN}, and length/spacing between N^+ drain and P^+ anode regions (L_{SP}). It is shown that, in general, the DeFinFET-SCR can offer higher ESD robustness, when compared with DeFinFET. However, transistor operation, particularly in the case of a conventional DeFinFET-SCR, was found to be seriously affected by early SCR turn-on, causing a tradeoff between ESD robustness and keeping transistor action intact. This can be mitigated by flipping the placement of anode P^+ and drain N^+ regions, or by inserting STI in the drift region. The flipped design was found to have lower ESD robustness when compared with the conventional design, which is due to weaker SCR action. Moreover, STI-based devices were found to have lower ESD robustness when compared with non-STI devices, which is attributed to poor SCR turn-on and confined current conduction resulting in higher self-heating. On the other hand, unlike conventional DeFinFET-SCR, flipped design and STI-based devices were not affected by early SCR turn-on during dc operation of intrinsic DeFinFET.

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