Selective Electron or Hole Conduction in Tungsten Diselenide (WSe_2) Field-Effect Transistors by Sulfur-Assisted Metal-Induced Gap State Engineering

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***Abstract*— For semiconductor industry to replace silicon CMOS integrated circuits by 2-D semiconductors or transition metal dichalcogenides (TMDs), TMD-based n-FETs as well as p-FETs having performance better than Si FETs are a must. While a lot of literature demonstrates n-channel characteristics, the major roadblocks in the realization of TMD-based CMOS integrated circuit are the lack of approach to realize p-channel transistors having performance comparable to n-channel transistors, all realized over the same TMD substrate. To address this, we propose a new technique by engineering WSe_2/metal interface to realize WSe_2-based high-performance p- and n-channel transistors and therefore unveil its potential toward CMOS-integrated technology. The technique involves a dry process, based on the chemistry between the sulfur atom and WSe_2 surface, that induces unique metal-induced gap states in the source/drain (S/D) contact area, which causes improved hole (electron) injection when Cr (Ni) as S/D metal was used. This has enabled the controlled realization of high-performance WSe_2 FETs with desired polarity (N, P, or ambipolar), which solely depends on the contact metal used and contact engineering (CE)/surface engineering. Fundamental investigations on the effect of the proposed CE on metal–WSe_2 interface revealed interesting and counter-intuitive facts, which very well corroborate with experimental observations.**

***Index Terms*— CMOS integrated circuits, FET, metal-induced gap states (MIGSs), tungsten diselenide (WSe_2).**

I. Introduction

THE 2-D transition metal dichalcogenides (TMDs) [1] are “beyond graphene” 2-D materials with finite nonzero bandgap. This property along with the atomically thin surface of 2-D TMDs makes them indispensable for replacement of Si for sub-3-nm CMOS applications [2]. In order to establish a 2-D material-specific transistor technology for CMOS logic applications, it is of prime importance that both n- and p-type FETs exist over the same substrate with comparable performance. For 2-D materials, the absence of a tunable and CMOS compatible doping technique is a bottleneck in unveiling their full technological potential [3]. The polarity of 2-D TMD FET relies on the position at which the metal Fermi level pins when contacted with the TMD surface. Usually, surface defects in TMDs manifest themselves in band structure as energy states within the bandgap. For example, S vacancies in MoS_2 and WS_2 surfaces lead to bandgap states lying closer to the conduction band minimum (CBM) [4]. As a result, the metal Fermi level is strongly pinned closer to the conduction band, thereby facilitating electron conduction across the contact. This is a strong reason for the observed unipolar electron conduction or n-type behavior in MoS_2 and WS_2 FETs, irrespective of the metal work function [5]. Unlike MoS_2 and WS_2, $MoSe_2$ and WSe_2 FETs exhibit ambipolar transistor behavior, which is attributed to a smaller bandgap and Fermi-level pinning (FLP) at the midgap energy level, respectively [6]. Still, in earlier works, the hole current reported was not significantly high. Besides, ambipolar conduction deteriorates the OFF-state characteristics of the device. For CMOS integration, the realization of unipolar n- and p-type FETs on the same material is preferred over ambipolar FETs, which ensures that the device metrics, such as leakage current, threshold voltage (V_T), and ON-to-OFF current ratio (I_{ON}/I_{OFF}), or circuit metrics, such as noise margin and static power loss, do not deteriorate.To address this, a few groups performed theoretical or computational investigations to study the effect of possible dopants for 2-D materials to engineer the polarity [7]–[9]. However, experimental demonstrations to achieve polarity control in 2-D TMD FETs are rare [10], [11]. A few techniques involve doping during the growth process and others involve in the wet chemical process that leads to surface charge transfer to facilitate an increase in the specific carrier (electron or hole) concentration. Besides, electrostatic doping has proved to be another remarkable technique to realize the CMOS performance in WSe_2 without achieving unipolar FETs [12]. In this article, we introduce a

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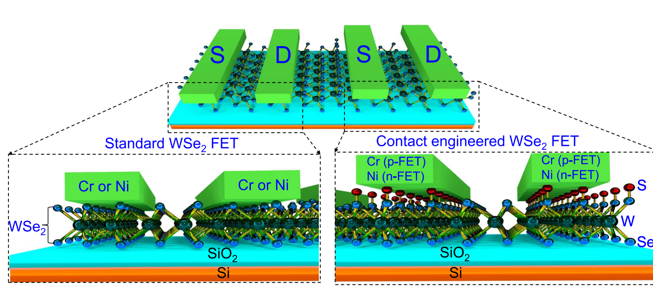

Fig. 1. Schematic of standard and H_2S-assisted S treated contact engineered WSe_2 FETs.

unique sulfur-based dry process that has enabled the controlled realization of n-channel FETs and p-channel FETs, with high performance, using the WSe_2 channel.

II. Experimental Framework and Validation

Fig. 1 shows the schematic of the proposed contact configuration (contact engineered) with introduced sulfur (S) atom in between source/drain (S/D) metal and WSe_2. The same has been compared with the standard contact configuration. To introduce S atom between S/D metal and WSe_2, exfoliated WSe_2 layers (exfoliated on top of a 90-nm thermally grown SiO_2 over p^{++}-doped Si substrate) were exposed to H_2S at 350 °C inside a chemical vapor deposition (CVD) chamber before the S/D metal deposition. H_2S is widely used as the source of sulfur (S) in CVD of S-based TMDs. The primary reason to use H_2S is that it decomposes on the surface of TMD surfaces [13] at lower temperatures and releases S. The mechanism of surface adsorption and subsequent addition of S atoms on the TMD surface is as follows. H_2S partially breaks down at 350 °C on top of MoS_2 by first getting adsorbed at sites close to S vacancies and subsequent detachment of H_2 from the surface leaving behind S on top of TMD surface at thermodynamically favorable sites. In order to remove S from the surface, a subsequent catalytic step is involved, as discussed in [13]. WSe_2 is another TMD and is expected to have a similar surface dynamics as MoS_2. Moreover, the electronegativity difference between S and Se is expected to help S to adsorb better on the surface of WSe_2. This is the motivation behind exposing a nonsulfur TMD with H_2S. The process followed in this article involves only the first step that is a low-temperature exposure of WSe_2 (at 350 °C) at the certain vapor pressure of carrier gas and flow rate of H_2S. Fig. 2 shows a general mechanism of H_2S decomposition on the surface of TMD (S- or Se-based). It is shown that S gets adsorbed on the TMD surface and can go to a thermodynamically favorable lattice site (discussed in the subsequent section). Before presenting the subsequent process steps, it is worth highlighting chemical changes introduced by the S treatment of WSe_2 by using X-ray photoelectron spectroscopy (XPS), as shown in Fig. 3. The following observations and resulting conclusion can be derived from the XPS spectra.

1) Presence of S orbital's 2p peaks in treated flakes that were otherwise missing in pristine WSe_2 samples. This confirms the incorporation of S atom over WSe_2 surface.

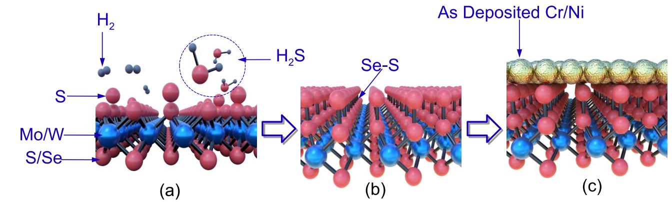

Fig. 2. Decomposition of H_2S on the surface of TMD at lower temperature followed by metal deposition. (a) Schematic of TMD surface in H2S environment. (b) Adsorption of S on the surface of the TMD. (c) Presence of S impurities at the TMD surface after metal deposition.

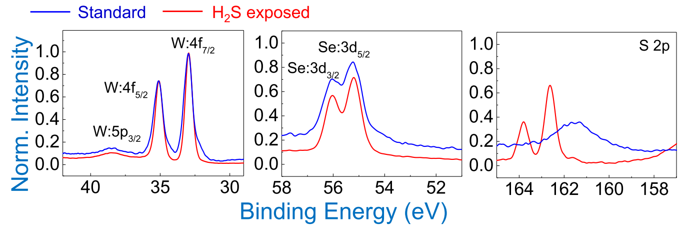

Fig. 3. XPS spectra of WSe_2 before and after H_2S-assisted S treatment.

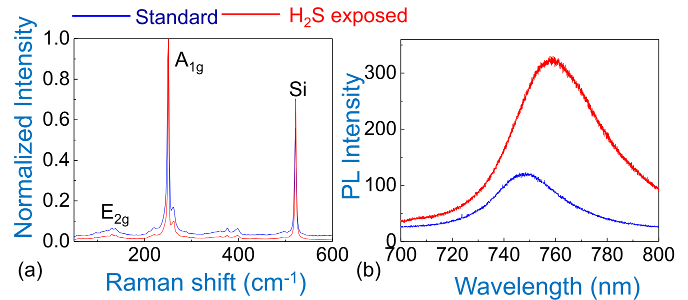

Fig. 4. (a) Raman and (b) PL spectra of WSe_2 before and after H_2S-assisted S treatment.

2) Lowering of shoulders around W-5p and 4p peaks along with those around Se-3d peaks. Lowering of shoulders close to the peaks is often attributed to reduced defect density.

In order to ensure that such a treatment does not drastically change the fundamental molecular structure of WSe_2, Raman and photoluminescence (PL) spectra are captured before and after the H_2S exposure, as shown in Fig. 4. The presence of the E_{1g} and A_{2g} peaks implies that the fundamental molecular structure, which causes the corresponding Raman active modes in WSe_2, is intact postexposure. A redshift is observed in the Raman spectra after exposure, which corresponds to the change in bond length due to added S over the WSe_2 crystal [14]. Moreover, a shift and spread in PL spectra, observed postexposure, implies the introduction of new states. Besides, a significant increase in the intensity of PL spectra implies a higher density of states (DOS) of introduced states postexposure when compared with DOS at valance band edge (VBM).

III. Device Characterization and Observations

Impact of S at the WSe_2–metal interface (engineered contact) is explored by fabricating FETs using the standard scotch tape method. The developed process flow is shown

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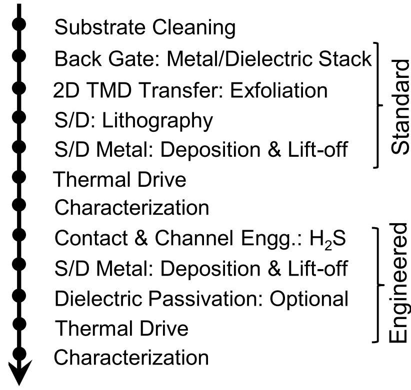

Fig. 5. Fabrication process flow for standard and engineered FETs.

in Fig. 5. Here, WSe_2 (from 2D Semiconductors) flakes (5–6 nm verified using optical microscope) are exfoliated on top of a 90-nm thermally grown SiO_2 on p^{++}-doped Si substrate. Electron beam lithography is used to pattern the S/D contact regions that are subsequently exposed inside an electron beam evaporator to deposit the desired metal stack (Ni/Au or Cr/Au) of thickness 5/50 nm. Liftoff followed by 200 °C thermal anneal step is performed to complete the fabrication of standard (without H_2S exposure) back-gated WSe_2 FETs with channel length (L_{CH}) = 1 μm. During the fabrication process, the channel region was masked by 15-nm Al_2O_3 for both standard and contact-engineered devices. These FETs are then electrically characterized inside a vacuum probe station at room temperature. In order to quantify the effect of H_2S exposure on the device behavior, the data are compared before and after H_2S exposure. It is worth mentioning that the same uniformly thick flake is used to fabricate contact-engineered (exposed to H_2S) FETs by patterning the S/D regions on the unprocessed portion of the same flake that is used to fabricate the standard FETs. This is done to eliminate variability due to varying flake thicknesses across different flakes. Next, the samples are loaded inside a furnace kept at 350 °C with a H_2S partial pressure of 20 torr after which the contact-engineered FETs are fabricated by following the exact same process as discussed earlier.

For standard devices, with Ni contact, ON current of n-FET ($I_{ON_{n\text{-FET}}}$) was found to be 8.5 μA/μm, whereas the same for p-FET ($I_{ON_{p\text{-FET}}}$) was 130 pA/μm. In case of Cr contact in a standard device, $I_{ON_{n\text{-FET}}}$ was found to be 5.8 μA/μm, whereas $I_{ON_{p\text{-FET}}}$ was 50 pA/μm. These trends depict a dominant n-channel conduction with marginal (50–100× lower) p-channel conduction, independent of S/D contact metal used in case of standard devices, which is consistent with the previous reports [15]. On the other hand, post-contact engineering (CE) 12× improvement in n-channel conduction ($I_{ON_{n\text{-FET}}}$ = 112 μA/μm), in case of Ni contacts and significantly enhanced (2100×) p-channel conduction in case of Cr devices ($I_{ON_{p\text{-FET}}}$ = 105 μA/μm), was found (see Fig. 6). At the same time, p-channel conduction in Ni devices was negligibly changed ($I_{ON_{p\text{-FET}}}$ = 1.35 μA/μm), whereas n-channel conduction in Cr devices was suppressed ($I_{ON_{n\text{-FET}}}$ = 2.1 μA/μm).

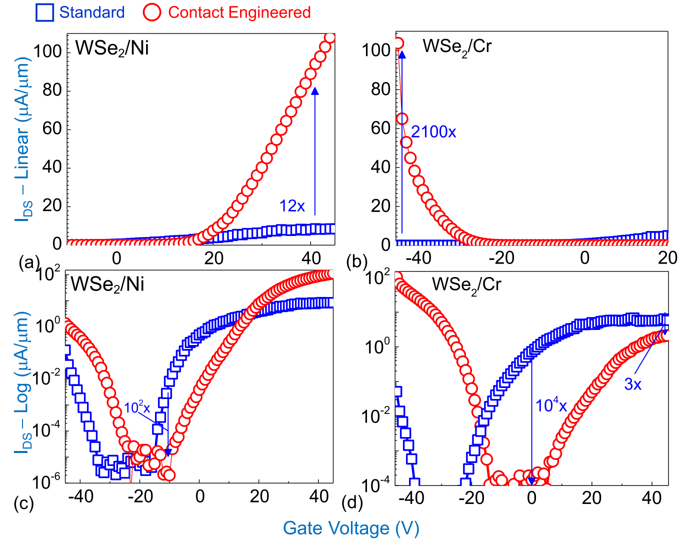

Fig. 6. Transfer characteristics of WSe_2 FETs before and after H_2S-assisted CE with (a) Ni and (b) Cr S/D contact. (c) Current of (a) shown in log scale. (d) Current of (b) shown in log scale. Here, channel length (L_{CH}) is 1 μm, gate oxide thickness (T_{ox}) is 90 nm, and drain voltage (V_{DS}) is 4 V.

Fig. 7(a) and (b) compares the contact resistance (R_C) of WSe_2 FETs, extracted using the Y-function method [16] with and without S introduction while using Ni and Cr S/D contact, respectively. To extract contact resistance, the following formula was used [16]:

$$R_C = \frac{s_2}{s_1} V_{DS} \tag{1}$$

where

$$s_1 = \frac{dY_0}{dV_g}; \quad s_2 = \frac{dY}{dV_g} \tag{2}$$

$$Y_0 = \frac{1}{\sqrt{g_m}}; \quad Y = \frac{I_{DS}}{\sqrt{g_m}} \tag{3}$$

g_m (transconductance) and I_{DS} (drain-to-source current) are measured from the transfer characteristics obtained experimentally.

In post-CE, the contact resistance of Ni devices, for electron conduction, was found to reduce from 500 Ω-μm (without CE) to 50 Ω-μm (with CE). The same, however, for hole conduction with Ni contact remains in the range of 10–50 kΩ-μm. Similarly, the contact resistance of Cr devices, for hole conduction, was found to reduce from 800 KΩ-μm (without CE) to 100 Ω-μm (with CE). In this case, R_C for electron conduction increased from 1 to 10 kΩ-μm in post-CE.

Significant reduction in contact resistance and its ohmic nature is further confirmed from the output characteristics, as shown in Fig. 8. It shows a linear rise in current at low-drain voltages when contact treatment was used. The same, however, shows the Schottky nature in case of standard contacts. It should be noted that the % improvement in R_C for hole conduction post-CE is significantly larger in Cr-based devices (R_C = 100 Ω-μm) when compared with Ni-based S/D contact devices (R_C = 10 kΩ-μm). Similarly, R_C for electron conduction post-CE reduced significantly in Ni-based devices

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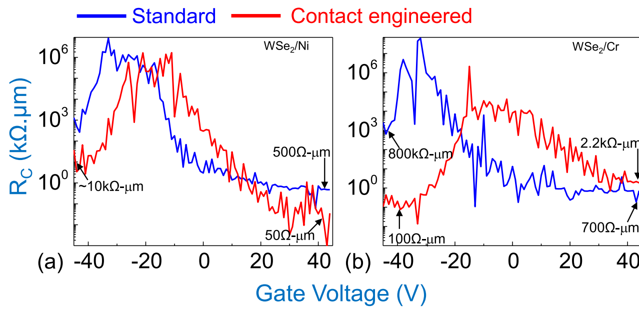

Fig. 7. Contact resistance (R_C) extracted using the Y-function method [16] for standard and contact-engineered WSe_2 FETs with (a) Ni and (b) Cr S/D contacts. Here, $V_{DS} = 4$ V.

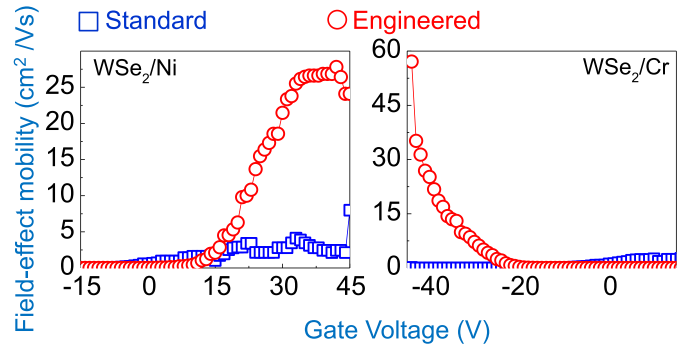

Fig. 9. Field-effect mobility extracted as a function of gate voltage.

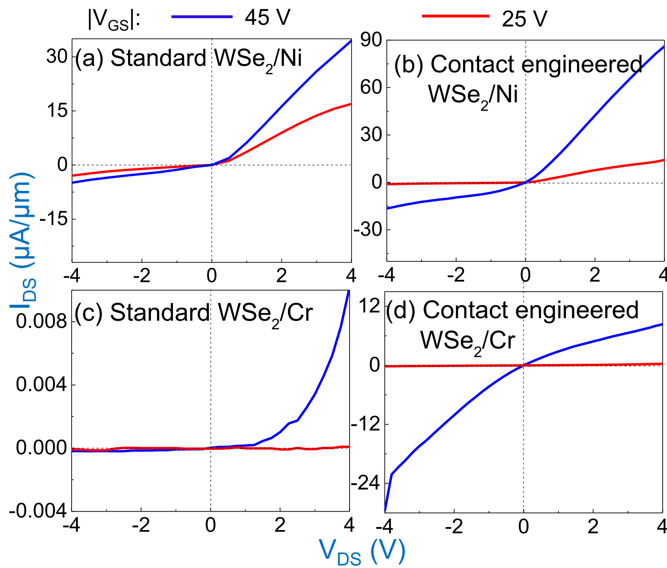

Fig. 8. Output characteristics of WSe_2 FETs before and after H_2S-assisted CE in the low-drain voltage regime with (a) and (b) Ni and (c) and (d) Cr S/D contact. Here, channel length (L_{CH}) is 1 μm and gate oxide thickness (T_{ox}) is 90 nm. Positive gate voltage was chosen for WSe_2/Ni (nMOS) devices, whereas negative gate voltage was chosen for WSe_2/Cr (pMOS) devices while measuring the output characteristics.

(R_C = 50 Ω-μm), which apparently increased, post-CE, in case of Cr-based S/D contact devices (R_C = 10 KΩ-μm). This is counter-intuitive as Ni being a high-work function metal should facilitate higher hole conduction (or reduced R_C for hole transport) and suppressed electron conduction (or increased R_C for electron transport) when compared with Cr-based devices, which is a low-work function metal. Cr being a low-work function metal should have facilitated enhanced electron conduction and suppressed hole conduction. It is worth highlighting that these contradictions are not related to unexpected trends related to other parameters affecting carrier transport. For instance, we noticed that the channel mobility ($\mu_{eff} = (L \cdot t_{ox} \cdot g_m/\epsilon_{ox} \cdot W \cdot V_{DS})$ and its improvement follow the same trends as we have seen for the channel current, as shown in Fig. 9. It is found that contact-engineered Ni-contacted WSe_2 FETs exhibit higher electron mobility than the standard FETs, whereas Cr-contacted WSe_2 FETs exhibit significantly higher hole mobility after CE. These contradictions from the standard theory of metal–semiconductor interface make the situation intriguing, which suggests an atomistic treatment to the problem, to develop and reveal the underlying fundamental mechanism.

IV. Unique Interface Chemistry and Its Impact on Device Behavior

To address this, density functional theory (DFT)-based band structure and DOS calculations were performed for the following four topologies (see Fig. 10) while having interface with Cr or Ni: 1) pristine WSe_2 (T1); 2) with Se vacancy (T2); 3) with S over Se vacancy (T3); and 4) with S at the interstitial site over pristine WSe_2 surface (T4). T1 is the ideal or defect-free contact topology, whereas T2 depicts the case when the TMD surface is not completely defect free due to the finite density of chalcogen vacancies. In practice, for contacts without treatment, T1 and T2 will coexist. T3 and T4 are the possibilities post-S treatment, which is due to the introduction of S in T2 and T1, respectively. In engineered contacts, T3 and T4 can coexist. In addition, metal-TMD bond length in each case was extracted using ATK-based simulations. In case of Cr contact, the bond length was found to increase (from 1.67 to 2.16 Å) with S treatment. The same was found to reduce with S treatment in case of Ni contact (from 1.07 to 0.96 Å). In general, Ni contacts were found to have a smaller bond length when compared with Cr contacts. This depicts higher orbital interaction in case of Ni contact when compared with Cr contact.

As shown in Figs. 11 and 12, atomic interaction between Se vacancy, S at the interstitial site, and metal atoms resulted in metal-induced gap states (MIGSs) that lie between conduction band edge (CBM) and VBM. The energy distribution and density of these states are a strong function of topology and metal contact, which governs the n-/p-type/ambipolar behavior observed in different contact configurations. For instance, in case of contact with Cr, while the MIGS lies at a unique energy level in all cases, the trap state becomes donor type when Se vacancy was introduced (T2). The same, earlier (T1), was at the midgap level. Introduction of donor state enabled S/D Fermi-level movement close to CBM, which increases thermionic electron current contribution and results in an observable electron conduction in WSe_2 FET without S treatment. On the other hand, when the S treatment was introduced, MIGS moved to midgap level when introduced

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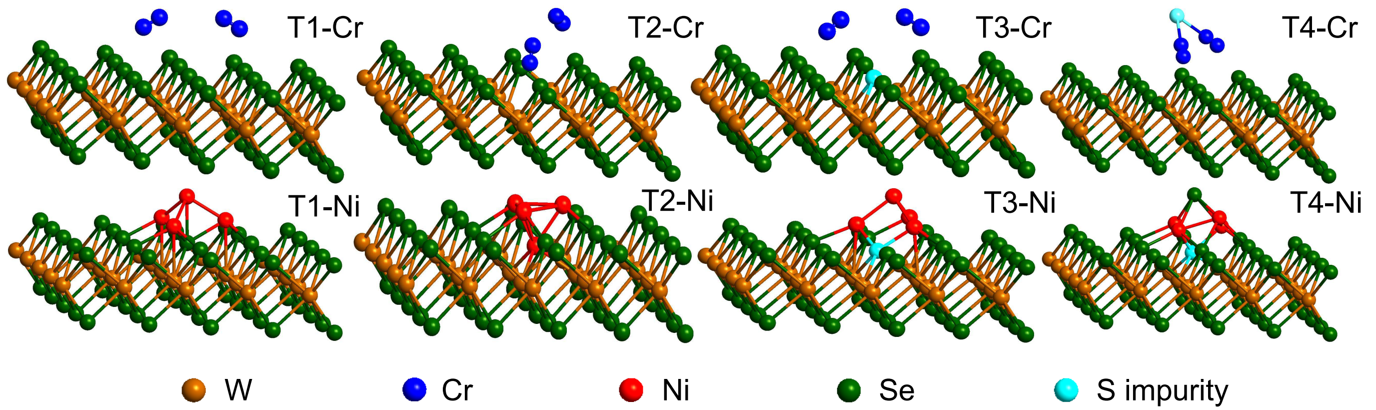

Fig. 10. Various interface topologies optimized using ATK for bandstructure and DOS calculation.

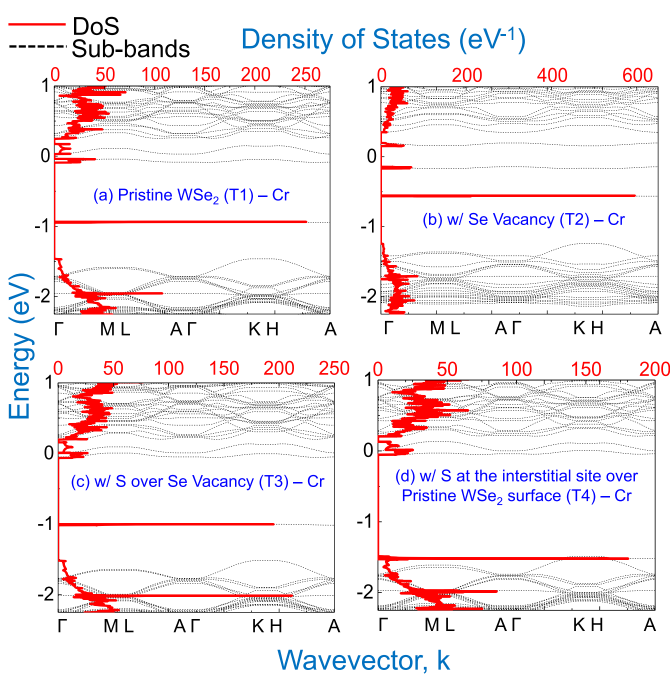

Fig. 11. Change in band structure (black dashed line) and DOS (red solid line) of WSe_2 crystal in contact with Cr compared for the following topologies. (a) pristine WSe_2 (T1). (b) With Se vacancy (T2). (c) With S over Se vacancy (T3). (d) With S at the interstitial site over pristine WSe_2 surface (T4).

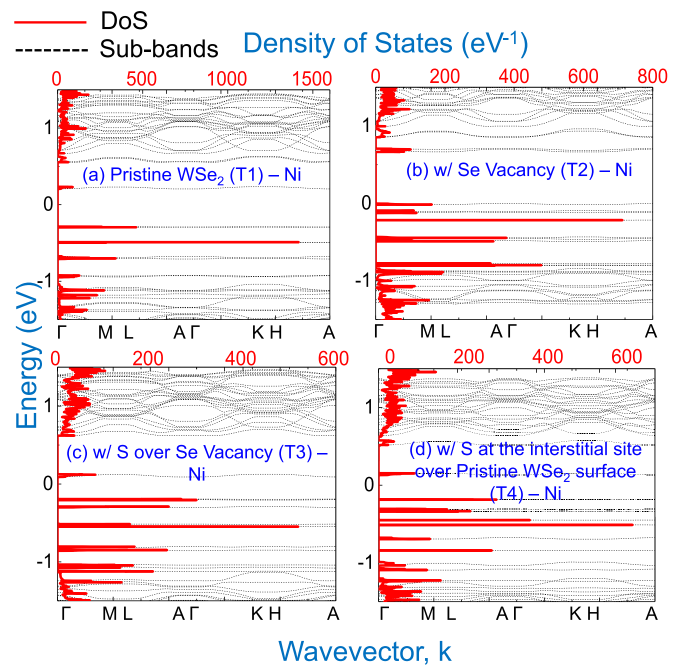

Fig. 12. Change in band structure (black dashed line) and DOS (red solid line) of WSe_2 crystal in contact with Ni compared for the following topologies. (a) Pristine WSe_2 (T1). (b) With Se vacancy (T2). (c) With S over Se vacancy (T3). (d) With S at the interstitial site over pristine WSe_2 surface (T4).

S atom-passivated Se vacancy (T3). The same resulted in degeneracy with VBM when S atom moved to the interstitial site (T4). Due to the defect state's degeneracy at VBM, the S/D Fermi level aligns with VBM, which significantly increases the thermionic hole current component and increases overall hole conduction in WSe_2 FET with S treatment and Cr contacts. Moreover, due to the S/D Fermi level aligns with VBM, thermionic injection of electron suffers, whereas attributed to increased bond length, which increases the tunnel barrier width, tunnel current component degrades significantly. As a result, collectively, electron current mitigates by an observable factor in case of WSe_2 FET with S treatment and Cr contacts.

In case of contact with Ni, MIGSs were found to be distributed across the bandgap between CBM and VBM. In case of T2 and T4, MIGSs near CBM support electron conduction. Moreover, the bond length was found to be smaller in Ni contact due to the stronger orbital interaction, when compared to Cr contact, which in conjunction with MIGS close to CBM dominate the electron conduction. With S treatment of WSe_2–Ni interface (T4), the bond length was found to be further reduced due to the increased orbital interaction, which increases the tunnel and thermionic injection of electrons and leads to a significant increase in electron conduction in WSe_2 FET with S treatment and Ni contacts. Besides, a marginal improvement in hole current was seen in WSe_2 FET with S treatment for Ni contacts, which can be explained by the MIGS shift toward VBM and reduced bond length in case of T4. The improvement was, however, insignificant due to a rather marginal shift of MIGS, which does not allow thermionic hole conduction component to increase significantly. Moreover, due

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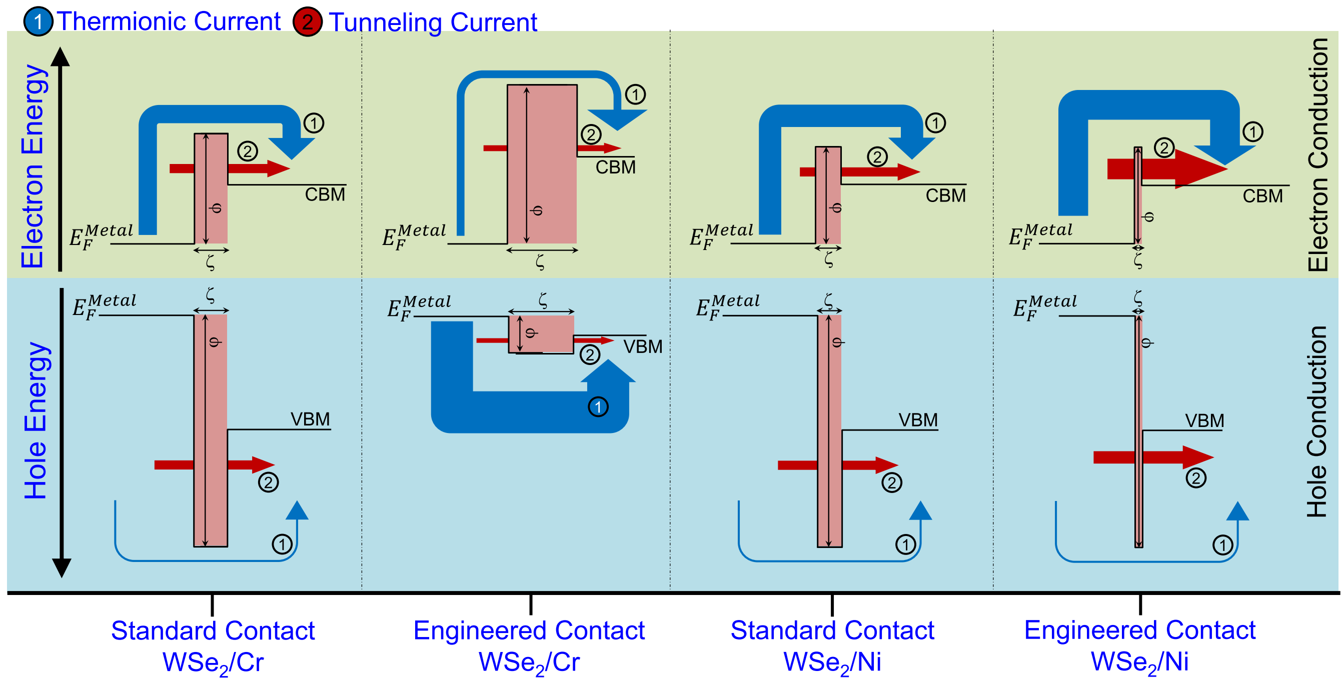

Fig. 13. Effect of metal and contact treatment on: 1) Schottky barrier height (ϕ) due to the relative position of Fermi level in reference to CBM/VBM and its impact on electron's/hole's thermionic injection over the Schottky barrier; 2) tunnel barrier width (ζ) due to the change in bond length, which affects the tunnel current components; and 3) resulting change in thermionic as well as tunneling current components while accounting for ϕ and ζ.

to the higher tunneling mass of hole, tunneling current component too does not increase in proportion to electron tunneling as explained earlier.

V. Conclusion

To summarize and compare, Fig. 13 shows the impact of metal and contact treatment on: 1) barrier height (ϕ) due to the relative position of Fermi level in reference to CBM/VBM, which explains for electron's/hole's thermionic injection over the Schottky barrier; 2) tunnel barrier width (ζ) due to the change in bond length, which defines the tunnel current components; and 3) resulting change in thermionic as well as tunneling current components while accounting for ϕ and ζ. Such fundamental insights, coherent with experimental results, about the impact of the type of defect and metal species on WSe_2–metal interface led to a controlled realization of n- and p-type FETs, thereby establishing another gateway for the development of complementary logic-based circuits on WSe_2.

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