Distinct Failure Modes of AlGaN/GaN HEMTs Under ESD Conditions

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***Abstract*— This article reports the distinct failure mechanisms and insights on device degradation of AlGaN/GaN high electron mobility transistors (HEMTs) under electrostatic discharge (ESD) stress conditions. The role of device surface, MESA isolation, and gate Schottky junction in defining the degradation type is discovered. Premature breakdown at the MESA Schottky junction and dislocation induced failure in the active region and their consequences on ESD robustness are reported. Physical mechanisms responsible for snapback instability in transmission line pulsing (TLP) characteristics are discussed. Change in device failure from soft to hard with pulsewidth is revealed. Finally, the role of contact resistivity, surface diffusion, and channel electric field and its fringing effect at contacts are analyzed in context to ESD failure of AlGaN/GaN HEMTs. Various stages of device degradation during TLP stress are captured on-the-fly using high-resolution (HR) optical microscopy and high-speed Si charge-coupled device (CCD) detector. Postdevice failure, damaged regions are analyzed using transmission electron microscopy and scanning electron microscopy together with *in situ* energy-dispersive X-ray spectroscopy to probe details of failure mechanisms involved. Finally, based on the learning from this article, design guidelines for an ESD robust HEMT are proposed.**

***Index Terms*— AlGaN/GaN high electron mobility transistor (HEMT), electrostatic discharge (ESD) failure modes, reliability, snapback instability.**

I. Introduction

GALLIUM nitride (GaN) has emerged as a promising semiconductor material for high-power applications due to its wide bandgap characteristics. AlGaN/GaN-based high electron mobility transistor (HEMT) promises higher efficiency over a wider temperature range for smaller footprint than Si devices. However, several reliability issues still limit its performance especially under high-voltage and high-current conditions, such as electrostatic discharge (ESD), which are common in automotive and power conversion environments. This article aims to gain insight into the physical mechanisms responsible for failure of GaN HEMT under ESD conditions. A good physical understanding of failure mechanisms is important in the development of rugged device technology. As material structure and device performance are intimately related, failure analysis (FA) of damaged regions in device can reveal vital details about the underlying degradation mechanism. Earlier works present on ESD reliability of AlGaN/GaN HEMT, attributes device failure to mechanisms, such as hotspot [1], filament formation [2]–[4], gate–source diode breakdown [3], gate–drain burnout [5], poor MESA definition [6], increased MESA leakage [7], high contact resistivity [7], and formation of crack in the channel region [8]. From the limited works presented to date, which mostly borrowed failure models from earlier works on AlGaAs/GaAs systems [9], [10], device design guidelines for robust HEMTs cannot be derived. Besides, due to various unique factors involved, which defines the ESD reliability of GaN HEMTs, it is nontrivial to determine exact individual role of various design and technology parameters. Therefore, it is critical to separate their distinct contributions for in-depth understanding of ESD failure in AlGaN/GaN HEMT [11]. To address this gap, our recent work [12] used special HEMT test structures covering unique design and process combinations to study ESD behavior and investigated evolution of ESD robustness with different design parameters. However, a detailed discussion on ESD failure physics and role of different technology parameters in determining the HEMT failure mode was missing.

This article investigates the ESD failure physics using special HEMT test structures while studying the transmission line pulsing (TLP) characteristics and FA of AlGaN/GaN HEMT test structures. This article is structured as follows. The device structure and experimental setup are described in Section II. Different failure modes captured by on-the-fly optical microscopy, scanning electron microscopy (SEM), and transmission electron microscopy (TEM) micrograph of damaged regions in devices failed under different ESD conditions are presented and discussed in Sections III–V. Snapback instability and its root cause are discussed in Section VI. Device design guidelines, derived from physical insights developed, have been presented in Section VII. Finally, Section VIII summarizes the key findings from this article.

II. Device Structure, ESD Characterization, and Degradation Monitoring

The AlGaN/GaN HEMT stack is grown on Si(111) with a linearly graded AlGaN transition region (250-nm

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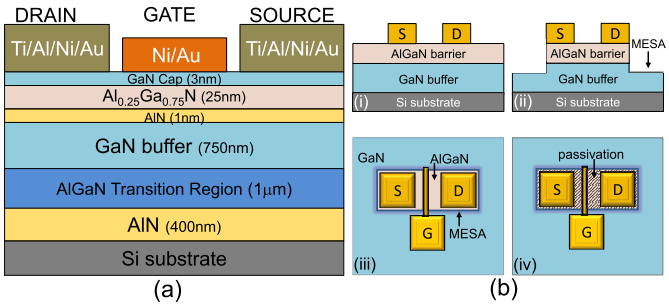

Fig. 1. (a) Schematic of layer stack used in AlGaN/GaN HEMT. Ti-/Al-/Ni-/Au-based source/drain ohmic contact and Ni-/Au-based Schottky gate are used. (b) Schematic cross section of (i) nonisolated structure without gate and (ii) MESA isolated structure without gate. Top view schematic of (iii) isolated structure with gate and (iv) isolated structure with surface passivation used in this article.

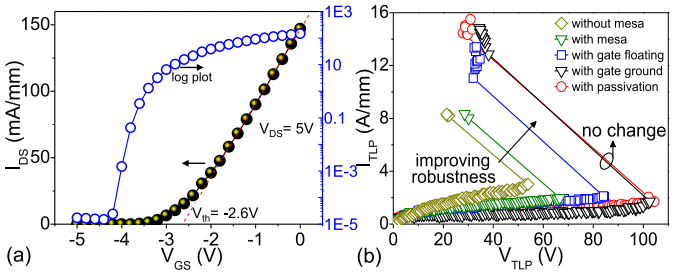

Fig. 2. (a) DC I_{DS}–V_{GS} characteristic of the AlGaN/GaN HEMT under study. (b) TLP characteristics of the different test structures of AlGaN/GaN HEMT obtained under 100-ns TLP stress at drain. Source is grounded in each case.

$Al_{0.75}Ga_{0.25}N$/ 250-nm $Al_{0.5}Ga_{0.5}N$/ 500-nm $Al_{0.25}Ga_{0.75}N$) and 750-nm-thick GaN buffer, as shown in Fig. 1(a). The 100-μm wide HEMT structures are realized on the epitaxial stack in following configurations: 1) with and without MESA isolation; 2) with and without gate; and 3) with and without surface passivation, as shown in Fig. 1(b).

A TLP tester is used to generate ESD pulses of different pulsewidths (PWs) with a fixed rise time (1 ns). Device voltage and current waveforms are recorded and averaged in 60%–90% pulse window to obtain a TLP characteristic. Linear drain-to-source current (I_{dc}) is spot measured under dc, at 50 mV V_{DS}, to monitor degradation after each TLP pulse. Here, low drain bias is used to minimize degradation during spot measurement. On-the-fly optical imaging is done to capture evolution of device failure using a high-resolution (HR) microscope with 1000× magnification and integrated Si charge-coupled device (CCD) camera that can capture up to 100 frames in between two pulses. First, AlGaN/GaN HEMT was dc characterized, and the transfer characteristic as obtained is shown in Fig. 2(a). Test devices of various source-to-drain spacing (L_{SD}) are ESD stressed at the drain, with source grounded. After the test, damaged regions of failed devices are studied using TEM and SEM together with *in situ* energy-dispersive X-ray spectroscopy (EDX) to analyze the signatures of degradation mechanism(s) involved.

Test structures fabricated exclusively with and without MESA isolation, with and without the gate, and with and without surface passivation are stressed at different TLP PW for a systematic step-by-step study of ESD failure in

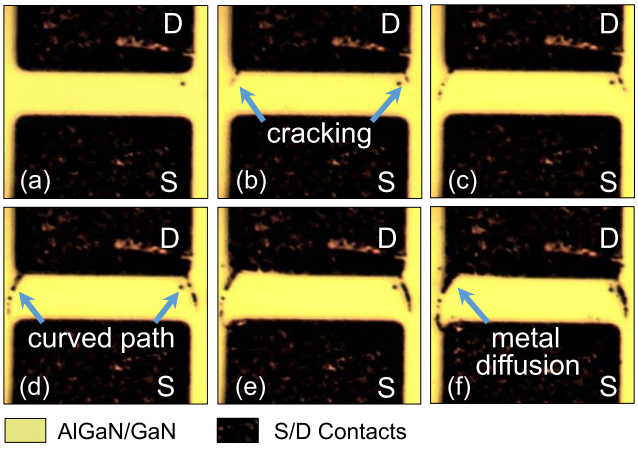

Fig. 3. Sequence of events captured while stressing a test structure without gate and MESA isolation using a 50-ns TLP pulse. (a) Device before stress. During stress: (b)–(d) contact metal(s) melt and diffuse from drain to source (e) following curved path and (f) ultimately lead to a source–drain short and permanent failure. The CCD detector settings are adjusted to high contrast for improved visibility.

AlGaN/GaN HEMT. Three devices are tested in each case to confirm the repeatability of results. Fig. 2(b) summarizes the TLP characteristics recorded at 100-ns PW for all the device variations studied in this article, and the results are consistent in each case. A summary of the key observations from these TLP stress measurements is as follows.

1) All devices show linear TLP characteristics and mostly fail in the snapback region itself.
2) Devices are found more susceptible to ESD failure in absence of device isolation, such as MESA.
3) Gated device exhibits improved ESD robustness than nongated structure.
4) Spot measured linear drain current (I_{dc}) effectively captures degradation in AlGaN/GaN HEMT exhibiting a unique degradation trend in each case.

In all the cases, the lowering of trigger voltage (V_{TRIG}) and failure current (I_{t2}) increased R_{ON} at higher PW, and the increase in V_{TRIG} and I_{t2} with increasing source-to-drain spacing (L_{SD}) is observed. The power required to trigger snapback (P_{Trig}) follows a power-law-like characteristic with PW. I_{t2} scales linearly with source-to-drain spacing. A correlation between % device degradation and snapback depth is established. Trap-induced cumulative degradation and snapback instability are observed in device. The device faces soft failure at low PW and hard failure at high PW. A detailed discussion on the above-mentioned electrical (TLP) findings can be found in our other recent work [12].

III. Failure in Nonisolated Structure Without Gate

A. Defect Assisted Contact Diffusion

The test structure having only source/drain ohmic contacts (see Fig. 1(b)-i) when stressed at drain undergoes a sequence of events as recorded on-the-fly by HR optical microscope is shown in Fig. 3. It reveals the following: 1) drain contact metal migrates/diffuses toward source pad and 2) failure occurs at

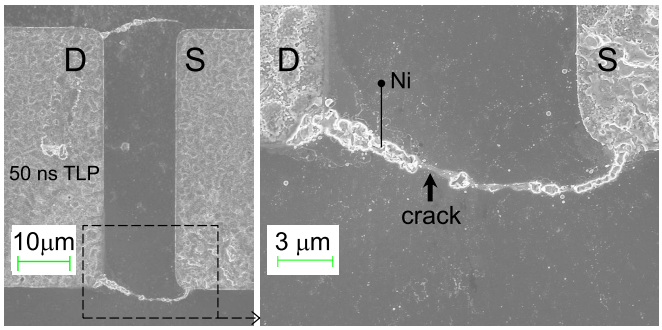

Fig. 4. Postfailure SEM images depicting failure in structure without gate and MESA isolation after 50-ns TLP stress. Damaged corners with curved short paths between the S/D contacts are visible.

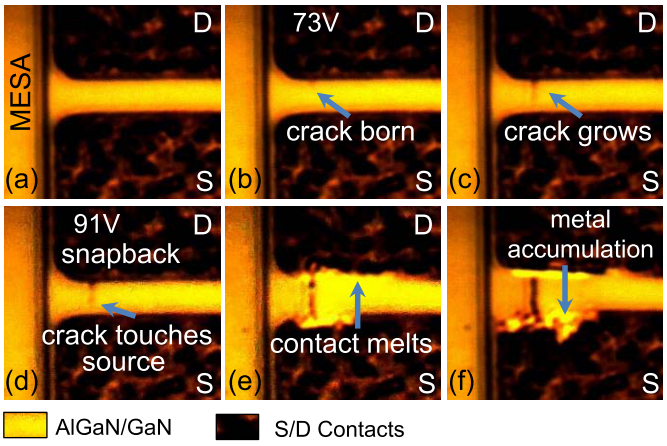

Fig. 5. Sequence of events captured across (a) structure ($L_{SD} = 7\ \mu m$) without gate and with MESA isolation during 50-ns TLP stress. (b) Mechanical crack originates from drain which (c) propagates and (d) touches the source. (e) Contact metals melt from drain edge due to high-current density and (f) diffuse to source via the crack and accumulates on source pad.

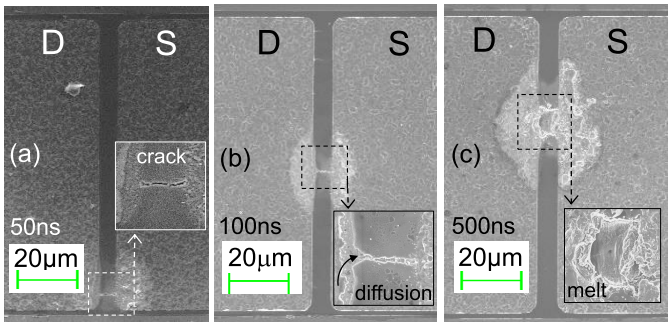

Fig. 6. Postfailure SEM images of structures with MESA isolation, which failed at (a) 50-ns, (b) 100-ns, and (c) 500-ns TLP stresses at drain. It shows (i) failure occurs within channel region and not at contact corners. (ii) Metal diffusion and migration become more aggressive with PW increment.

contact corners. Postfailure SEM imaging in Fig. 4 shows the presence of shallow cracks in top AlGaN-GaN layers, and the EDX analysis confirms the presence of Ni (7.27%) traces in the cracked region. These details point toward a failure mechanism that involves a complex interplay of mechanical stress and material diffusion and can be explained as follows. The normal component of field (E_Z) induces mechanical strain via inverse piezoelectric effect [13] at high ESD voltage, and the lateral component generates thermal stress [14] at high ESD current levels. In the absence of the gate, the electric field peaks at the drain, which further gets enhanced at contact corners due to field crowding. The accumulated stress at corners releases via crack/defect nucleation at drain, which further propagates to source following fringe field lines, as shown in Fig. 3(c)–(f). Over time, high power density (J.E) at contact corners causes localized heating and melt drain contact. Ti/Al/Ni/Au alloy used at drain–source is reported to suffer poor thermal stability and lateral diffusion [15]. Cracks/defects provide low-energy path for material diffusion [16], and Ni has high tendency to diffuse in GaN [17]. Thus, molten Ni diffuses along the crack as confirmed by the EDX analysis and creates a drain–source short, and the device sees permanent failure. It is worth mentioning that crack propagation and material diffusion possibly occur simultaneously as inferred from Fig. 3(c)–(f). Therefore, the test structure without MESA isolation exhibits lowest ESD robustness among all four device variants, under study, as shown in Fig. 2.

IV. Failure in Isolated Structure Without Gate

A. Influence of MESA Isolation

A comparison of the TLP characteristics of the device with and without MESA isolation in Fig. 2 reveals that device with MESA isolation exhibits higher trigger voltage (V_{Trig}) and failure current (I_{t2}) than without MESA isolation. To understand the reason for improved ESD robustness with MESA isolation, a test structure with MESA isolation (see Fig. 1(b)-ii) is stressed. Different stages of its degradation are recorded during the test as presented in Fig. 5(a)–(f). No physical change is visible until a crack originates from drain edge at 73-V stress. With increase in TLP voltage, crack propagates and reaches source at 91 V, and the device's TLP characteristic instantly switches from saturation to snapback region. The abrupt increase in TLP current in the snapback region causes local contact melting and contact shorting, leading to permanent failure. As a result, devices with MESA isolation fail in snapback region itself and exhibit no-holding state akin to device without MESA isolation, as shown in Fig. 2. Failure in device with MESA follows a mechanism similar to that in device without MESA. That is, initially, a crack develops, and then, the contact metal diffuses via crack, which eventually leads to source/drain shorting. However, there is a major difference in the way migration occurs. As noted in Fig. 6, in device with MESA isolation, failure occurs within channel region, whereas in device without MESA isolation, failure occurs at drain corners, as shown in Fig. 4. This behavior is consistent across all PWs and L_{SD} values. The difference can be explained as follows: in structure with MESA isolation, the discontinuity in AlGaN layer at MESA isolation edge locally relaxes tensile strain in AlGaN near drain corners and avoids early cracking at contact corners. However, the AlGaN layer in channel region is always under high tensile strain, which further builds up with increasing channel field due to inverse piezoelectric effect. Thus, the failure occurs in channel.

B. Influence of Self-Heating

A reduction in ESD robusteness is observed with an increase in PW, as shown in Fig. 7(a). To understand this dependence, failure analysis is done for devices that failed at different PWs. It exhibits a complex interplay of mechanical stress (which develops cracks) and diffusion (which causes short). Fig. 6 compares SEM micrograph of similar test structures with MESA isolation that failed at ESD stress of different PWs. Failure at low PW (50 ns) exhibits only crack between the source and the drain with no visible traces of metal migration, but contact edges are seen eroded, as shown in the inset of Fig. 6(a). At higher PW, as the device gets stressed for longer duration, stress accumulation and defect generation are more severe. Furthermore, at high ESD current, localized heating at drain melts contact metal(s) that diffuses through crack, as shown in the inset of Fig. 6(b), and creates electrical short. Moreover, surface diffusion rate also increases at high temperature according to the following equation [18]:

$$h \propto e^{-E_a/k_bT} \tag{1}$$

where h is the hopping rate, E_a is the energy barrier to diffusion, and T is the surface temperature.

Aggressive melting and diffusion at high PW make failure more thermal in nature, as shown in Fig. 6(c). The EDX analysis of short portions confirms the presence of Al, which is melted from the Ti/Al/Ni/Au contact stack. Also, Al content increased from 8% at 100 ns to 12% at 500 ns in shorts.

C. Influence of Electric Field

Devices with larger source–drain spacing (L_{SD}) exhibit higher V_{Trig} and I_{t2}, as shown in Fig. 7(b). Robustness scaling with L_{SD} can be explained as follows: field strength in channel changes with L_{SD} for a given stress voltage. Therefore, L_{SD} influences the field-driven reliability phenomena, such as hot carrier degradation and trapping. FA of the test structures of different L_{SD} that failed at same PW are done. Drain contact melting and metal diffusion occur to a different extent in devices with a different value of L_{SD}, as shown in Fig. 8. It reveals stronger diffusion/migration in smaller L_{SD} (7 μm) device. This is because, as the electric field assists in material diffusion along the surface, the effective activation energy (E_a) for the material diffusion gets lowered in the presence of high field intensity in smaller L_{SD} devices. This observation also explains scaling in ESD robustness with L_{SD}, as shown in Fig. 7(b).

To summarize the learning so far, post-FA is done for test structures without MESA and with MESA isolations that were ESD tested at different PW and L_{SD}. In both cases, failure occurred with cracking in top AlGaN layer and diffusion of drain contact via cracks. Structure without MESA isolation failed at contact corners, while in structures with MESA isolation, failure is confined to the channel region. The higher diffusion rate is observed at larger PW as confirmed by increased metal content in the shorted regions. Failure gets delayed at larger L_{SD}.

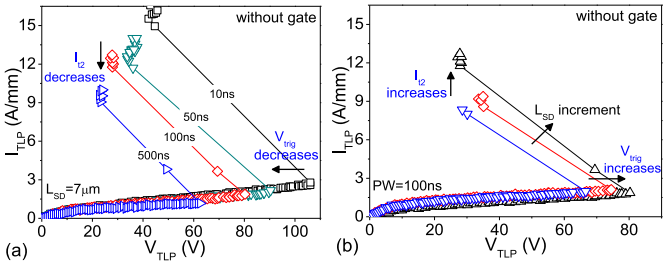

Fig. 7. TLP characteristics of structure without gate and with MESA isolation (a) under TLP stress of different PWs and (b) for a different value of L_{SD}.

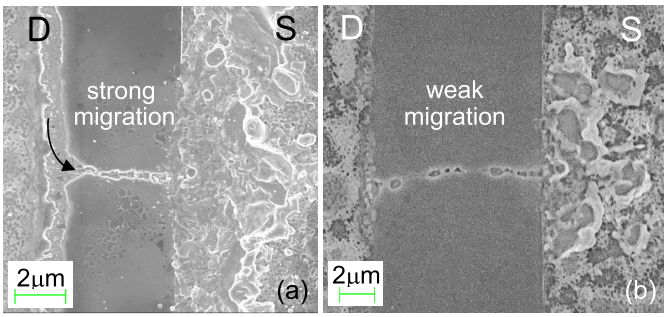

Fig. 8. Comparison of postfailure SEM micrograph of structure without gate and with MESA isolation with (a) L_{SD} 7 μm and (b) L_{SD} 11 μm that failed at 100-ns PW, exhibiting the source/drain short. The device with larger L_{SD} (11 μm) shows suppressed migration.

V. Failure in Isolated Structure With Gate

In the discussion so far, we learned about the effect of MESA isolation and contact diffusion on HEMTs' ESD reliability. Now, to understand the effect of gate, test structures with the Schottky gate (see Fig. 1(b)-iii) are stressed under similar conditions. Physical analysis of failed structures is done to understand the associated failure physics.

A. Influence of Gate

A comparison of TLP characteristics of gated and nongated structures is shown in Fig. 9(a). It reveals higher V_{Trig} and I_{t2} in structure with gate. The improved ESD reliability in the gated structure can be explained as follows: in gated structure, when the drain is stressed, the gate-to-drain Schottky diode gets reverse biased and depletes the 2-dimensional electron gas (2DEG) in gate–drain region. An increase in drain stress extends the depletion region toward drain [19], which spreads field lines in channel and relaxes electric field (E) in gate vicinity. Moreover, depletion of 2DEG increases device's R_{ON} and limits the current density (J). As a result, the power density ($J.E$) in channel gets lowered. A decrease in power density means less self-heating and reduced channel temperature, which suppresses the temperature-dependent scattering and mobility degradation [20]. As a result, device sustains higher ESD stress and exhibits higher V_{Trig} before failure. To validate the hypothesis, a test structure with partially gated channel region is fabricated and tested with a 100-ns pulse at drain. SEM micrograph of the failed structure shown in Fig. 9(b) illustrates that failure preferably occurs in the

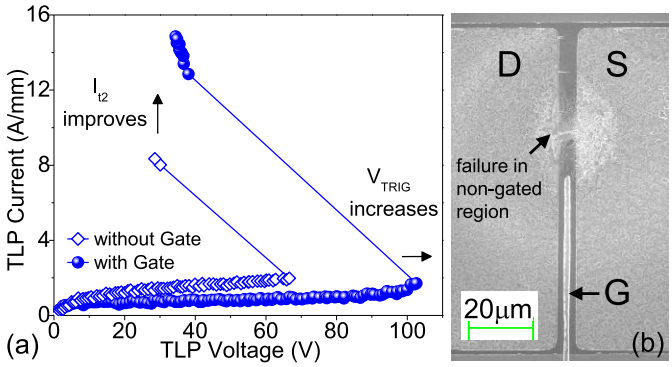

Fig. 9. (a) Comparison of TLP characteristics of a structure with gate (grounded) and without the gate. Figure highlights higher failure current (I_{t2}) and trigger voltage (V_{TRIG}) in the gated structure. (b) Postfailure SEM micrograph of partially gated structure.

nongated region and no physical damage is seen in the gate-controlled region. This observation corroborates well with the hypothesis and that the presence of gate improves the ESD reliability of HEMT.

B. Failure Under Gate Floating

Now, it is clear that the presence of the gate further improves the ESD robustness of the test structure. Next, the device is stressed at drain under two stress conditions, namely, with gate floating and with gate grounded. Fig. 10(a) shows a comparison of the TLP characteristics obtained in the two conditions. It shows that the device when stressed under floating gate sees early failure. The parasitic capacitive coupling between the gate and drain turns on the gate-to-source Schottky diode [3]. The gate-to-source Schottky diode begins to degrade much below the snapback point (V_{Trig}) as evident from its increased reverse and forward current, measured at different stress levels, as shown in Fig. 10(b). Moreover, the device shows a negative shift in threshold voltage, an increase in drain-to-source leakage, and ON-resistance, unlike reported in previous literature [3]. SEM image of the failed device reveals damage at the MESA edge toward the gate pad and points to an interesting failure mechanism, as in the following.

1) Failure of MESA Schottky Diode: A parasitic Schottky diode exists at MESA edge where 2DEG gets exposed to the gate finger running over side wall. It can have a detrimental effect on device reliability as illustrated in the SEM image of one of the failed structures in Fig. 11. It depicts that the damage occurs at the MESA edge that points to premature breakdown of the MESA Schottky diode. The gate-to-source diode turn-on increases gate leakage. High leakage through the weak MESA Schottky diode causes gate metal melting/peel-off, followed by gate-to-drain–source shorts. The EDX analysis of the shorted region confirmed the presence of 15.7% Au, which possibly migrated from Ni/Au gate finger. This finding complements the existing literature [3], where gate-to-source diode turn-on is reported to follow by filamentation in the gate–drain region and eventually permanent failure in device.

C. Failure Under Gate Grounded

Next, the device is stressed under grounded gate condition. Fig. 12(a) shows the postfailure SEM micrograph of the failed

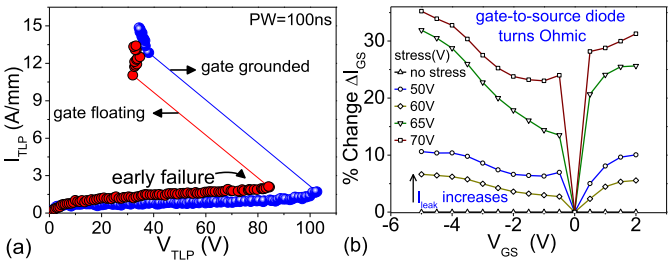

Fig. 10. (a) TLP characteristics of the gated structure under floating gate and grounded gate stress conditions. (b) Percentage increase in the gate-to-source Schottky diode reverse and forward current with stress.

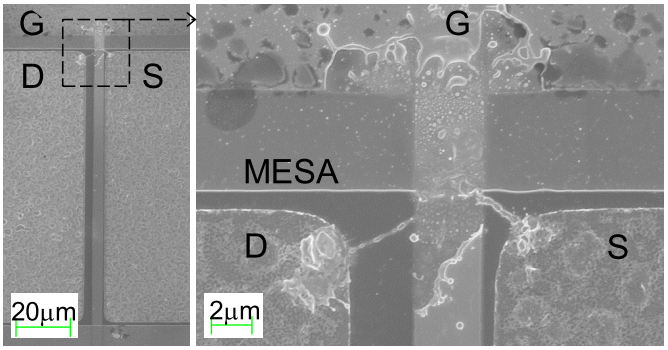

Fig. 11. Postfailure SEM micrograph of structure with MESA isolation and gate, which was stressed at 100-ns TLP stress under floating gate condition. The figure reveals the premature breakdown of gate Schottky diode at MESA edge.

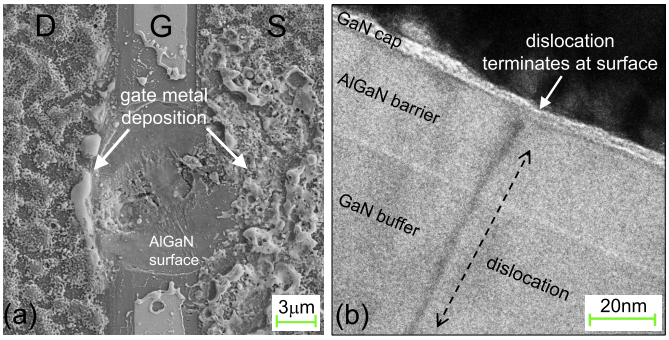

Fig. 12. (a) Postfailure SEM micrograph of a structure with MESA isolation and gate stressed under grounded gate condition using 50-ns TLP pulse. (b) TEM cross section taken at damaged location reveals a dislocation site.

structure. Localized damage in channel region can be seen with gate finger blown-off and aggressive metal peel-off. This happened because in grounded gate condition, the gate-to-drain Schottky diode is reverse biased with the peak field at gate edge toward drain. Under transient stress, such as ESD, the gate edge faces tensile thermoelastic strain [21], which makes gate finger more prone to damage. An increase in TLP stress at drain enhances the peak field intensity and tensile strain at the gate edge. Eventually, the gate finger blows off due to the excessive strain accumulation, as shown in Fig. 12(a).

1) Role of Dislocation in Failure: TEM cross section of the damaged area is done in the gate peel-off region [in Fig. 12(a)]. Interestingly, it reveals the presence of a threaded dislocation also under the gate finger, as shown in Fig. 12(b).

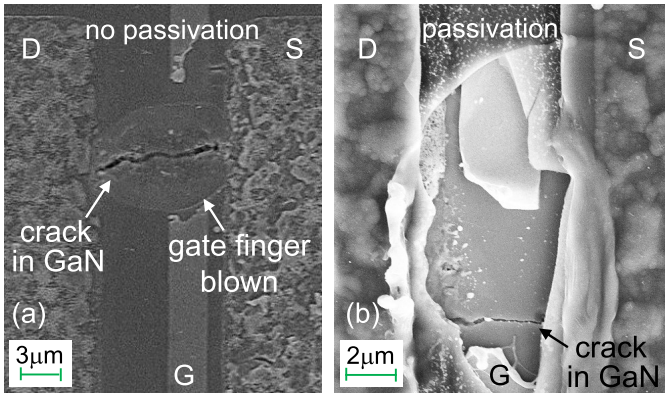

Fig. 13. Postfailure SEM images of HEMT (a) without passivation and (b) with passivation, stressed under similar condition (grounded gate, 100-ns TLP). In both cases, a massive crack is present between the source and the drain with gate finger blown-off.

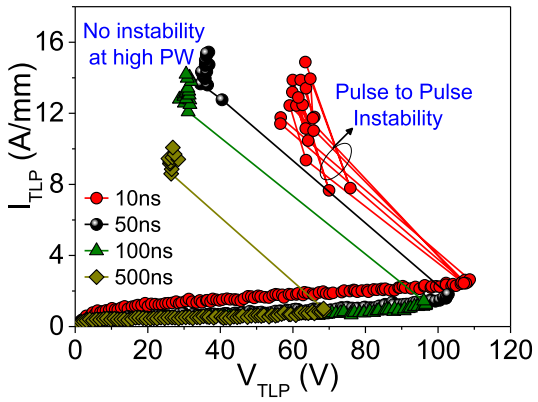

Fig. 14. TLP characteristics of a device stressed under grounded gate condition at different PWs. Instability observed in the snapback region at 10 ns is absent at higher pulse duration.

Since dislocations provide a path for metal diffusion so possibly, the gate metal diffused into dislocation, which locally deteriorated the Schottky junction [22] and enhanced the gate leakage [23]. All these effects locally weakened the gate finger and the finger blows off at the dislocation site with increase in the TLP stress. The gate metal(s) splash with the blow and deposit on the source/drain pads, as evident from Fig. 12(a).

D. Influence of Surface Passivation

HEMT devices, in practice, use surface passivation, such as SiN and SiO_2, to suppresses surface effects that are responsible for current collapse [24] or dynamic R_{ON} [25] in GaN HEMTs. Surface passivation also introduces additional mechanical stress into AlGaN/GaN system [26]. Therefore, it is worth studying the effect of the passivation layer on ESD robustness in AlGaN/GaN HEMTs. To investigate the role of surface passivation on ESD failure, devices without and with SiN passivation [see Fig. 1(b)-iii and iv] are stressed under the same stress conditions. Fig. 2(b) shows the TLP characteristic of the device with and without passivation. V_{Trig} and I_{t2} are the same as in the device without passivation. This observation points that ESD failure physics of GaN HEMT seems independent of the surface condition in present case. In fact, the unchanged V_{Trig} in both the cases hints of a field-driven failure mechanism. Failed devices, in both the cases, showed massive cracking in source–drain region with gate finger blown-off, as shown in Fig. 13. This shows that the inverse piezoelectric effect dominants the failure mechanism and the device's surface conditions are observed to have minimal impact on the ESD robustness of GaN HEMT.

Table I summarizes the impact of different parameters on ESD performance (V_{Trig} and I_{t2}) and the failure mechanisms dominant in different types of ESD test structures used in this article. In all the cases, V_{Trig} and I_{t2} increased with L_{SD} and decreased with increase in ESD PW.

VI. Snapback Instability

AlGaN/GaN HEMT devices, when stressed using a shorter pulse (10 ns), were found to show an unstable TLP characteristic. The device characteristic was seen to oscillate between the blocking and snapback states, as shown in Fig. 14. To depict the pulse-to-pulse instability further, Fig. 15(a) and (b) shows the device voltage and current versus time waveforms, respectively, compared for consequently blocking and snapback states. When the voltage across the device drops, the current through the same increases, which can be seen as the snapback mode. The same, however, recovers back to the blocking state during the next pulse. The postfailure SEM image of the device in Fig. 15(c) shows multiple physical damages along the device width, which depicts localized regions consisting higher carrier/current density or multiple dominating current paths, i.e., current filaments, along the width from source to drain. The nonuniform

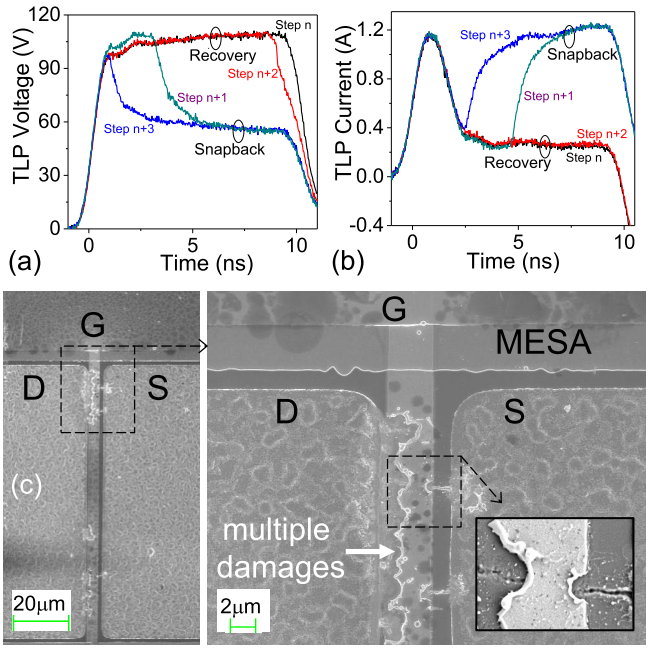

Fig. 15. (a) Voltage and (b) current versus time waveform captured across the device depicting pulse-to-pulse instability. (c) Postfailure SEM picture of device stress using 10-ns TLP under grounded gate condition.

TABLE I
IMPACT OF DIFFERENT DESIGN AND TECHNOLOGY PARAMETERS ON ESD ROBUSTNESS, FAILURE MECHANISM, AND FAILURE LOCATION IN GaN HEMTs

ESD Test Structure	MESA	Gate	V_{Trig}	I_{t2}	Failure Spot	Failure Mechanism
w/o MESA & w/o Gate	No	No	Low	Low	At Source/Drain corners	Crack formation in AlGaN barrier near source/drain contact corners & metal diffusion via cracks
w/ MESA & w/o Gate	Yes	No	Improved	Improved	In channel region	Crack formation in AlGaN barrier & channel and metal diffusion via cracks
w/ MESA & Floating gate	Yes	Floating	Improved	Improved	At MESA edge under the gate	MESA Schottky turn-ON due to C_{gd} coupling
w/ MESA & grounded gate	Yes	Grounded	High	High	At Gate finger	Gate finger blows-off due to mechanical strain near gate edge
w/ MESA & Surface Passivation	Yes	Grounded	High	High	At Gate finger	Gate metal finger blew-off due mechanical strain between gate and drain
p-GaN Cap Gate (commercial) HEMT	NA	Grounded	High	High	In Gate Region	Gate bus bar blew-off due to mechanical strain between drain and gate

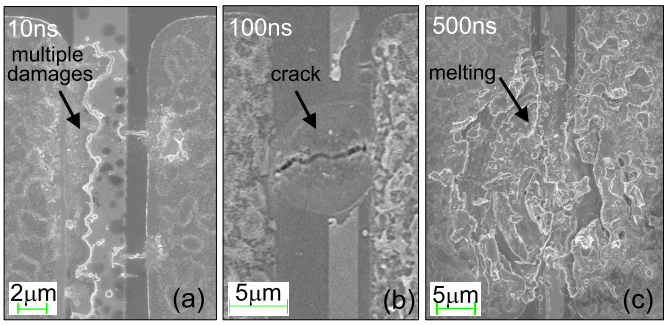

Fig. 16. Postfailure SEM picture of device stress using (a) 10-ns, (b) 100-ns, and (c) 500-ns TLPs.

conduction could be due to nonuniform trap distribution along the width and, hence, nonuniform field distribution. This eventually leads to development of multiple cracks underneath the gate finger at higher stress levels originated along the current paths, as shown in Fig. 15. To confirm this hypothesis, the test was repeated in presence of subbandgap UV ($\lambda = 365$ nm) exposure and higher PWs. No instability in snapback region was found under UV exposure. Moreover, at higher pulse stress durations, the instability vanished, as shown in Fig. 14. This highlights that trapping–detrapping mechanism is responsible for the snapback instability, which vanishes under UV exposure or self-heating conditions (under higher PW stress), which allows uniform field distribution. UV exposure permanently detraps the carrier by photo excitation, whereas the later assists in carrier detrapping by thermal excitation. This can be further confirmed by analyzing failure behavior at higher PWs, as shown in Fig. 16. While short-pulse (10 ns) stress leads to multiple damages along the width, device was found to fail with aggravated crack development between source and drain with gate or drain metal migration when PW was increased to 100–500 ns.

VII. DESIGN GUIDELINES TO IMPROVE ESD ROBUSTNESS

Based on the discussions in the earlier sections, the following device design guidelines can be derived for improved ESD robustness of AlGaN/GaN HEMTs.

1) *S/D Contacts:* S/D metal contacts of individual fingers should have corner rounding at their extreme ends.
2) *Isolation Between Fingers or Set of Fingers:* A trench (or MESA) isolation when used around the active area relaxes the tensile strain in the AlGaN barrier, which suppresses cracking and improves ESD robustness. Power switches typically have 100 s of fingers (active regions) connected in parallel to each other. Here, the device's robustness can be increased by introducing a trench (MESA) isolation between the individual fingers. Besides, the distance between the contact pads and trench (MESA) edge must also be optimized for maximum robustness.
3) *Schottky Contacts in MESA Region:* The Schottky contact of gate metal finger with GaN buffer in the trench (MESA) region must be avoided. This can be achieved by using a trench (MESA) fill by a dielectric.
4) *Gate Finger:* Field plate can be used to reduce mechanical strain in gate vicinity. It suppresses field peak and the associated mechanical strain.

VIII. CONCLUSION

ESD failure physics of AlGaN/GaN HEMT was investigated using specially designed test structures while studying role of different effects step-by-step. Distinct failure modes were observed in each case. In the absence of gate, the field peaked at drain and piezoelectric stress-induced cracking at drain edge under high ESD field. Contact metals like Ni/Au melted from drain, diffused to source along the crack, shorting source drain, which caused permanent device failure. In the absence of MESA isolation, fringing field accelerated crack formation and metal migration led to early failure at corners. ESD robustness scaled with an increase in source-to-drain spacing and a decrease in pulse width due to suppressed surface diffusion at smaller field intensity and lower surface temperature, respectively. Failure in gated structure retarded as Schottky depletion reduced power density in channel. However, parasitics in gate vicinity, such as MESA Schottky diode and threaded dislocations, caused premature breakdown. Thermal instability and nonuniform carrier trapping

along the device width triggered multiple localized current conduction paths, which caused snapback instability at low pulsewidth. Increase in pulsewidth vanished device instability as it aggravated crack development between source and drain, which blew off the gate finger. Based on the above-mentioned learnings, design guidelines for an ESD robust HEMT were proposed.

REFERENCES

[1] J. Kuzmík, D. Pogany, E. Gornik, P. Javorka, and P. Kordoš, "Electrical overstress in AlGaN/GaN HEMTs: Study of degradation processes," *Solid-State Electron.*, vol. 48, no. 2, pp. 271–276, Feb. 2004.

[2] J. Kuzmík, D. Pogány, E. Gornik, P. Javorka, and P. Kordoš, "Electrostatic discharge effects in AlGaN/GaN high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 83, no. 22, pp. 4655–4657, Dec. 2003, doi: 10.1063/1.1633018.

[3] A. Tazzoli, F. Danesin, E. Zanoni, and G. Meneghesso, "ESD robustness of AlGaN/GaN HEMT devices," in *Proc. 29th Electr. Overstress/Electrostatic Discharge Symp. (EOS/ESD)*, Sep. 2007, p. 4A, doi: 10.1109/EOSESD.2007.4401762.

[4] M. Meneghini *et al.*, "Normally-off GaN-HEMTs with p-type gate: Off-state degradation, forward gate stress and ESD failure," *Microelectron. Rel.*, vol. 58, pp. 177–184, Mar. 2016.

[5] V. Vashchenko and A. Shibkov, "Ultra high voltage ESD," in *Proc. Int. Electrostatic Discharge Workshop*, May 2011, pp. 1–13.

[6] M. Meneghini, A. Tazzoli, G. Mura, G. Meneghesso, and E. Zanoni, "A review on the physical mechanisms that limit the reliability of GaN-based LEDs," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 108–118, Jan. 2010, doi: 10.1109/TED.2009.2033649.

[7] S.-C. Lee, J.-C. Her, S.-M. Han, K.-S. Seo, and M.-K. Han, "Electrostatic discharge effects on AlGaN/GaN high electron mobility transistors on sapphire substrates," *Jpn. J. Appl. Phys.*, vol. 43, no. 4B, pp. 1941–1943, Apr. 2004. [Online]. Available: http://stacks.iop.org/1347-4065/43/i=4S/a=1941

[8] I. Rossetto *et al.*, "Demonstration of Field- and power-dependent ESD failure in AlGaN/GaN RF HEMTs," *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2830–2836, Sep. 2015, doi: 10.1109/TED.2015.2463713.

[9] V. A. Vashchenko and V. F. Sinkevitch, "Current instability and burnout of HEMT structures," *Solid-State Electron.*, vol. 39, no. 6, pp. 851–856, Jun. 1996. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110195004041

[10] V. A. Vashchenko, N. A. Kozlov, Y. B. Martynov, V. F. Sinkevitch, and A. S. Tager, "Negative differential conductivity and isothermal drain breakdown of the GaAs MESFET," *IEEE Trans. Electron Devices*, vol. 43, no. 4, pp. 513–518, Apr. 1996.

[11] B. Shankar and M. Shrivastava, "Unique ESD behavior and failure modes of AlGaN/GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2016, pp. EL-7-1–EL-7-5, doi: 10.1109/IRPS.2016.7574608.

[12] B. Shankar, S. Raghavan, and M. Shrivastava, "ESD reliability of AlGaN/GaN HEMT technology," *IEEE Trans. Electron Devices*, vol. 66, no. 9, pp. 3756–3763, Sep. 2019, doi: 10.1109/TED.2019.2926781.

[13] A. Sarua *et al.*, "Piezoelectric strain in AlGaN/GaN heterostructure field-effect transistors under bias," *Appl. Phys. Lett.*, vol. 88, no. 10, Mar. 2006, Art. no. 103502, doi: 10.1063/1.2182011.

[14] A. Sarua, T. Batten, H. Ji, M. J. Uren, T. Martin, and M. Kuball, "ESD issues in compound semiconductor high frequency devices and circuits," in *Proc. CS MANTECH Conf.*, May 2009, pp. 1–12.

[15] H. Morkoç, *Handbook of Nitride Semiconductors and Devices, Electronic and Optical Processes in Nitrides*, vol. 2. Hoboken, NJ, USA: Wiley, Aug. 2009, doi: 10.1002/9783527628414.

[16] M. Kuball, M. Tapajna, R. J. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes," *Microelectron. Rel.*, vol. 51, no. 2, pp. 195–200, Feb. 2011. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271410004786

[17] H.-C. Chiu, C.-W. Lin, C.-K. Lin, H.-L. Kao, and J. S. Fu, "Thermal stability investigations of AlGaN/GaN HEMTs with various high work function gate metal designs," *Microelectron. Rel.*, vol. 51, no. 12, pp. 2163–2167, Dec. 2011. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271411001776

[18] K. Oura, V. Lifshits, A. Saranin, A. Zotov, and M. Katayama, *Surface Science: An Introduction*, 1st ed. Berlin, Germany: Springer-Verlag, May 2003, doi: 10.1007/978-3-662-05179-5.

[19] T. Sugiyama *et al.*, "Evaluation methodology for current collapse phenomenon of GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2018, p. 3B-4.

[20] V. Joshi, A. Soni, S. P. Tiwari, and M. Shrivastava, "A comprehensive computational modeling approach for AlGaN/GaN HEMTs," *IEEE Trans. Nanotechnol.*, vol. 15, no. 6, pp. 947–955, Nov. 2016.

[21] J. P. Jones, E. Heller, D. Dorsey, and S. Graham, "Transient stress characterization of AlGaN/GaN HEMTs due to electrical and thermal effects," *Microelectron. Rel.*, vol. 55, no. 12, pp. 2634–2639, Dec. 2015. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271415301554

[22] R. S. Kajen, L. K. Bera, H. R. Tan, S. B. Dolmanan, Z. W. Cheong, and S. Tripathy, "Formation of Ni diffusion-induced surface traps in GaN/Al_x Ga_{1-x}N/GaN heterostructures on silicon substrate during gate metal deposition," *J. Electron. Mater.*, vol. 45, no. 1, pp. 493–498, Jan. 2016, doi: 10.1007/s11664-015-4135-4.

[23] W. Qian, G. Rohrer, M. Skowronski, K. Doverspike, L. Rowland, and D. Gaskill, "Open-core screw dislocations in GaN epilayers observed by scanning force microscopy and high-resolution transmission electron microscopy," *Appl. Phys. Lett.*, vol. 67, no. 16, pp. 2284–2286, Aug. 1995. [Online]. Available: http://dx.doi.org/10.1063/1.115127

[24] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001, doi: 10.1109/16.906451.

[25] D. Jin and J. A. del Alamo, "Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs," in *Proc. 24th Int. Symp. Power Semicond. Devices ICs*, Jun. 2012, pp. 333–336, doi: 10.1109/ISPSD.2012.6229089.

[26] N. Shigekawa and S. Sugitani, "Numerical analysis of impact of stress in passivation films on electrical properties in AlGaN/GaN heterostructures," *IEICE Electron. Express*, vol. 6, no. 14, pp. 1045–1050, 2009, doi: 10.1587/elex.6.1045.