Physical Insights Into the ESD Behavior of Drain Extended FinFETs (DeFinFETs) and Unique Current Filament Dynamics

B. Sampath Kumar, Milova Paul, Harald Gossner, *Senior Member, IEEE*, and Mayank Shrivastava, *Senior Member, IEEE*

***Abstract*—Single and multi-Fin behavior of drain-extended FinFET (DeFinFET) devices under low and high current injection conditions is studied using detailed 3-D TCAD simulations. For completeness, electrostatic discharge (ESD) behavior of both shallow trench isolation (STI)-type and non-STI-type DeFinFET devices is studied. Under low current injection, junction breakdown, parasitic bipolar turn-on, as well as the onset of space charge modulation and its implications on high current behavior are explored. Under high current injection, the role of space charge modulation in electrothermal instability and filament formation is discussed. Unique filament spreading behavior has been discovered in DeFinFETs. Fin-based construction was found responsible for filament spreading. The interplay among bipolar turn-on, bipolar efficiency, filament density, and nature of filament spreading is explained.**

***Index Terms*—DeMOS, drain-extended FinFET (DeFinFET), electrostatic discharge (ESD), FinFET, laterally double diffused MOS (LDMOS), system on chip (SoC).**

I. Introduction

ADVANCED system-on-chip (SoC) applications require various high-voltage (HV) circuit capabilities, to be integrated over the same chip, such as dc–dc converters, level shifters, and RF power amplifiers [1], [2]. In the planar technology nodes, drain-extended MOS (DeMOS) devices catered to such HV applications. Drain-extended FinFETs (DeFinFETs) are expected to offer HV-handling capability in FinFET nodes for the same applications. Since traditional cascading of low-voltage transistors, to scale up the voltage-handling capability, is limited to <3.3 V in FinFET nodes, DeFinFET becomes a pressing demand [3], [4]. To enable HV devices, such as drain-extended concepts, in ultrascaled nodes, electrostatic discharge (ESD) and hot carrier robustness are the most important qualifiers. Planar DeMOS devices were earlier found to be highly susceptible to ESD events due to early current filament formation and filament-driven failure [5]. This was addressed by delaying the onset of space charge modulation, which was found to cause filament-driven failure [6], [7]. Although several works have reported the ESD failure mechanism of planar DeMOS or laterally double diffused MOS (LDMOS) devices [6]–[10], similar work on DeFinFET is broadly missing except a preliminary work by Sampath Kumar *et al.* [11]. Keeping this gap in mind, this article attempts to extend its predecessor [11] to explore physics of DeFinFET devices under ESD stress conditions. Physical insights into the quasistatic as well as transient operation using 3-D TCAD simulations are developed while highlighting the ESD current dynamics in multi-Fin DeFinFET and shallow trench isolation (STI)-DeFinFET devices, which were missing in the previous work.

This article is arranged as follows. Section II explains the construction and low current operation of various DeFinFETs under study. Section III discusses transmission line pulsing (TLP) characteristics of DeFinFET and STI-DeFinFET extracted using single-Fin and multi-Fin 3-D TCAD simulations. ESD device physics and quasi-static behavior of current filament is presented in Section IV, whereas the dynamics of current filamentation, filament spreading, and failure are explained in Section IV. Filament mechanisms and dynamics discovered in this article are systematically summarized in Section V. Finally, the work is concluded in Section VI.

II. DeFinFETs

Fig. 1 shows the multi-Fin (3-D), single-Fin (3-D), and cross-sectional (2-D) view of DeFinFET and STI-DeFinFET. DeFinFET uses the same Fin for the channel, drift region, and drain contact. Attributed to this construction, the current conduction in DeFinFET is laterally confined, as depicted in Fig. 2(a). STI-DeFinFET, on the other hand, uses two Fins—one for channel as well as drift region and the other Fin (aligned to channel Fin) for the drain contact. Here, the drift region's Fin and drain contact Fin are electrically connected through an N-well while having an STI-based isolation between the two Fins. Attributed to this construction, the current from drain to channel flow via N-well under the STI region, as depicted in Fig. 2(b). Besides, placement of

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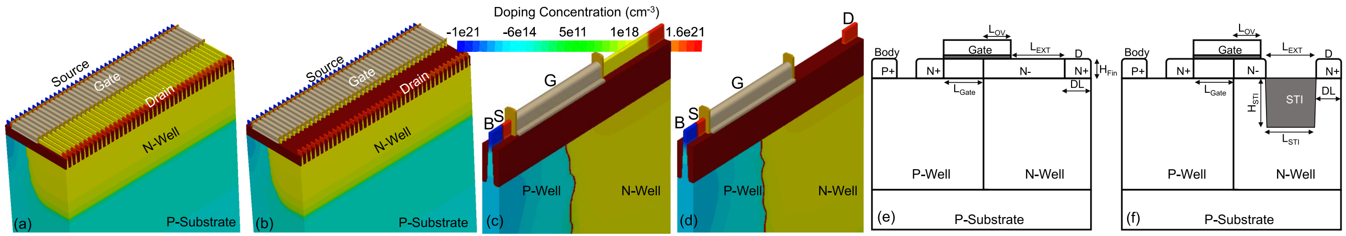

Fig. 1. (a) and (b) 3-D or isometric view, (c) and (d) single-Fin or quasi-3-D, and (e) and (f) cross-sectional view of (a), (c), and (e) DeFinFET and (b), (d), and (f) STI-DeFinFET. Unlike a DeFinFET device, an STI-DeFinFET has an STI isolation in the drift region [2]. Here, a highly doped drain Fin contact is disposed over a moderately doped drain-extended N-well, which enables HV-handling capability. P-type well is implanted deeper into the inactive fin and bulk regions, while keeping the channel region (active Fin) undoped. The gate overlap and Fin region under gate overlap region are extended over the N-well region to reduce the surface field. Drain extension length (DL) (L_{EXT}) and STI length (L_{STI}) for DeFinFET and STI-DeFinFET, respectively, are optimized through a detailed design of experimental simulation to maximize the breakdown voltage-ON-resistance tradeoff [2], [3]. Details of ESD TCAD setup are presented in our earlier works [12]–[14]. For both DeFinFET and STI-DeFinFET $W_{Fin} = 10$ nm, $H_{Fin} = 40$ nm, $L_{Gate} = 320$ nm, $L_{Ov} = 120$ nm, $L_{EXT} = L_{STI} = 200$ nm, peak N-well doping (N_{Doping}) $= 3 \times 10^{17}$ cm^{-3}.

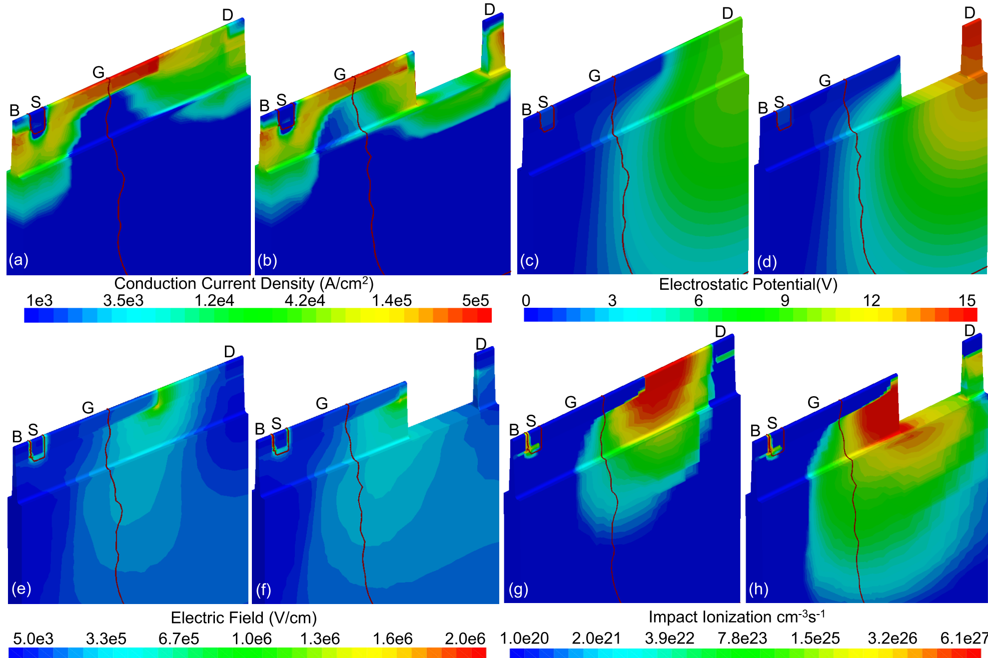

Fig. 2. (a) and (b) Current density, (c) and (d) electrostatic potential, (e) and (f) electric field, and (g) and (h) impact ionization rate across DeFinFET (a), (c), (e), and (g) and STI-DeFinFET (b), (d), (f), and (h) at junction breakdown (at A: $I_{TLP} = 1$ μA/μm): current normalized to device layout width.

STI in the drift region changes the electrostatic potential distribution, which in turn changes the electric field profile and eventually the impact ionization under the high field condition. Fig. 2(c) and (d) shows that STI-DeFinFET can hold higher voltage than the DeFinFET device, for the same lateral dimensions, which is due to STI in the drift region. STI enables higher voltage-handling capability of STI-DeFinFET, before avalanche breakdown takes place. This leads to lower electric field in STI-DeFinFET, for a given drain voltage, when compared to DeFinFET. At avalanche breakdown, both the devices encounter peak electric field at the gate overlap edge. In the case of DeFinFET, as depicted in Fig. 2(e), the peak field can be seen in active drift (Fin) region, which results into peak impact ionization in the active Fin region [Fig. 2(g)]. On the other hand, due to STI in the drift region of STI-DeFinFET, the peak electric field and impact ionization is found to be localized in the inactive Fin region, under the gate overlap [Fig. 2(f) and (h)]. Due to peak avalanche multiplication confined close to the Fin surface, electron and hole pairs generated at the gate edge are effectively collected by drain and substrate contacts. It is worth highlighting that at breakdown, the current through source contact is missing. Majority of the current through the body contact signifies that parasitic bipolar (formed by N-well, P-substrate/p-well, and the N+ source) has not triggered yet.

III. TLP Behavior of DeFinFETs

Fig. 3(a) and (b) shows simulated Fig. 3(a) TLP I–V (I_0 vs. V_{TLP}) and maximum lattice temperature versus pulse current (I_{TLP}) characteristics of DeFinFET and STI-DeFinFET. Both single-Fin and multi-Fin (number of Fins: $N_F = 40$) devices were simulated using 3-D TCAD. A single-Fin, due to its few-nanometer-Fin thickness, emulates 2-D or quasi-3-D behavior. It captures ESD physics of the device without accounting for 3-D effects like current filamentation or nonuniform self-heating along the width. On the other hand, multi-Fin simulation is performed to capture true 3-D phenomena,

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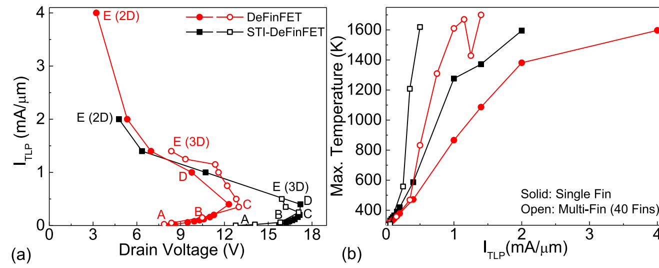

Fig. 3. (a) TLP I–V and (b) maximum lattice temperature versus pulse current behavior of DeFinFET and STI-DeFinFET, extracted using 3-D TCAD simulation of single-Fin and multi-Fin devices. Failure threshold is considered as current when lattice temperature exceeds 1600 K.

such as nonuniform turn-on, current filamentation, filament spreading, and local hot spot formation. TLP I–V depicts the following distinct states, existent in both DeFinFET and STI-DeFinFET: A: avalanche breakdown; B: device turn-on with a high resistance state; C: onset of voltage snapback (V_{t1}); D: snapback or negative differential resistance region, and E: failure threshold (I_{t2}). The respective current and voltage values to achieve these states ($A - E$), however, depend on the device design/architecture (DeFinFET or STI-DeFinFET) and nature of simulation (quasi-2-D or 3-D). For instance, DeFinFET has avalanche breakdown (A), device turn-on (B), and onset of snapback (C) at lower voltages when compared to STI-DeFinFET. The respective currents are the same. Furthermore, DeFinFET experiences an observable snapback (D) with failure (E) at higher current than STI-DeFinFET. STI-DeFinFET, however, fails immediately after the onset of snapback, which leads to merger of states C, D, and E in STI-DeFinFET. Moreover, Fig. 3(a) shows that till point C single-Fin and multi-Fin characteristics are identical/superimposed, which drifts after point C, that is, onset of snapback. Fig. 3(b) shows that STI-DeFinFET experiences higher self-heating, for a given current, when compared to DeFinFET. This is attributed to its higher voltage-handling capability, that is, higher voltage drop for a given injected ESD current, which results into higher power density across STI-DeFinFET. This eventually leads to higher self-heating for a given TLP current. It should also be noted that between states C and E, single Fin simulation underestimates the self-heating across the device, for both DeFinFET and STI-DeFinFET, which highlights the presence of strong 3-D effects after the onset of snapback (point C) and justifies the need for multi-Fin investigations. Moreover, while STI-DeFinFET has a sharp rise in lattice temperature after the snapback, DeFinFET experiences a drop in lattice temperature after experiencing a peak value before thermal failure. These observations with ESD physics of these devices are elaborated in detail in subsequent sections. Keeping these observations in mind, states from A to C are studied using single-Fin simulations, however states right after C are studied using multi-Fin simulations.

IV. ESD Physics: Steady-State Behavior

Fig. 4 shows conduction current density across DeFinFET and STI-DeFinFET at points A and B of the TLP curve.

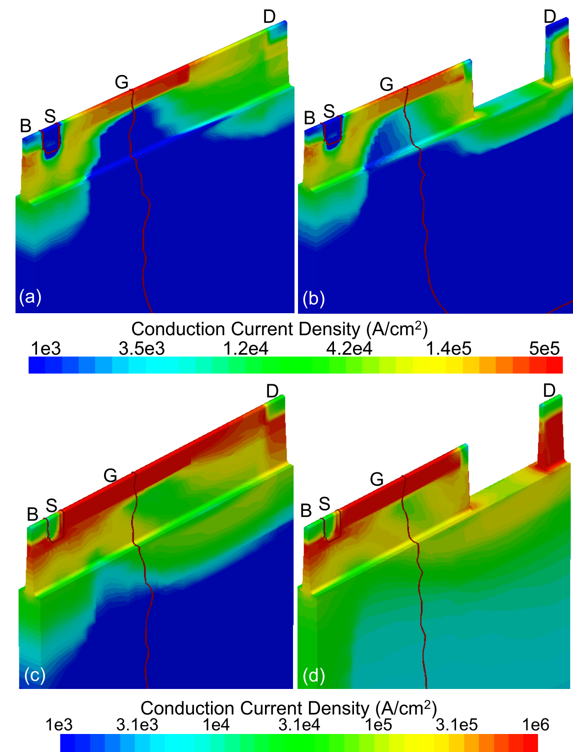

Fig. 4. Conduction current density across (a) and (c) DeFinFET and (b) and (d) STI-DeFinFET at point A, that is, junction breakdown (a) and (b) and point B, that is, parasitic bipolar turn-on (c) and (d). At A: $I_{TLP} = 1$ μA/μm and at B: $I_{TLP} = 200$ μA/μm.

Under low current injection condition, that is, after the junction breakdown, conduction current contributed by impact ionization was found to be confined in the active fin region, under the gate and in between drain and bulk contact regions. Impact ionization-generated electrons and holes are collected by the drain and bulk contacts, respectively. Absence of current through the source contact (emitter of parasitic n-p-n) signifies missing bipolar action for currents less than current at point B (at B: $I_{TLP} = 200$ μA/μm). After point B, current is found to be primarily confined between the drain and source contacts, which shows strong n-p-n action in DeFinFET and STI-DeFinFET. It should be noted that the onset of parasitic bipolar in DeFinFET and STI-DeFinFET required the same TLP current, which is due to identical construction of the source side region (emitter and base region of parasitic n-p-n) of the two DeFinFET variants.

Fig. 5 shows the electric field distribution across DeFinFET and STI-DeFinFET after the bipolar turn-on Fig. 5(a) and (b) and at the verge of snapback Fig. 5(c) and (d), that is, point C. At I_{TLP} less than current at point C, the peak electric field was confined to the gate overlap region. The same shifts under the drain contact as soon as injected current exceeds the current at point C. This can be explained in Fig. 6(a), which shows the onset of space charge modulation at point C. As soon as the injected carrier density exceeds the background (N-well) doping, the positive space charge in the N-well region, near the well junction, gets disturbed due to excess negative charges. This leads to a shift in the peak electric field next to highly doped drain contact region. Moreover, due to

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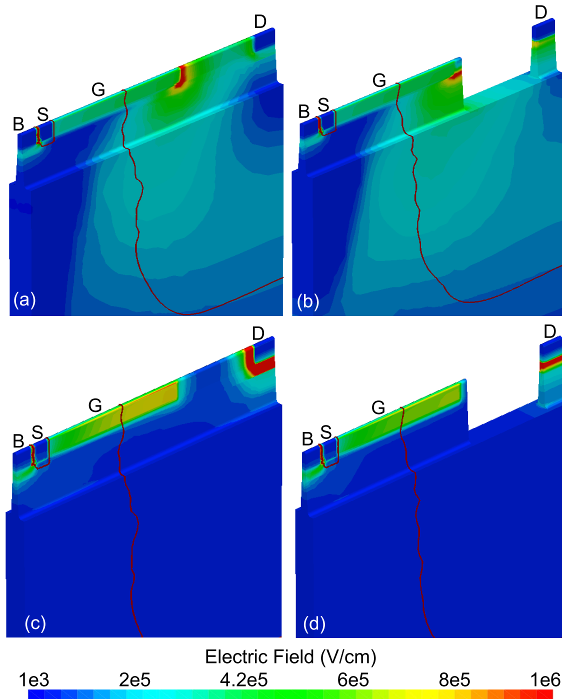

Fig. 5. Absolute electric field across (a) and (c) DeFinFET and (b) and (d) STI-DeFinFET after parasitic bipolar triggering (a) and (b) and at the verge of voltage snapback (c) and (d), that is, point C.

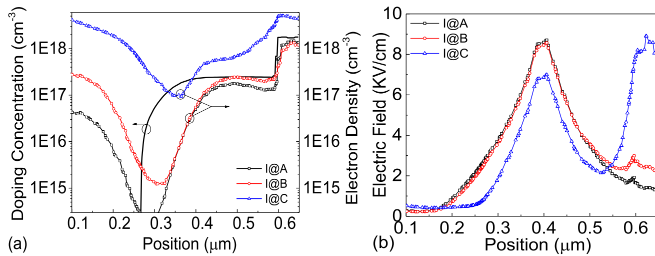

Fig. 6. (a) N-well doping concentration plotted with electron density in the N-well region for different injected TLP currents depicting (b) shift in the peak electric field from the gate edge to the drain edge due to space charge modulation.

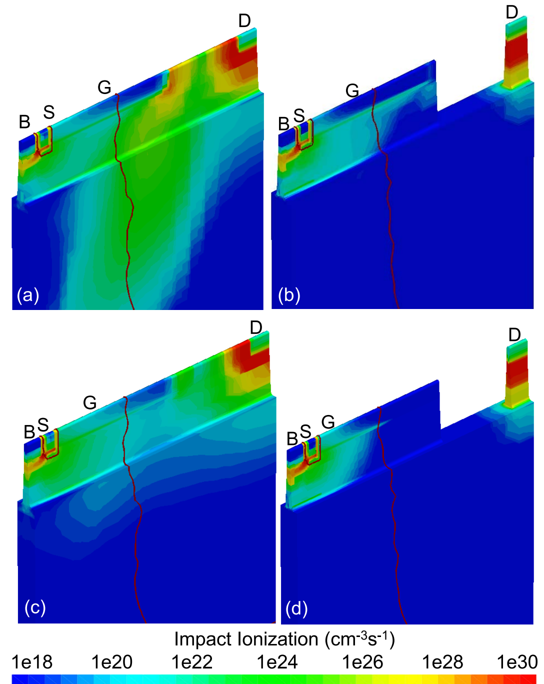

Fig. 7. Impact ionization rate across (a) and (c) DeFinFET and (b) and (d) STI-DeFinFET after parasitic bipolar triggering (a) and (b) and at the verge of voltage snapback (c) and (d), that is, point C.

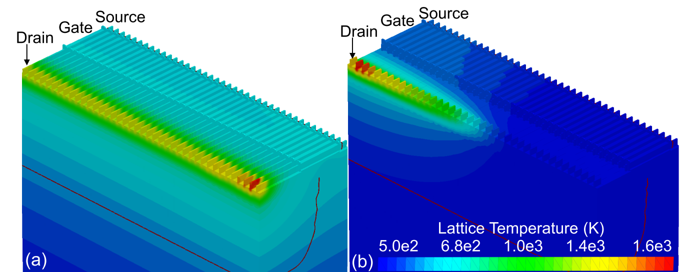

Fig. 8. Lattice temperature at the verge of failure in multi-Fin (a) DeFinFET (extracted at $t = 90$ ns) and (b) STI-DeFinFET (extracted at $t = 60$ ns). This state is depicted as region R_4 in Fig. 10. Note: here 40 fins were used for 3-D TCAD simulations to account for 3-D/multi-Fin effects.

localization of the space charge into a narrow region around the drain contact, the space charge density increases, which in turn also increases the peak electric field value (near the drain contact) compared to the peak electric field value at the gate edge before space charge modulation. As a result of the increase in the peak electric field after space charge modulation, the impact ionization rate increases significantly (Fig. 7), which leads to voltage snapback (i.e., region D) for the same injected current. This is because a lesser voltage can sustain the conduction, after space charge modulation, by generating the required impact ionization generated excess carriers. The voltage snapback adjusts the peak electric field to the same peak value as it was at the gate edge before space charge modulation. This behavior is depicted in Fig. 6(b). It should be noted that the localization of the peak electric field near the drain contact region also leads to electron mobility degradation, as explained in our earlier works [6], [7], which leads to current filamentation.

As observed in the TLP characteristics, depicted in Fig. 3, both DeFinFET and STI-DeFinFET experience a thermal failure after snapback. It is worth noting that the lattice temperature increases abruptly after the snapback. Fig. 8 shows the lattice temperature across multi-Fin (no of Fins: $N_F = 40$) configuration of Fig. 8(a) DeFinFET and Fig. 8(b) STI-DeFinFET. A localized hot spot along the width of the device is apparent from Fig. 8. Attributed to this localized failure, DeFinFETs undergo catastrophic failure immediately after snapback. It is, however, worth noting that while the hot spot is extremely localized across few Fins at one of the corner in the case of STI-DeFinFET, the same in the case of DeFinFET appears to have a spread across large number of Fins. This behavior will be discussed in detail in later sections.

V. Dynamic Behavior: Physics of Current Filamentation

Fig. 9(a) and (b) shows the drain voltage, source current, and substrate current as a function of stress time for DeFinFET and STI-DeFinFET, respectively. Here (and in

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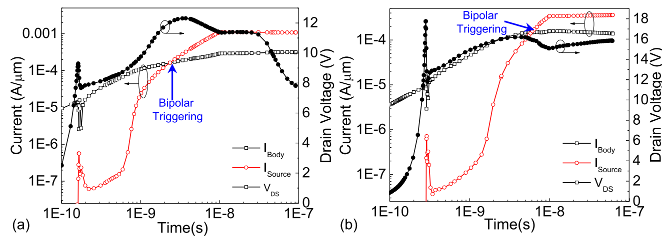

Fig. 9. Drain voltage, source current, and substrate current as a function of stress time for (a) DeFinFET and (b) STI-DeFinFET. Here, 40 fins were used for 3-D TCAD simulations to account for 3-D/multi-Fin effects. $I_{TLP} = 1.25$ and 0.5 mA/μm was used for DeFinFET and STI-DeFinFET, respectively.

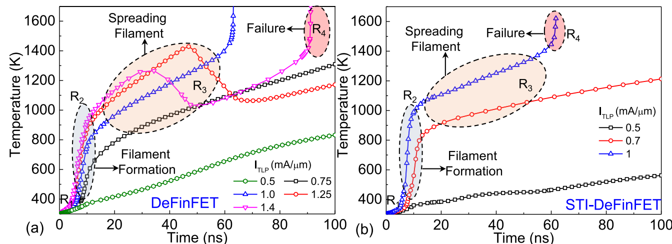

Fig. 10. Lattice temperature, extracted for different TLP current values, as a function of stress time for (a) DeFinFET and (b) STI-DeFinFET. Here, 40 fins were used for 3-D TCAD simulations to account for 3-D/multi-Fin effects.

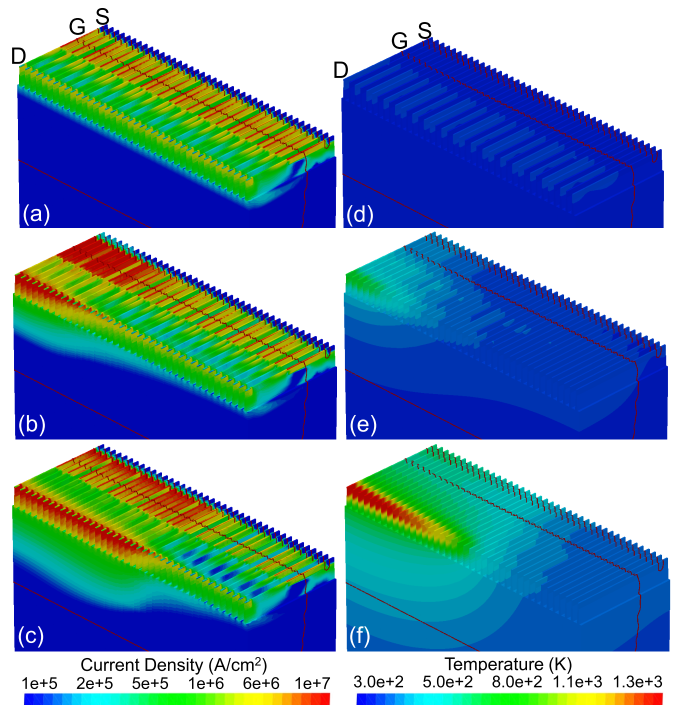

Fig. 11. (a)–(c) Conduction current density and (d)–(f) lattice temperature extracted across multi-Fin ($N_F = 40$) DeFinFET devices showing: (a) and (d) uniform current conduction and lattice heating along the width after parasitic bipolar turn-on (and before space charge modulation), which is depicted as R_1 in Fig. 10(a). (b) and (e) Filament formation immediately after space charge modulation causing abrupt increase in temperature, which is depicted as R_2 in Fig. 10(a), (c), and (f) filament spreading causing slower rate of lattice heating than region R_2 and then drop in temperature due to relaxed current density inside the filament, which is depicted as R_3 in Fig. 10(a). Here, 40 fins were used for 3-D TCAD simulations to account for 3-D/multi-Fin effects.

subsequent simulations), 40 fins were used for 3-D TCAD simulations to account for 3-D/multi-Fin effects. It shows that when DeFinFET (STI-DeFinFET) was stressed at $I_{TLP} = It_2$, the source current, that is, the emitter current of parasitic bipolar, was always lesser than the body (base) current till stress times =2 ns (=8 ns). However, for stress time greater than 2 ns (8 ns), the source current exceeds the body current significantly. This behavior signifies that the parasitic bipolar turn-on in DeFinFET (STI-DeFinFET) takes place at 2 ns (8 ns). This is also the point when a minor snapback is observed in the transient drain voltage characteristics. This first snapback is due to bipolar turn-on. Furthermore, the transient drain voltage characteristics show another snapback at longer stress time which is attributed to space charge modulation. This is the time when current filament forms. Clearly, the parasitic bipolar is triggered much earlier than the time when space charge modulation takes place. Therefore, it can be concluded that space charge modulation is apparently the root cause of current filamentation, not parasitic bipolar turn-on. We will explore this further in subsequent discussions.

Fig. 10(a) and (b) shows lattice temperature, extracted for different TLP current values, as a function of stress time for DeFinFET and STI-DeFinFET, respectively. Here, four distinct regions are presented, that is, $R_1 - R_4$. Figs. 11 and 12 show the conduction current density and lattice temperature extracted across multi-Fin ($N_F = 40$) DeFinFET and STI-DeFinFET, respectively, for these distinct states. R_1 [Figs. 11(a) and (d) and 12(a) and (d)]: uniform conduction, which is a state when the current flows uniformly across the device, hence the temperature increases linearly with time in this state. R_2 [Figs. 11(b) and (e) and 12(b) and (e)]: filament formation, which is a state when the current flows nonuniformly across the device width by getting localized across a few Fins. This localization of current increases lattice temperature inside filament (T_F) abruptly with time. R_2 is followed by region R_3 [Figs. 11(c) and (f) and 12(c) and (f)] when the filament tends to spread along the width, which relaxes the current density across the device/Fins. In R_3, the increase in lattice temperature is slower than what it was in region R_2. In the case of DeFinFET, drop in lattice temperature, for higher stress current values, after experiencing a certain critical temperature (T_{CRIT}), is also observed. In these cases, the filament spreading was faster than the lattice heating, due to faster bipolar turn-on in DeFinFET at higher currents, which relaxes the peak temperature across the devices. However, in STI-DeFinFET at all currents and in DeFinFETs at moderate currents, since the bipolar turn-on was slower, the lattice temperature continues to increase with time despite the presence of filament spreading. Here, filament spreading was slower than rate at which lattice temperature increases. In R_3, temperature inside the filament continues to increase, which when exceeds the critical temperature for thermal runaway ($T_{TR\text{-}CRIT}$) leads to rapid increase in lattice temperature. This results in filament temperature exceeding temperature for catastrophic fail (T_{FAIL}). As a result, finally the device experiences thermal failure due to excessive lattice heating, which is region R_4.

The filament formation and spreading behavior is further closely depicted in Fig. 13 showing conduction current density

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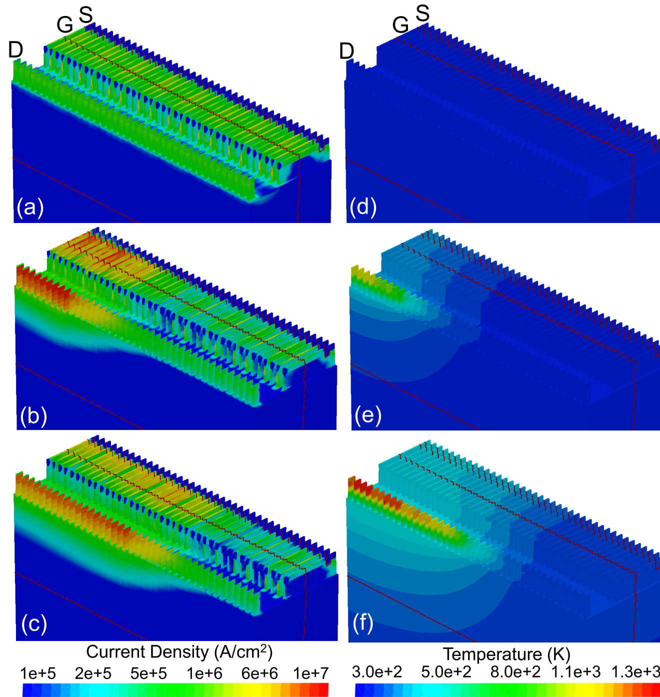

Fig. 12. (a)–(c) Conduction current density and (d)–(f) lattice temperature extracted across a multi-Fin ($N_F = 40$) STI-DeFinFET device showing: (a) and (d) uniform current conduction and lattice heating along the width after parasitic bipolar turn-on (and before space charge modulation), which is depicted as R_1 in Fig. 10(b). (b) and (e) Filament formation immediately after space charge modulation causing abrupt increase in temperature, which is depicted as R_2 in Fig. 10(b), (c), and (f) filament spreading causing slower rate of lattice heating than region R_2 and then drop in temperature due to relaxed current density inside the filament, which is depicted as R_3 in Fig. 10(b). Here, 40 fins were used for 3-D TCAD simulations to account for 3-D/multi-Fin effects.

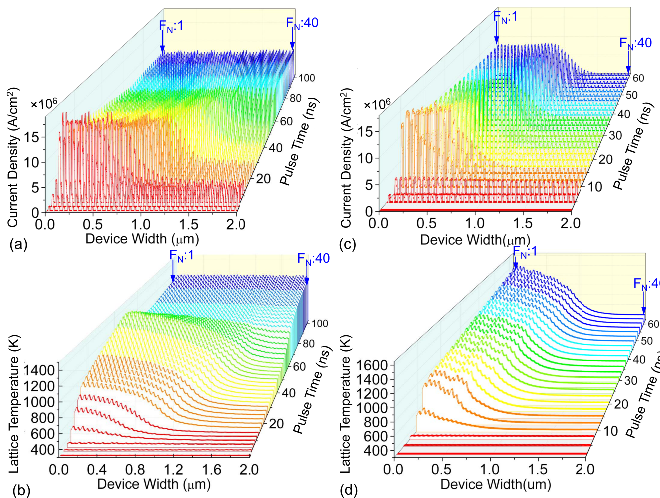

Fig. 13. (a) and (c) Conduction current density and (b) and (d) lattice temperature along the device width, as a function of pulse stress time for (a) and (b) DeFinFET and (c) and (d) STI-DeFinFET. Here, 40 fins were used for 3-D TCAD simulations to account for 3-D/multi-Fin effects. Injected stress current was kept the same as I_{t2}, that is, 1.25 mA/μm for DeFinFET and 0.5 mA/μm for STI-DeFinFET.

Fig. 13(a) and (c) and lattice temperature Fig. 13(b) and (d) along the device width, as a function of pulse stress time for DeFinFET and STI-DeFinFET. Fig. 13 shows uniform current conduction and lattice heating for an initial duration; subsequently, a nonuniform conduction or filament formation can be seen, which localizes the current across a limited number of Fins across a given corner of the device. This resulted in a sharp increase in lattice temperature inside the filament. After filament formation, filament spreading is evident. In DeFinFET, the filament spreads faster than the same in STI-DeFinFET. As a result, DeFinFET experiences uniform conduction, at longer stress times, after filament formation and drop in lattice temperature after reaching a peak, whereas STI-DeFinFET has a linear rise in lattice temperature, at longer stress times, due to slow filament spreading. Fig. 14 shows the maximum lattice temperature extracted from a single Fin simulation, which shows the missing regions R_2, R_3, and R_4 (i.e., filament formation, filament spreading, and failure, respectively). This validates strong 3-D effects responsible for behavior explained for $R_2 - R_4$ above.

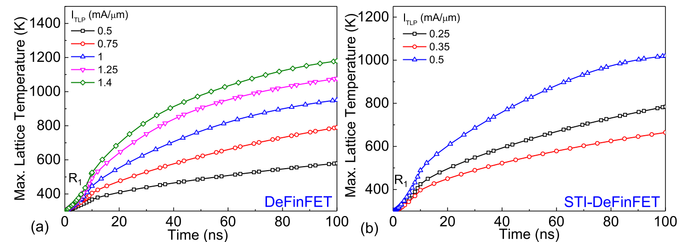

Fig. 14. Lattice temperature, extracted for different TLP current values, as a function of stress time for single Fin (a) DeFinFET and (b) STI-DeFinFET. Here, single Fin was used for simulations to avoid 3-D/multi-Fin effects.

The rate at which the filament spreads depends on bipolar efficiency, which in turn depends on the number of excess carriers generated and intrinsic bipolar efficiency of the parasitic path. The number of excess carriers generated after filament formation depends on the current density (C_{D}). Therefore, the filament having higher filament density would spread faster than the filament having lower filament density. This explains why DeFinFET experiences faster filament spreading and drop in lattice temperature for higher stress currents, that is, the current density inside the filament (C_{D}) is greater than the critical current density (C_{CRIT}). Whereas for lower stress current (i.e., $C_{\mathrm{D}} < C_{\mathrm{CRIT}}$), DeFinFET does not experience drop in lattice temperature despite filament spreading, which is due to slower filament spreading. Similarly, in STI-DeFinFET, due to intrinsically weaker parasitic bipolar, lattice temperature continue to increase despite filament spreading.

Physics of filament formation and filament spreading is explained in Fig. 15. Fig. 15(a)–(c) depicts the electric field, electron mobility, and impact ionization rate, respectively, along the width of DeFinFET, as a function of pulse stress time, extracted under the drain contact. The electric field around the drain contact after space charge modulation increases sharply with respect to time, which leads to a significant drop in electron mobility and increase in impact ionization. This leads to formation of current filament as a balancing act to sustain current conduction [6]. Formation of current filament gives rise to charge density inside the filament, which screens the electric field and avoids further increase in the electric field. This allows electron mobility to recover and sustains current conduction [15].

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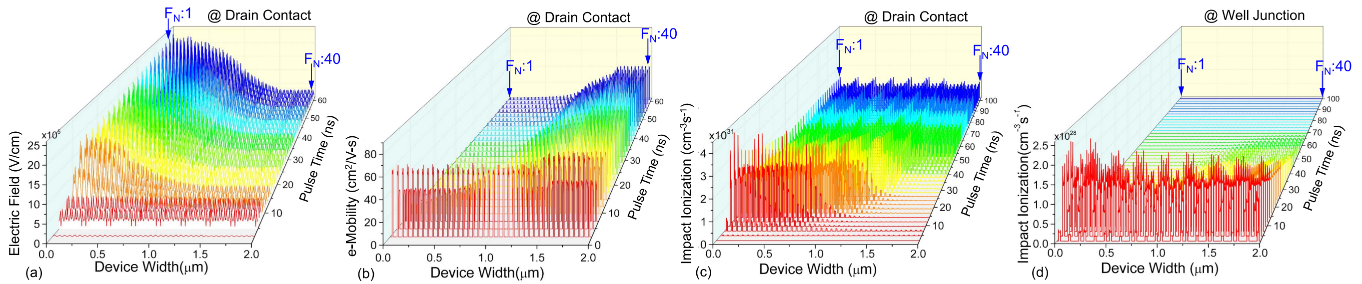

Fig. 15. (a) Electric field, (b) electron mobility, and (c) impact ionization rate along the device width, extracted under drain contact, as a function of pulse stress time for DeFinFET. (d) Rate along the device width, extracted at well junction, as a function of pulse stress time for DeFinFET. Here, 40 fins were used for 3-D TCAD simulations to account for 3-D/multi-Fin effects. Injected stress current was kept the same as I_{t2}, that is, 1.25 mA/μm for DeFinFET.

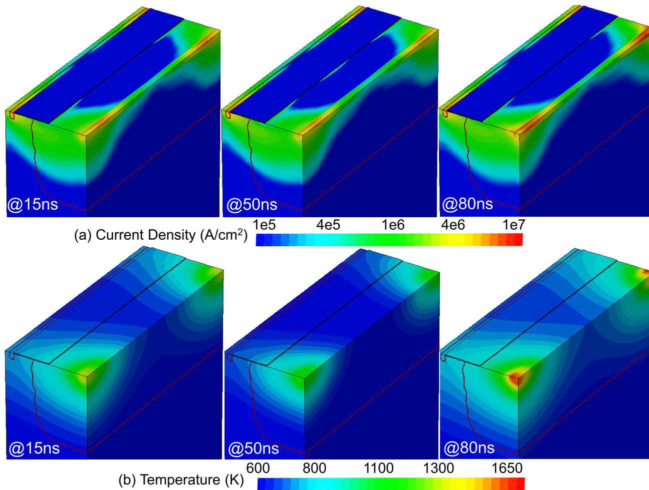

Fig. 16. (a) Conduction current density and (b) maximum lattice temperature contour, extracted as a function of stress time for $I_{TLP} = I_{t2}$, for a planar DeMOS device while keeping the design/technology parameters same as DeFinFET.

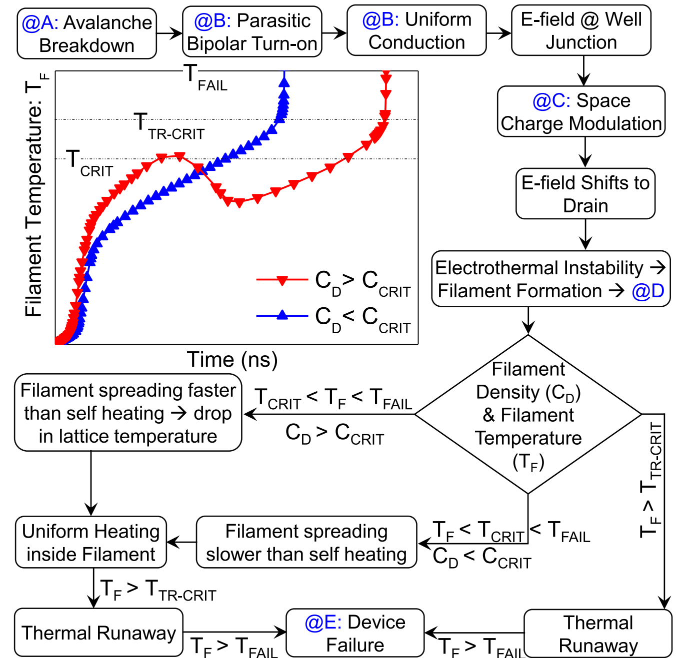

Fig. 17. Chart summarizing physics of high current behavior, current filament dynamics, and failure in DeFinFET devices under ESD stress condition.

Fig. 15(c) and (d) shows the uniform impact ionization inside the filament under the drain contact and the absence of impact ionization at the well junction after filament formation. This signifies that unlike planar DeMOS cases [9], where filament spreading is attributed to higher impact ionization outside the filament, at well junction, in the case of DeFinFET, filament spreading is attributed to Fin-based construction of DeFinFETs. This is validated in Fig. 16 which shows the static filament in the case of a planar DeMOS device for exactly the same layout design, device dimensions, and well profile as used for DeFinFET. Fig. 16 signifies that filament spreading in DeFinFET is attributed to Fin-based construction. Physical insights into filament spreading in DeFinFETs are summarized in Section VI.

VI. Summary of Mechanisms

In summary, the ESD behavior of both STI-type and non-STI-type DeFinFET devices, as summarized in Fig. 17, is studied in this article. At lower current, excess carrier generation after avalanche breakdown triggers the parasitic bipolar. The current required for bipolar turn-on was found to be the same in both the devices due to identical source–body side construction. However, the turn-on time for DeFinFET was smaller than the same for STI-DeFinFET, which is attributed to the difference in hole current density posed by the difference in device footprint and device architecture. After bipolar turn-on, the onset of space charge modulation leads to a shift in the peak electric field from well junction to the drain contact. The field confinement near the drain contact and increase in the peak field value leads to increased impact ionization, which causes voltage snapback. Moreover, the increased electric field leads to mobility degradation near the drain contact, which causes electrothermal instability and formation of current filament. Increased carrier density inside the filament screens the electric field, which helps recover majority carrier mobility and sustain the current conduction after filament formation. Spreading nature of the filament was discovered in DeFinFETs, which was attributed to Fin-based construction of DeFinFETs. The same was validated from the absence of filament spreading seen in the case of a planar DeMOS device while keeping the same layout design and well profiles. The rate at which the filament spreads was found to be dependent on the number of excess carriers generated after filament formation and intrinsic bipolar efficiency of the parasitic bipolar. The filament having higher filament density was found to spread faster, as far as the filament

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temperature does not exceed critical temperature to trigger thermal fail. Attributed to this, DeFinFET experiences faster filament spreading and drop in lattice temperature when the current density inside the filament was greater than the critical current density. Whereas for moderate stress current in DeFinFETs and due to slower bipolar turn-on in STI-DeFinFETs, drop in lattice temperature was missing during filament spreading. Finally, when lattice temperature exceeds critical temperature to trigger thermal fail, a sharp increase in lattice temperature leads to catastrophic failure in DeFinFET devices under high current stress conditions.

VII. Conclusion

A clear difference between the findings from single-Fin and multi-Fin analysis is seen. DeFinFETs were found to have strong 3-D effects under high current injection conditions. The filament formation is attributed to electrothermal instability after space charge modulation. Therefore, the onset of filament formation and current density inside the filament depends on N-well doping density, its profile, and drain side construction. For a layout and well design, while planar DeMOS has static filaments, DeFinFETs, on the other hand, due to Fin-based construction, have spreading nature of filaments. In DeFinFETs, the rate at which the filament spreads depends on turn-on time of the parasitic bipolar and current density inside the filament. It is, therefore, imperative that DeFinFETs are designed keeping filament dynamics/spreading in mind to maximize its high current-handling capability. The key design parameters to maximize the ESD robustness of DeFinFETs are L_{EXT} and DL. In the case of STI-DeFinFETs, increasing DL improves I_{t2} and lowers R_{ON}. Whereas in non-STI DeFinFETs, increasing DL increases V_{t1} and I_{t1} with marginal improvement in I_{t2}. As far as L_{EXT} is concerned, it does not affect I_{t2} initially; however, a very large L_{EXT} may reduce I_{t1} and I_{t2} with increased V_{t1}. On the other hand, a short L_{EXT} will lower the breakdown voltage as well as V_{t1}, without any serious change in I_{t2}. The % change in I_{t1}, I_{t2}, and V_{t1} as a function of L_{EXT} strongly depends on the N-well doping.

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