Time Dependent Shift in SOA Boundary and Early Breakdown of Epi-Stack in AlGaN/ GaN HEMTs Under Fast Cyclic Transient Stress

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***Abstract*—This experimental study reports first observations of (i) SOA boundary shift in AlGaN/GaN HEMTs and (ii) early time-to-fail of vertical AlGaN/GaN epi-stack under fast changing (sub-10ns rise time) cyclic pulse transient stress, which otherwise qualified for 600 V DC stress. It is shown that a epi stack qualified for 10 years lifetime under DC stress, fails faster under cyclic transient stress. The drain-to-substrate leakage exhibits different trends under DC and pulse stress. Integrated electrical and mechanical stress characterization routine involving Raman/ PL mapping, PFM and CL spectroscopy along with atomistic simulations reveals material limited unique failure physics under transient stress condition. Failure analysis using cross-sectional SEM and TEM investigations reveal signature of different degradation and failure mechanism under transient and DC stress conditions. A failure model is proposed for rapid breakdown of AlGaN/GaN epi-stack under cyclic transient stress and it is experimentally validated.**

***Index Terms*—GaN HEMT, pulse switching stress, safe operating area, time dependent breakdown, fatigue, trapping.**

I. Introduction

AlGaN/GaN HEMTs promise superior switching performance than their Si counterparts. However, their reliability, in particular, under switching conditions is less explored [1]. In a typical power converter, during OFF-cycle the high blocking voltage appears at drain, as shown later in Fig. 1(a) which introduces significant drain-to-gate lateral stress and enormous drain-to-substrate vertical stress. While the corresponding time dependent failure physics has been widely studied, but it is limited however to DC like stress [2]–[6]. For example, at low DC stress, drain-to-substrate leakage occurs via charge hopping [5] and threaded dislocations in buffer, exhibiting Ohmic behaviour [6]. Under high DC stress, Poole-Frenkel emission from buffer traps, dictates conduction [4], resulting in faster increase in buffer leakage and gradual failure of AlGaN/GaN epi-stack on Si. Breakdown voltage of the stack drops at higher temperatures and confirms absence of Avalanche triggered failure [4]. Time-to-Failure (TTF) of AlGaN/GaN epi-stack exhibits exponential dependence on DC stress voltage, indicating presence of field driven failure mechanism [6]. Under DC stress, the high drain-to-substrate unidirectional electric field introduces enormous piezoelectric biaxial strain in AlGaN/GaN stack layers which generates defects to form current percolation paths between drain and substrate and eventually lead to soft breakdown of AlGaN/GaN epi-stack [6]. However, in power switching converters the stress is not constant unlike under DC, instead the stresses are cyclic and transient in nature as shown later in Fig. 1(a). Therefore, to encourage widespread adoption of AlGaN/GaN HEMTs in power conversion, it is crucial to understand the failure mechanisms and estimate their actual lifetimes under practiccal switching conditions [1], [7]–[10]. This work is an extension of our earlier study [11]. It aims to contribute to the existing understanding of OFF-state stress reliability of GaN HEMT, however under fast and cyclic pulse transient conditions. Drain-to-substrate vertical stress is imposed on HEMT devices while emulating real converter circuit like stress scenario. Variation in TTF, with pulse voltage and pulse rise-time is recorded and lifetime of AlGaN/GaN epi-stack is estimated. Comprehensive material-device co-investigations are done using integrated electrical, optical and material characterization techniques for on-the-fly study of degradation physics. Variation in device parameters is recorded and temporal evolution of mechanical strain and trap distribution is captured. Implications of OFF-state transient stress on device's Safe Operating Area (SOA) and shift in SOA boundary is studied under accumulative stress. Atomistic simulations are done to gain physical insight into stress at molecular level. The underlying degradation physics is investigated, and a unique failure model for AlGaN/GaN epi-stack under pulse switching stress is proposed and experimentally validated. This manuscript is organized as follows; Section II presents details of device design/fabrication and

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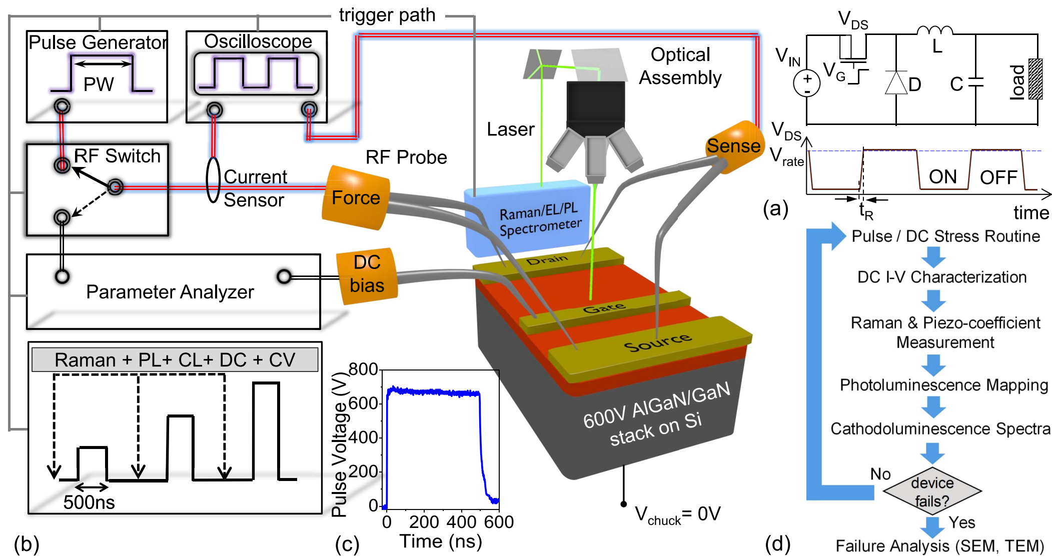

Fig. 1. (a) Schematic representation of buck power converter along with drain voltage (V_{DS}) waveform during switching. (b) Schematic of experimental set-up with integrated Raman, PL and sub-μs pulse generator used for on-the-fly electrical and material characterization of HEMT/epi-stack under stress. (c) Waveform of pulse stress voltage as applied at drain. (d) Flowchart depicting sequence of characterization steps performed during pulse and DC stress.

characterization set-up. Results in Section III highlight the SOA boundary shift as observed in AlGaN/GaN HEMT under pulse switching stress. Section IV discloses the time dependent breakdown of AlGaN/GaN epi-stack and rapid degradation in HEMT under drain-to-substrate pulse stress. In Section V, the physics of time dependent breakdown of epi-stack and SOA boundary shift in AlGaN/GaN HEMT under pulse switching stress is presented. Based on the new findings a failure model is proposed and experimentally validated. Finally, the key learnings and conclusive remarks are drawn in Section VI.

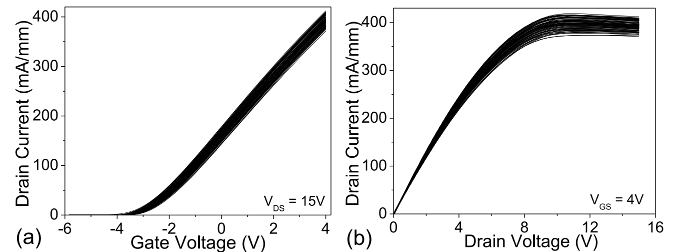

Fig. 2. DC (a) Transfer characteristics and (b) output characteristics of devices which were developed in-house on 600 V DC qualified AlGaN/GaN epi-stack.

II. Device Under Test and Experimental Set-Up

In this work, two classes of HEMT devices were used; (i) commercially available E-mode (p-GaN gate) GaN HEMT and (ii) In-house developed GaN HEMT. In-house, HEMT devices were realized on a commercial grade AlGaN/GaN stack grown on 6-inch p-type Si (111) substrate and is qualified for 600 V operation with 10-year lifetime. The epitaxial stack consists of 150 nm AlN nucleation layer, 1 μm linearly graded AlGaN transition region, 3 μm C-doped GaN buffer, 250 nm unintentionally doped GaN region above C-doped GaN buffer and 22 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The epitaxial stack was capped with a 40 nm thick *in-situ* grown SiN. 100 μm wide HEMTs with 3 μm gate length and 25 μm source-to-drain distance were fabricated. Source and drain pads were realized from Ti/Al/Ni/Au metal stack which was deposited using e-beam evaporation and later annealed at ~870 °C to make Ohmic contact with the two-dimensional electron gas (2DEG). AlGaN barrier in gate region, was partial recessed using O_2/BCl_3 based atomic layer etching. Post gate dielectric deposition and dielectric anneal, Ni/Au gate metal stack was deposited and soft annealed at ~400 °C. On wafer, devices were MESA isolated using $Cl_2/Ar/BCl_3$ chemistry based Inductively Coupled Plasma - Reactive Ion Etching. All the devices were surface passivated with 50 nm in situ SiN. 160 devices per die were fabricated and the processed run had more than 90% device yield with less than ± 5% variation. DC I-V characteristics of a set of in-house developed HEMTs are shown in Fig. 2. As evident from Fig. 2(a), the devices exhibit threshold voltage; V_{GS} of −3 V and I_{ON} of ~375 mA/mm with less than ± 5% variation.

The experimental set-up used in this work is shown in Fig. 1(b). It was developed by integrating electrical, optical and material characterization techniques, which allows on-the-fly device-material co-study while device is under pulse cyclic and transient stress. The cyclic and transient stress, as encountered in a DC-DC buck converter, was emulated using rectangular pulses of a fixed pulse width (500 ns) as depicted in Fig. 1(c). Pulse rise time was varied in sub-10ns range, which is typical in GaN based power converters. An OFF period of 1 s was introduced between two consecutive pulses to allow reasonable time for the device to relax. Devices were also tested under constant DC stress to understand the difference in their degradation mechanisms under DC and pulse transient stress. To record the evolution of device degradation under stress, the electrical stress routine (DC or

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pulse) was interrupted at regular intervals, in each case and the change in electrical as well as material parameters of the device was recorded. Following measurements were carried out to monitor changes in parameters: (i) drain-to-substrate vertical leakage current was measured after each stress pulse and its hysteresis behaviour was recorded at regular intervals. (ii) Device's DC characteristics were measured and change in its ON-resistance (R_{ON}), ON-current (I_{ON}) and threshold voltage (V_{TH}) was determined at regular intervals. In region between source and drain (iii) μ-Raman mapping was done to record change in piezoelectric strain distribution, (iv) UV-Photoluminescence (PL) mapping is done to capture newly formed trap levels and their corresponding spatial distribution. (v) Cathodoluminescence (CL) spectra was measured in regions which showed high PL intensity of blue and yellow luminescence defect bands, at different stress time. CL depth profiling [12] was done to determine the exact location of defected regions within the epitaxial stack. At high e-field, mechanical stress generates across the active region of device due to the piezoelectric nature of GaN. The evolution of mechanical stress distribution was captured using visible Raman ($\lambda = 532$ nm) where, a positive shift in GaN's E_{2H} peak (567.5 cm^{-1}) indicates compressive strain whereas a negative shift points to tensile strain in GaN devices [13]. The defects density distribution was determined using PL with UV($\lambda = 325$ nm) excitation from a He-Cd laser. After device failure SEM and TEM analysis was done to gain physical insight into the breakdown mechanism. The characterization routine as followed is summarized in the flowchart shown in Fig. 1(d).

III. SOA Characterization and Stress Dependent SOA Shift

A. SOA Characterization

To bench mark the observations, first the commercial E-mode GaN HEMT was characterized and its SOA boundary was extracted under pulse condition. Drain was pulsed with gate DC biased, while source and substrate were grounded. After each pulse, the drain-to-source linear current (I_{DC}) was spot measured (at 1 V DC) immediately after the pulse goes OFF, to record change, if any, due to the applied stress. For each gate bias, V_{DS} was increased in step size of 1 V, till the device's breakdown point, which marked the SOA boundary. Figure 3(a) shows the measured pulse I-V characteristics of the device, depicting its SOA boundary. I_{DC} decreased with increase in pulse drain voltage as seen in Fig. 3(b), which is due to trapping induced degradation [1]. A maximum degradation of up to ∼100% was observed under OFF-state whereas a relatively lower change in I_{DC} was seen in ON-state. These observations highlight that the OFF-state stress is the worst-case scenario for device. During the OFF-state, maximum voltage stress appears from drain-to-substrate along with drain-to-gate. This high stress condition occurs periodically during the OFF-cycle of the power converter as illustrated in Fig. 1(a). Therefore, this work hereafter focuses on drain-to-substrate cyclic pulse stress in AlGaN/GaN HEMT and its implications on device's SOA and reliability.

B. Stress Dependent SOA Shift

Next, the SOA boundary of the commercial E-mode HEMT was monitored under drain-to-substrate pulse stress. A high voltage (180V) pulse train with 500ns pulse width and 1ns rise time was stressed at drain with substrate grounded, while keeping gate and source floating. In this configuration, the AlGaN/GaN epi-stack gets stressed. A capacitor is hard tied between gate and ground, next to the probe/pad, to avoid the unwanted voltage induction from drain-to-gate [14]. We would like to highlight that despite the worst-case scenario considered here, by connecting gate hard tied to ground potential, no change in gate current was observed during drain stress, which signifies that the failure behavior discussed in subsequent sections is not influenced by field near gate.

Each time, a set of five devices was pre-stressed at 180 V for a certain number of pulses. After the stress, the corresponding SOA boundary was determined. The number of pulse stress cycles was increased in the subsequent device sets. Figure 3(c) shows device's SOA boundary extracted under increasing number of pulses from 0 (which refers to the pristine device) to 30000. A shift in SOA boundary is observed under cyclic pulse stress. SOA shrinks with increase in number of stress cycles of fixed amplitude. This is unusual as such a SOA shift does not exist in conventional Si power devices and was never explored earlier for AlGaN/GaN HEMT. Such unwanted shift in SOA boundary with time, during the switching operation can impose serious reliability challenge to GaN HEMTs in power switching applications. Hence, it is crucial to understand the underlying physics of SOA degradation.

IV. Time Dependent Vertical Breakdown and Degradation Under Pulse Stress

A. Time Dependent Breakdown of AlGaN/GaN Epi-stack

As, discussed in previous section, the drain-to-substrate pulse voltage, stresses the AlGaN/GaN epi-stack in HEMT over the time, during power conversion. So, it is important to understand, the epi-stack degradation and its time dependent failure mechanism under pulse stress and understand how different it is from epi-stack failure under DC. To accomplish this, in-house developed HEMT was used. Lifetime of AlGaN/GaN epi-stack in HEMT, was determined at different stress voltages, both under DC and pulse stress conditions. In each case, voltage stress was applied at drain while substrate was grounded. The drain-to-substrate leakage current (I_{leak}) was continuously monitored during the stress. I_{leak} increased under stress. When it achieved 1 μA/mm value, the epitaxial stack was considered failed. The corresponding time taken to fail the stack, is termed as time-to-fail (TTF). TTF of AlGaN/GaN epi-stack varied with DC stress voltage as shown in Fig. 4(a). At 600 V DC stress, the stack shows a 10 year lifetime. An exponential dependence of TTF on applied stress voltage is observed which indicates electric field driven failure of AlGaN/GaN epi-stack [6]. Under DC stress, I_{leak} increases gradually with time as shown in Fig. 5(a) and indicates soft-failure of AlGaN/GaN epi-stack.

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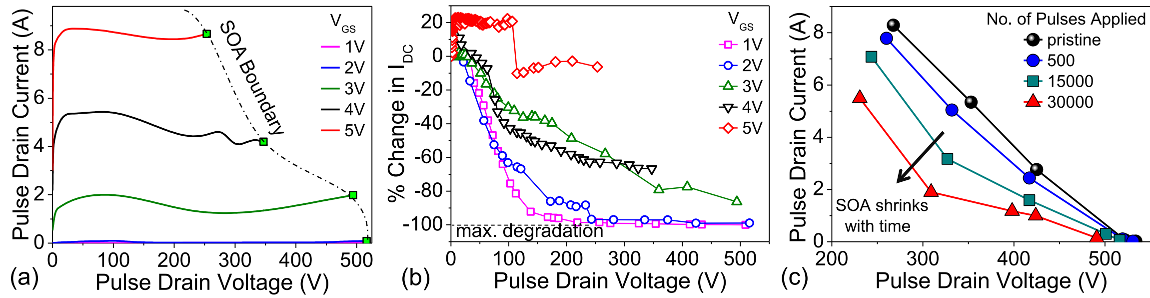

Fig. 3. (a) Pulse I-V characteristics depicting SOA boundary of a commercially available E-mode GaN HEMT. (b) Percentage change in linear drain-source current (I_{DC}) measured after each voltage pulse. Device shows highest degradation in OFF state stress condition. (c) SOA of commercial e-mode GaN HEMT, extracted at different stages of OFF-state stress cycles. Shift in SOA boundary with increasing number of stress pulses can be seen.

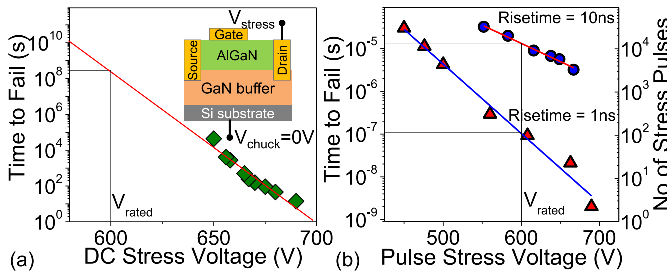

Fig. 4. (a) Time-to-fail (TTF) for the AlGaN/GaN epi-stack used in this work demonstrating 10-year lifetime for 600 V DC stress. (b) TTF under pulse stress is presented on left y-axis and the corresponding number of pulses required for epi-stack failure is shown on right y-axis.

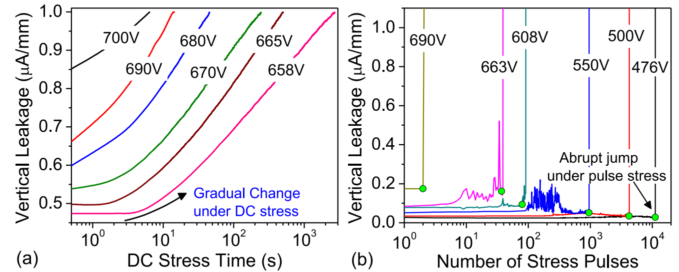

Fig. 5. Time evolution of drain-to-substrate vertical leakage current at different (a) DC stress voltages and (b) pulse voltages.

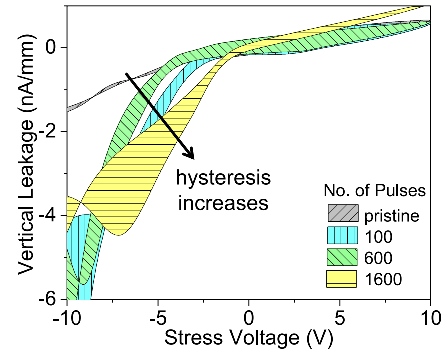

Fig. 6. Hysteresis behavior recorded in drain-to-substrate leakage current after different number of stress cycles applied at drain.

Next, voltage pulses of a fixed amplitude, each of 500 ns pulse width and 1 ns rise time, were applied on the AlGaN/GaN epi-stack. The corresponding TTF is shown in Fig. 4(b). TTF shows exponential dependence on the applied pulse stress similar to that under DC stress, indicating electric field dependent failure. However, TTF was found to be much smaller than that under DC stress. For instance, the 600 V AlGaN/GaN epi-stack which was qualified for 10-year lifetime under DC stress, failed only within 100 pulses. Further, the experiment was repeated with stress pulses of higher rise time. Interestingly, TTF was found to improve by two orders when pulse rise time was increased from 1 ns to 10 ns. This observation indicates that the time dependent rapid failure of AlGaN/GaN epi-stack under pulse stress, is indeed also related to the rate of change of electrical stress or the slew rate (dV/dt) of the applied stress pulse. The time evolution of I_{leak} under different pulse stress voltages is shown in Fig. 5(b). Unlike the DC stress case (Fig. 5a), I_{leak} remained intact over time under cyclic pulse stress, till the verge of epi-stack failure. On failure, I_{leak} increased abruptly beyond 1 μA/mm, indicating a hard failure of AlGaN/GaN epi-stack. Furthermore, just before failure I_{leak} turned noisy. Noise in leakage current originates from defect/trap generation in AlGaN/GaN epi-stack [2] However, no noise was observed in leakage under DC stress as depicted in Fig. 5(a). To confirm the presence of trap generation in epi-stack under pulse stress, hysteresis in I_{leak} was studied. Figure 6 shows the change in hysteresis behavior of I_{leak} with increasing number of stress pulses/cycles. Pristine device showed negligible hysteresis as evident from insignificant loop area of black curve in Fig. 6. However, a consistent increment in hysteresis area can be noticed with increase in number of stress cycles. This observation points to; (i) increased charge accumulation via trapping in different regions of bulk GaN with each stress pulse. Electrons trapped by deep-levels in buffer region, undergo slow de-trapping which leads to negative charge accumulation in epi-stack with increasing stress cycles. (ii) increased density of new defects in bulk GaN which further participate in electron trapping. Both these phenomena translate to increased hysteresis under pulse cyclic stress.

B. HEMT Degradation Under Pulse Stress

As discussed above, the cyclic pulse transient stress across AlGaN/GaN epi-stack increases defects density and charge accumulation in buffer as well as transition regions of HEMT. Trapping in different regions of device has significant influence

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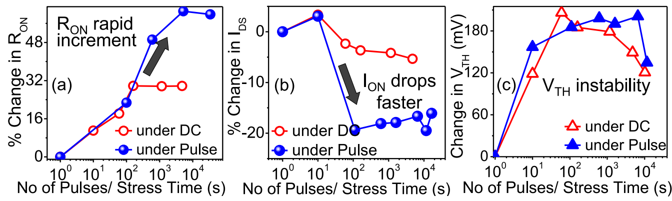

Fig. 7. Degradation in device parameters, recorded on-the-fly during DC and pulse stress measurements done at 180 V. (a) R_{ON} increases and (b) I_{ON} drops at a much faster rate under pulse stress than under DC stress. (c) Significant V_{TH} shift is observed in both the cases.

on device performance and reliability [1]. Change in device parameters was recorded from DC I-V characterization done at regular intervals during the stress routines, as discussed in Section II. Figure 7 presents a comparison of the change in ON-resistance (R_{ON}), ON-current (I_{ON}) and threshold voltage (V_{TH}) under pulse and DC stress. Rapid and more sever changes in device parameters are observed under pulse stress compared to that in DC stress case. For instance, with only 100 pulses applied at drain, R_{ON} was found to increase by 25 %, I_{ON} dropped by 20 % and V_{TH} shift of 180 mV was recorded.

C. Spatial and Temporal Evolution of Traps

Defects generated under cyclic pulse stress in AlGaN/GaN epi-stack layers. Electrically active defects or traps deteriorated the device performance as highlighted above. However, it is still not very clear, (i) where these trap levels are located within the GaN bandgap, (ii) how they are spatially distributed across the device and (iii) what is their temporal evolution under pulse stress. To understand these aspects, PL mapping of device's active region was done at regular intervals during the pulse stress routine. PL mapping of drain-source region revealed that the increased defect generation introduces deep level traps within defect band 425-525 nm (E_C - 0.48 to E_C - 1.14 eV). Also, the PL intensity, which is a direct measure of the trap density, was recorded as shown in Fig. 8. Pristine device exhibits a relatively uniform PL intensity distribution (Fig. 8a). PL intensity increases with number of stress pulses (Fig. 8b). However, it becomes non-uniform at the verge of failure with the highest PL intensity observed near the drain contact (which was under cyclic pulse stress) as in Fig. 8(c). Therefore, Fig. 8 reveals that the density of mid-bandgap defects (425-525 nm), increases with number of pulses with peak concentration close to the drain contact edge. CL spectra is taken at the location of highest PL intensity near the drain, after different number of stress pulses as shown in Fig. 9(a). It shows an increase in Blue (BL) and Yellow luminescence (YL) intensities with stress pulses which confirms the presence of mid-bandgap defects. CL profiling reveals penetration depth of $\sim$1.2 μm from top surface [12]. Hence, it is confirmed that theses mid-bandgap defects are located in GaN buffer, 1.2 μm below the device surface near the drain contact. Raman map is captured between source-drain region of the device before and after the stress routines as in Fig. 10. A residual stress is observed in the recessed region under gate in pristine device (before stress) as seen in Fig. 10(a). A significant compressive stress builds up at the drain contact edge after the device is stressed with 5000 pulse cycles as shown in Fig. 10(b) and it is different from the strain distribution obtained under DC stress condition, as evident from Fig. 10(c). The stress signature received, is from the GaN buffer which correlates well with penetration depth (1.2 μm) determined from CL measurements.

D. Degradation of Piezoelectric Nature and Epi-Stack Failure

Strain accumulation in GaN buffer region underneath drain contact can possibly be a manifestation of physical change in material quality and nature. To verify this, the piezoelectric coefficient (d_{33}) which is responsible for biaxial strain in AlGaN/GaN stack, is spot measured after a fixed number of stress cycles. The measurement is done across twenty five equally spaced points along the device width near the drain end, using Piezo-response Force Microscopy (PMF). Figure 9(b) shows percentage change in d_{33} as recorded, with increasing number of stress cycles. Device stressed with 1 ns rise time pulse, suffered early drop in d_{33}, however increase in rise time to 10 ns delayed the degradation in d_{33}. This observation indicates, that the very fundamental piezoelectric nature of AlGaN/GaN epi-stack changes under pulse stress. However, what triggered the change in piezo-coefficients in AlGaN/GaN epi-stack? To understand the root cause, failure analysis of damaged regions of devices was done. Figure 11 shows the post failure SEM images of a device which catastrophically failed within 100 pulses of 600 V each. Top view SEM image of failed device reveals failure occurred with massive crack in the gate-drain region (Fig. 11a). Cross-sectional SEM is done along the line 'a-b' at the damaged drain edge and is shown in Fig. 11(b).

It reveals that the damage reaches 1.4 μm deep into the GaN buffer. The region underneath the damage is scanned using a high resolution-TEM. The HR-TEM image of the region is shown in Fig. 11(c). It depicts presence of multiple cracks at the interface of GaN-buffer/AlGaN-transition-region, just below the damaged region. On the other hand, in the devices which failed under DC stress, no failure signature is observed in the bulk and the damage is localized to the device surface as depicted in Fig. 12(a)–(b). TEM cross-section of damaged region taken along line 'a-b' (Fig. 12c) reveals a network of dislocations with no visible damage in epi-stack. Dislocations are intrinsic to AlGaN/GaN stack grown on foreign substrate and are present in pristine (unstressed) device as well. Figure 13 shows TEM image of buffer region of a pristine device. From these observations is can be concluded that the failure under DC stress occurred due to dislocations which act as current leakage path [5].

To understand the root cause of cracking at GaN-buffer/transition-region interface, atomistic simulation is done using QuantumATK computational package. For computational ease, GaN/AlN interface is considered where GaN is a part of buffer and AlN is a part of transition-region. A super cell of GaN/AlN interface is created and optimized with

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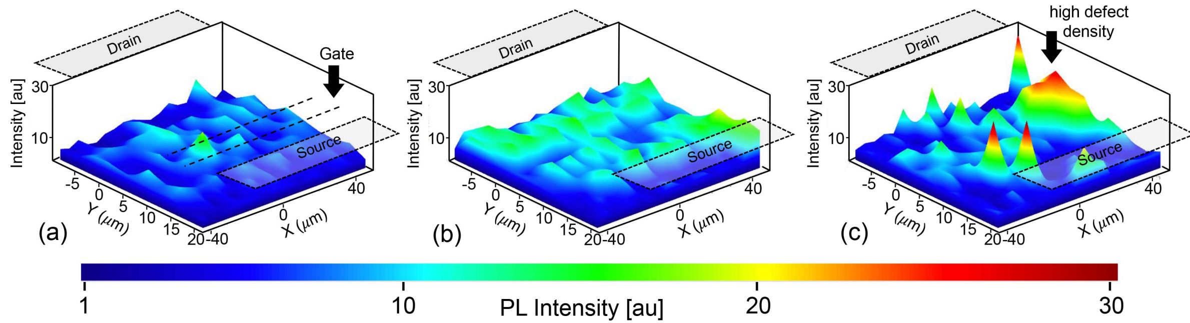

Fig. 8. PL intensity distribution for defect band (425-525 nm) captured between source-drain region of the HEMT device (a) before stress, (b) after stressing with 5000 pulses and (c) at the verge of failure.

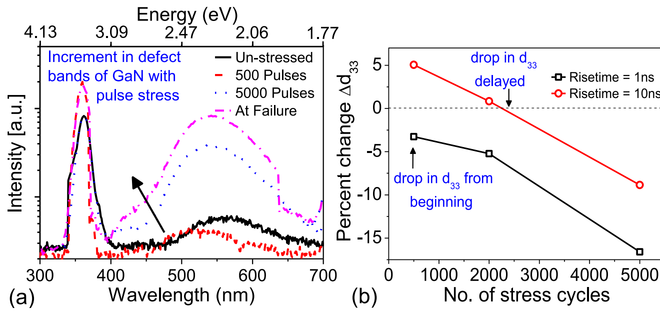

Fig. 9. (a) CL spectra of GaN captured in drain contact vicinity where highest PL intensity was observed. (b) Percentage change recorded in piezoelectric coefficient d_{33} with increasing number of stress cycles. Drop in d_{33} is delayed when pulse rise time is increased from 1 ns to 10 ns.

0.01 eV/Å force tolerance and 0.001 eV/Å3 stress tolerance. Local Density Approximation (LDA) exchange-correlation function is used to improve computational efficiency with 10x10x1 k point sampling and density mess cut-off of 45 Hartree. Electric field was applied across GaN/AlN normal to the interface plane in the module as shown in Fig. 14(a) top. The DFT computation results presented in Fig. 14(a) show the distribution of normal component of electric field; E_z (left y-axis) and change in total force; ΔF (right y-axis) experienced by individual *Ga*, *Al* and *N* atoms within the GaN/AlN system. The periodic fluctuation in electric field/force as seen in bulk of GaN and AlN, originates from the periodic potential of *Ga*, *Al* and *N* atom arrangement along c-axis of the crystal. ΔF varies from GaN to AlN with maximum change at the GaN/AlN interface. The maximum increment in force occurs at the interface as the electric field component peaks close to the interface. Therefore, the GaN/AlN interface undergoes maximum stress (force per unit area) during pulse switching and eventually it develops micro-cracks (Fig. 11c).

V. Discussion and New Physical Insights

A. Understanding Failure Under Cyclic Transient Stress

Under drain-to-substrate DC stress, the AlGaN/GaN epi-stack failure occurs via percolation paths between drain and substrate, formed by defect generation and their activation at high electric field [3]. However, the defect percolation theory, which is originally borrowed from the conventional gate dielectric failure model, cannot explain significantly reduced TTF, its dependence on pulse rise time (Fig. 4 b) and aggressive catastrophic failure of device (Fig. 11) under cyclic pulse transient stress. These newly discovered trends and findings in fact, suggest a presence of an electrical shock based fatigue phenomenon which is responsible for time dependent AlGaN/GaN epi-stack failure under pulse stress. This can be explained as following; when a voltage pulse is applied across the AlGaN/GaN epi-stack, vertical component of electric field (E_Z) introduces in-plain piezoelectric strain (σ_{xy}) [15];

$$\sigma_{xy} = \left(e_{33}\frac{C_{13}}{C_{33}} - e_{31}\right)E_z \tag{1}$$

where, e_{33}, e_{31} are piezoelectric coefficients and, C_{13}, C_{33} elastic stiffness tensors. The generated strain creates new defects in bulk region, in drain contact vicinity, where peak field lies and accumulates with increasing number of stress pulses (Fig. 10b). Furthermore, the piezoelectric AlGaN/GaN epi-stack undergoes cyclic loading via mechanical strain generation-relaxation, under pulse stress as evident from the Raman map, captured before and after pulse stress (Fig. 10a-b). Over the time, cyclic stress introduces changes in piezoelectric nature (Fig. 9b) and results in time dependent strain variation [16] as;

$$\sigma_{XY}(t) = \sigma_0\left(1 - e^{\frac{-t}{\tau}}\right) \tag{2}$$

Such electrically developed fatigue under cyclic electrical loading, was observed in other piezoelectric materials too [17]. Furthermore, the electrical fatigue generated, keeps accumulating in device with each stress pulse, as evident from increased YL, BL bands in CL spectra (Fig. 9a) and increased hysteresis (Fig. 6) over time. Hence, electrical fatigue is accumulative in nature. Moreover, the GaN-buffer/AlGaN-transition-region interface experiences maximum stress (Fig. 14a) under applied electric field. Over the time, the electrical fatigue nucleates micro-cracks at GaN-buffer/AlGaN-transition-region interface (Fig. 11c). High strain energy at crack tip, under cyclic electrical loading, propagates it towards device top and hits the surface to form pits and causes catastrophic failure as seen in Fig. 11(a). On failure, abrupt increase in localized current density, melts drain contact metal and develops crack in top AlGaN barrier due to thermal stress generated from the associated heating [10]. Then molten metal diffuses and migrates via crack [18]. Fatigue accumulation accelerates with rate of change of electric field (pulse rise time) possibly because the

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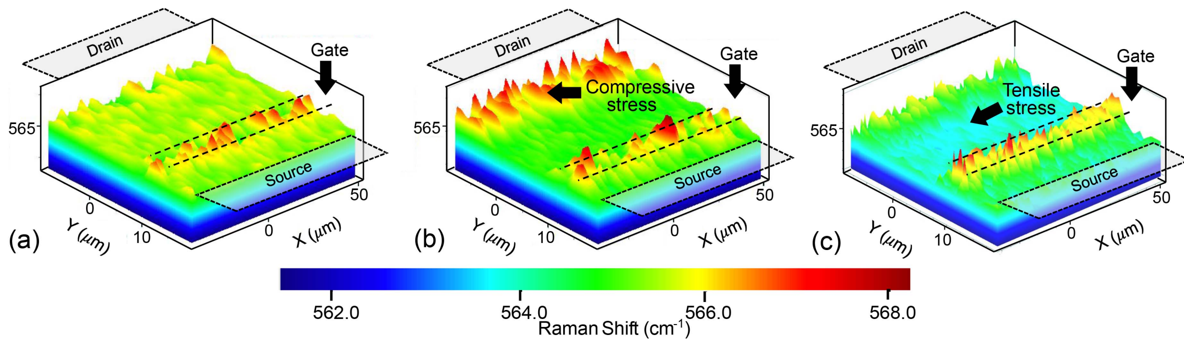

Fig. 10. (a) Raman map captured in region between source - drain in (a) pristine device (before stress) , (b) after application of 5000 stress pulses and (c) at the end of 2.5 hours of DC stress.

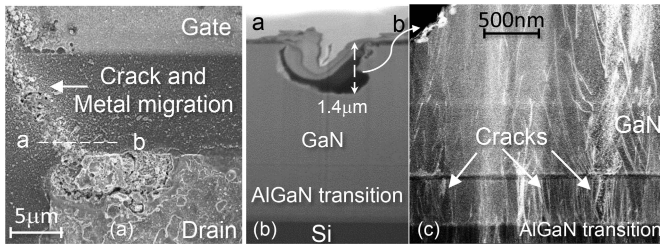

Fig. 11. (a) Top view SEM image depicting HEMT failure under 600 V drain-to-substrate pulse stress. (b) Cross-sectional SEM taken along line 'a-b' in (a). (c) HR-TEM image of the region below the damaged area in (b).

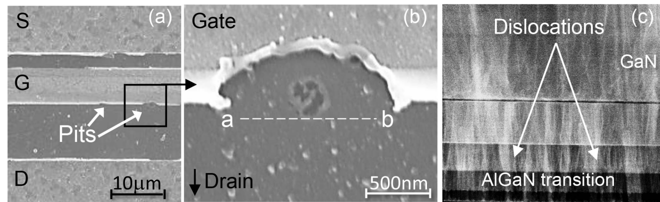

Fig. 12. (a)-(b) Top view SEM images of HEMT device failed after 600 V of DC stress. (c) Cross-sectional TEM along line 'a-b' in (b).

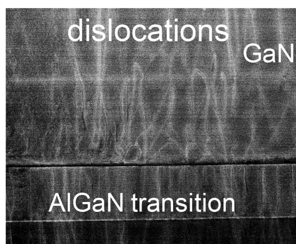

Fig. 13. TEM image of epi-stack in pristine device, taken under the drain contact depicting intrinsic dislocation density.

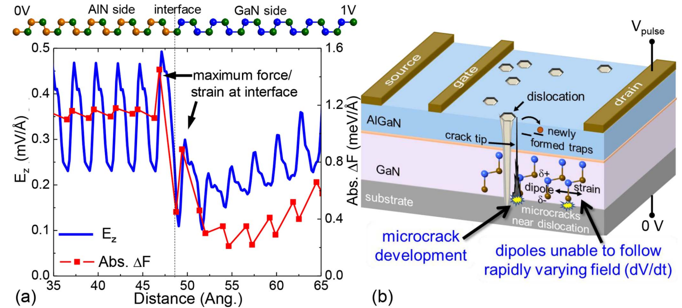

Fig. 14. (a) Simulated electric field and change in total force, experienced by individual atoms in GaN/AlN system under 1 V stress applied on GaN side. (b) Schematic illustrating the failure physics under pulse transient stress.

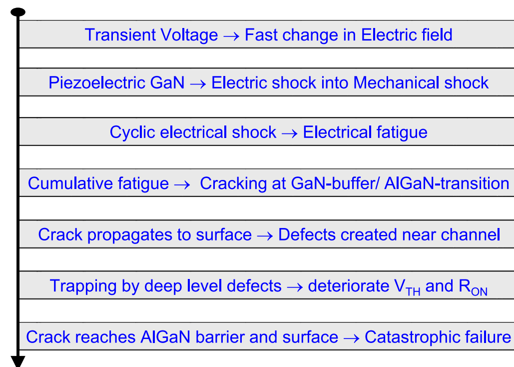

Fig. 15. Sequence of events involved in time dependent breakdown of AlGaN epi-stack and shift in SOA boundary of HEMT, under fast cyclic pulse stress.

intrinsic dipoles are unable to follow the rapidly changing field and get strained and assist in micro-crack development as illustrated in Fig. 14(b). This results in drop in TTF for faster cyclic transients (Fig. 4b). It should be noted that the proposed failure model is applicable only for time dependent failure of AlGaN/GaN epi-stack under pulse transient stress.

B. Validation of Proposed Failure Model

Figure 15 presents a sequence of events which constitute the proposed failure model of AlGaN/GaN epi-stack under pulse transient stress. As discussed above, the electrical cyclic loading under pulse condition, causes stress accumulation and defect generation via compressive piezoelectric strain in GaN buffer and transition region. To validate the proposed argument, a device was stressed with 5000 pulse cycles at drain before its Raman map was captured. A significant compressive stress gets accumulated around drain contact (Fig. 16a). Subsequently, the stressed device is heated at 373K for 10 mins followed by Raman mapping. Raman profile depicts that after heating, the compressive stress at drain relaxes (Fig. 16b). Heating in device introduces thermoelastic tensile stress which partially compensates compressive stress [19]. This improvement should be reflected in TTF of AlGaN/GaN epi-stack. To verify this, GaN epi-stack is pulse stressed at 373K and

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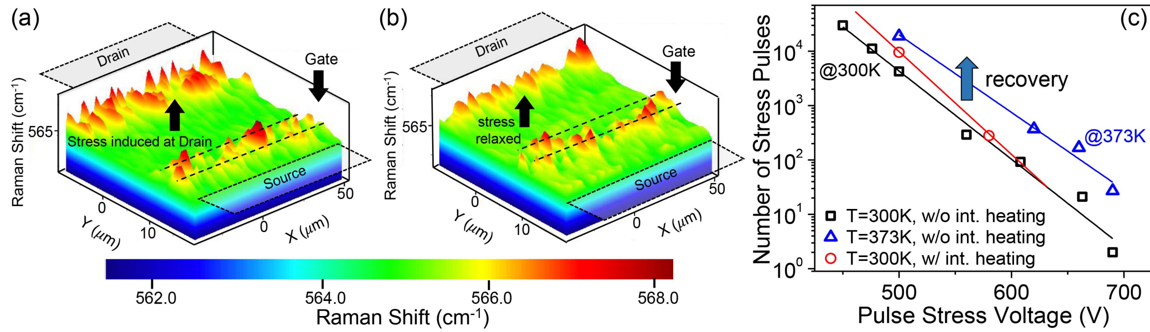

Fig. 16. (a) Raman map of device after it is stressed with 5000 pulses (b) Raman map captured, after the device was heated at 373K post pulse stress. (c) Variation in TTF of AlGaN/GaN epi-stack under pulse stress, recorded at different temperature treatment. Heating improves TTF.

its TTF is extracted. In another experiment, AlGaN/GaN epi-stack is pulse stressed and intermediate heat treatment (373K) is given to it. Figure 16(c) shows the TTF of AlGaN/GaN epi-stack extracted at different temperature under pulses stress. TTF improved with heat treatment (Fig. 16c), which validates the proposed failure model.

VI. Conclusion

Shift in SOA boundary of AlGaN/GaN HEMT is discovered under pulse stress. Vertical drain-to-substrate breakdown in AlGaN/GaN epi-stack under fast and cyclic pulse stress was found to obey a different degradation physics than under DC stress. TTF extracted for AlGaN/GaN epi-stack from fast, cyclic pulse stress measurements did not obey the lifetime predicted by DC stress. Time to fail, under pulse stress showed exponential dependence on stress voltage, which however increased with pulse rise time or temperature. Cyclic electrical loading invoked electric fatigue in buffer. Defect density increased in buffer with stress time due to accumulative nature of fatigue. Increased deep level defects deteriorated device performance. Under pulse stress, cracks nucleated at GaN-buffer/AlGaN-transition-region interface, due mechanical stress enhancement at interface and triggered device failure. Failure under DC stress occurred close to device surface and with no signature of damage in bulk GaN.

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