The Japan Society
of Applied Physics

REGULAR PAPER

Nano-second timescale drain voltage induced electrical instabilities in hydrogenated amorphous silicon thin film transistors

View the article online for updates and enhancements.

REGULAR PAPER

Nano-second timescale drain voltage induced electrical instabilities in hydrogenated amorphous silicon thin film transistors

Rajat Sinha[1,2*] [iD], Prasenjit Bhattacharya[3], Sanjiv Sambandan[3,4], and Mayank Shrivastava[1]

[1]Department of Electronic System Engineering, Indian Institute of Science, Bangalore, Karnataka 560012, India
[2]Centre for Nano Science and Engineering, Indian Institute of Science, Bangalore, Karnataka 560012, India
[3]Department of Instrumentation and Applied Physics, Indian Institute of Science, Bangalore, Karnataka 560012, India
[4]Department of Engineering, University of Cambridge, Cambridge CB2 1TN, United Kingdom

*E-mail: rajatsinha.bit@gmail.com

In this work, we study the device degradation of a-Si:H thin film transistors upon application of high frequency nano-second timescale pulse stress on the drain contact. Degradation mechanisms at different field stress levels have been investigated using real-time current–voltage, capacitance–voltage and Raman spectroscopy measurements. A positive V_T shift under moderate electric field stress followed by a V_T recovery (negative shift) at high drain fields has been observed. Spatial variance in the degradation has been studied. A variance in the degradation mechanism from the hot to cold contact is observed. No material changes are observed, confirmed through Raman spectroscopy as the field stress is applied. The role of self-heating in degradation is studied by varying the pulse width of the field stress in nano-seconds range. Finally, the impact of thermal and gate bias anneal on V_T shift has been investigated through electrical measurements in a recursive stress-anneal cycle.
© 2020 The Japan Society of Applied Physics

Supplementary material for this article is available online

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) based thin film transistors (TFTs) have found usage in numerous applications including image sensors,[1–3] solar cells,[4] active matrix liquid crystal displays[5–7] and owing to their low-temperature fabrication, in flexible electronics applications.[8–11] a-Si:H TFTs have also been used in active matrix organic light emitting diode displays due to their uniform and low-cost fabrication process.[5]

However, device reliability is an important consideration in a-Si:H devices. A reliable operation is important to ensure the applicability of a technology and is a direct consequence of the stability of it's constituent devices. This makes the exploration of device instability behavior necessary for proper implementation of the technology. Threshold voltage (V_T) shift is an instability behavior that can have a significant negative impact on the performance of a-Si:H devices. Gate bias induced V_T shift in a-Si:H TFTs has been studied extensively, with the physics of the instability explained through either defect state creation in insulator-channel interface[12–17] or charge trapping in the gate dielectric[18–21] and has been modeled for circuit applications as well.[22,23] While studies have also been done to understand the V_T shift instability caused due to DC stress application on drain contact,[24,25] a similar thorough investigation has been missing in case of drain induced instability phenomenon under pulse stress conditions in these devices.[26,27]

With the application of field stress across the a-Si:H channel, optical phonons are generated in the-Si:H layer (optical phonon energy in a-Si:H is 58 meV). A dense distribution of optical phonons could lead to a complex instability behavior, which would not be observed at a low-field stress condition and present an unique instability behavior. To efficiently investigate the instability behavior at varying field conditions, where phonon behavior can assume significance, it is important that the electrical stress is applied for a short interval so as to not cause excessive self-

heating. Application of field stress in the time scales comparable to thermal diffusion time allows us to understand the potential role of phonons in the instability phenomenon. Investigation of high-field instability behavior also allows for probing the device behavior as a potential protection element in circuits and systems. This also leverages the investigation of instability behavior at ultra high frequencies, which could be of potential interest involving high frequency applications.

In the course of this work, we have studied the instability behavior of a-Si:H TFTs under varying field conditions through the application of nano-second timescale field stress at the drain contact. The instability behavior, in this work, has been characterized using TFTs with inverted-staggered configuration through current–voltage (I–V), capacitance–voltage (C–V) and Raman spectroscopy measurements. C–V hysteresis measurements are performed to further investigate the physics of device degradation. Thermal and gate bias anneal are performed to investigate the device degradation and the recovery mechanism. Material changes taking place in the a-Si:H under stress are investigated using Raman spectrosocpy.

2. Experimental details

Devices used in the course of this work have an inverted-staggered configuration and have been fabricated in-house (Fig. 1). The devices are based on glass substrate and have an aluminum–chromium gate contact. A 200 nm thick silicon nitride (SiN_x) layer is used as the gate dielectric and is deposited using a plasma enhanced chemical vapor deposition (PECVD) technique. A 150 nm thick a-Si:H layer is used as the active layer and is also deposited using PECVD. A 30 nm thick, highly n-doped a-Si:H layer, deposited through PECVD as well, is used to create an ohmic contact between the semiconductor and metal contacts. Finally, these layers are etched using a reactive ion etch process. A DC sputtering process is then used to deposit the aluminum–molybdenum source/drain contact, which are subsequently etched using a wet etch process. Further details of the fabrication process
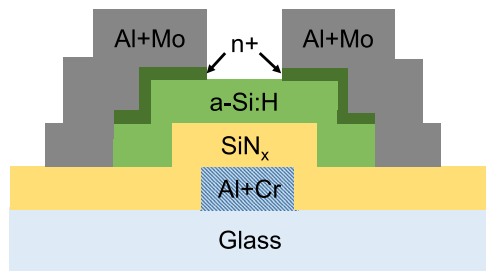
Fig. 1. (Color online) Cross section view of the inverted staggered back channel etch a-Si:H TFT used in this work.

have been discussed in the supplementary material, which is available online at stacks.iop.org/JJAP/59/074004/mmedia. It is also worth mentioning that in some cases, devices with a 300 nm thick SiN_x top passivation are also used. However, no qualitative changes are observed in device degradation behavior.

Exploration of nano-second timescale stress induced degradation is done using the experimental setup shown in the Fig. 2. A pulse generator capable of supplying voltage levels upto 2 kV with pulse widths ranging from 1 ns to 1.5 μs is used to apply the desired pulse stress to the device under test (DUT) through a 50 Ω transmission line. The pulse setup also comprises of a Keithley 4200-SCS parameter analyser used to measure any changes in the device behavior in the aftermath of pulse stress through a series of current–voltage (I–V) and capacitance–voltage (C–V) characterization. A LabRam HR raman setup is also used to characterize any material changes in the active layer using a 532 nm DPSS laser with a spot size of 1.18 μm. The device current under the pulse voltage is sensed using a current sensor and the device voltage and current waveforms are captured using

a high bandwidth digital phosphor oscilloscope. Further discussions on the pulse generation setup are presented in the supplementary material. The devices are stressed by applying a pulse voltage at the drain contact while the source and gate are kept grounded ($V_G = V_S = 0$ V). A voltage pulse with a pre-determined amplitude, rise time and pulse width is applied and is followed by an off-time of 500 ms, which is provided to allow device reach thermal equillibrium. In the course of this work, the voltage stress pulse initiates at 0.5 V and has a step size of 0.5 V [shown in Fig. 2(b)]. The next pulse is then applied with similar width and higher amplitude i.e. 0.5 V higher than last pulse. The voltage stress is then stopped once a pre-determined stress level is reached and a series of DC I–V, C–V and Raman measurements are done. A pulse of width 100 ns and a rise/fall time of 10 ns is used, unless stated otherwise. It is also worth noting that although, the devices used in this work have a similar back channel configuration, there are variations in channel dimensions and the same have been mentioned in the corresponding figures.

3. Results and discussion

Figure 3 depicts the DC I–V characteristics of the device at the pulse voltage levels of 0, 60 and 120 V applied in a grounded gate configuration. It can be observed that as the device is stressed to 60 V level, a positive V_T shift, leading to a decrease in device current takes place. The sub-threshold current, however, presents no change. An absence of change in sub-threshold current implies no change in the properties of semiconductor–insulator interface and that the degradation in the device on-current could either be due to charge trapping in the SiN_x dielectric or due to generation of excessive traps near the drain contact.[28] As the stress level is further increased to 120 V, a negative V_T shift takes place
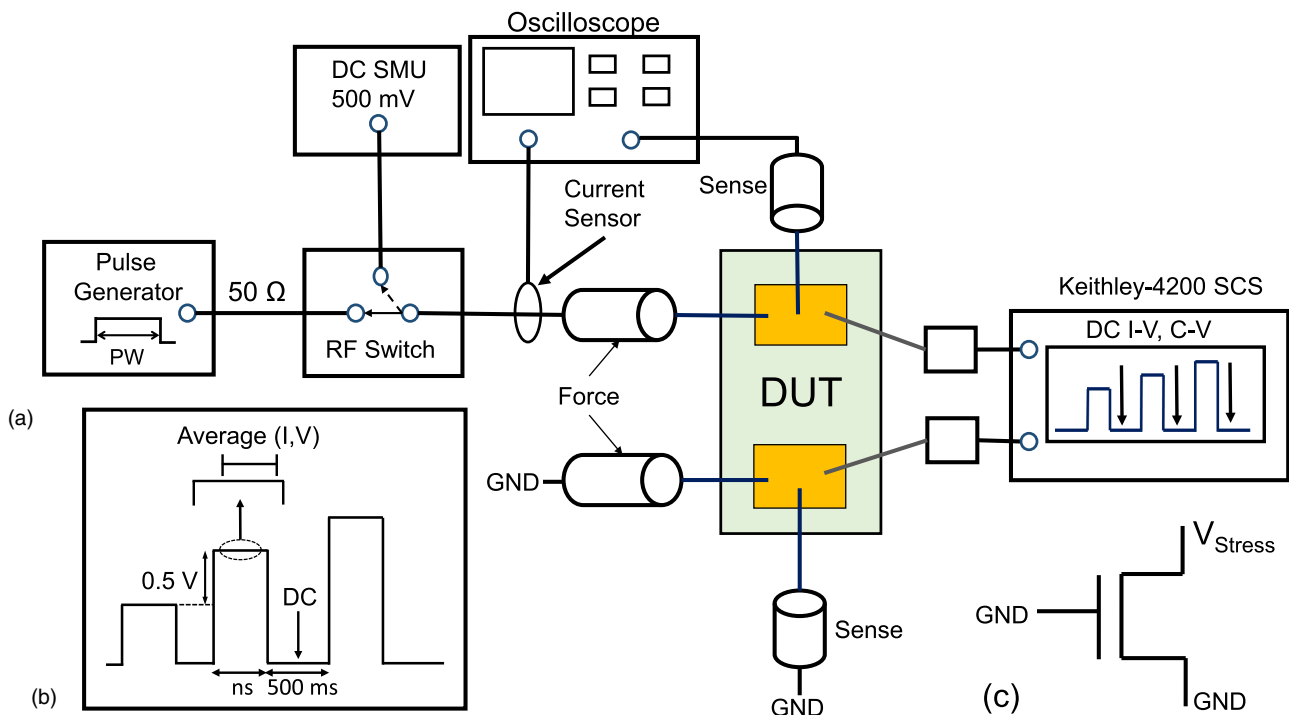

Fig. 2. (Color online) (a) Schematic view of the experimental setup used in the course of this work. Pulse characterization is done using a four probe pulse setup. A digital phosphor oscilloscope with a bandwidth of 4 GHz is used to capture voltage and current waveforms. Current sensor with a sensitivity of 0.5 mv mA^{-1} is used to measure device current. (b) Schematic view of the pulse voltage stress waveforms with the averaging window, used to extract quasi-static pulse characteristics. (c) Schematic description of the device under test. The voltage pulse stress is applied at the drain contact, while the source and gate are kept grounded.
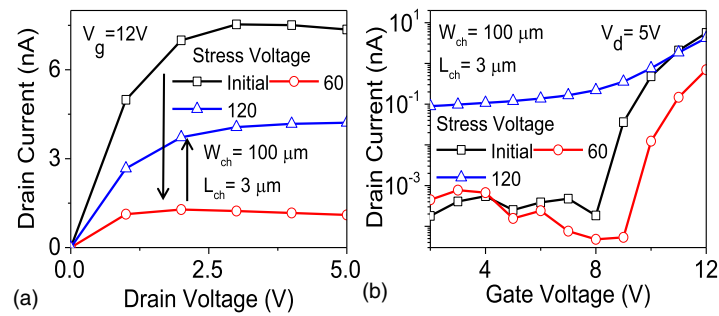
Fig. 3. (Color online) DC *I–V* characteristics of the device at various pulse voltage levels. The device experiences a partial recovery in the electrical characteristics as the applied pulse voltage is increased to 120 V.

and V_T recovers towards it's initial value. It can also be observed that although the device on-current increases after 120 V, there is also an increase in the sub-threshold current of the device, indicating a change in the properties of semiconductor–insulator interface. To further analyse the behavioral changes in the device at varying pulse stress levels, *C–V* measurements are done and the results are presented in Fig. 4. It is observed from Fig. 4 that there is a parallel shift in the *C–V* curve as the pulse stress increases to 60 V level, indicating that the dominant degradation mechanism at these stress levels is charge trapping in the dielectric. A positive shift indicates that the electron trapping takes place in the dielectric. Even in the sub-threshold condition, electrons are present in the a-Si:H bulk and an electron density of 5×10^{11} cm^{-2} has been reported at grounded gate condition.[29–31] As the stress pulses are applied to the drain contact, a field is established across the semiconductor layer and the electrons gain enough energy to cross the a-Si:H-SiN$_x$ barrier and are trapped in the dielectric layer. This phenomena also explains the observations made through DC *I–V* characterization. Further investigations of the *C–V* characteristics in Fig. 4 reveals that, as the pulse stress levels are increased to 120 V, a stretched-out behavior due to the fact that defect states are created at the semiconductor–insulator interface takes place. This is attributed to the fact that as the voltage levels applied at the drain contact are increased, a depletion layer is formed in the channel and the Fermi level moves below the mid-gap level. Extra defects are then created in the upper half of the bandgap.[32] At high field conditions, optical phonon generation also takes place, leading to an increase in the channel temperature and thus defect density. The relation between the channel temperature and defect generation can be explained through the concept of "thermalization energy", given by the expression

$$E_{th} = kT \ln(vt),$$

where *v* is the attempt-to-escape frequency.[33] The generated defect states envelope the impact of electron trapping in the gate dielectric. It is also interesting to note that this V_T recovery behavior is different from what has been reported for high negative gate bias induced instabilities, where the V_T recovery in the device takes place on the account of hole trapping in the dielectric layer.[34] To further explore the instability behavior, *C–V* and *C–V* hysteresis measurements are performed at a frequency 10 and 100 kHz at different stress levels and the results are presented in Fig. 5. The hysteresis measurements are performed by sweeping the device to accumulation and then sweeping it back. It is also worth noting that for the course of this work, hysteresis measurements are not performed for *I–V* measurements so as not to induce additional instabilities due to DC voltage stresses. It can be observed from Fig. 5(a) that at 120 V stress level, defect states are formed in the a-Si:H channel. The amount of hysteresis between the forward and reverse sweeps can be used to compare nature of the defect states. It can be observed that there is a reduction in the capacitance in the reverse sweep in Figs. 5(b) and 5(d), both of which correspond to *C–V* results of unstressed devices. This can be explained by the presence of acceptor defect states in the as-fabricated a-Si:H channel. As the stress level is further increased to 120 V, it is also observed from Figs. 5(c) and 5(e), that there is a reduction in the amount of hysteresis between the capacitance in forward and reverse sweeps. This observation along with an observed increase in defect states in the bandgap can be explained if the generated defects are donor defects. On performing the reverse sweep, the Fermi-level in the semiconductor channel moves towards mid-gap. However, there will be electrons trapped in the acceptor defects. The hysteresis due to these trapped electrons will be
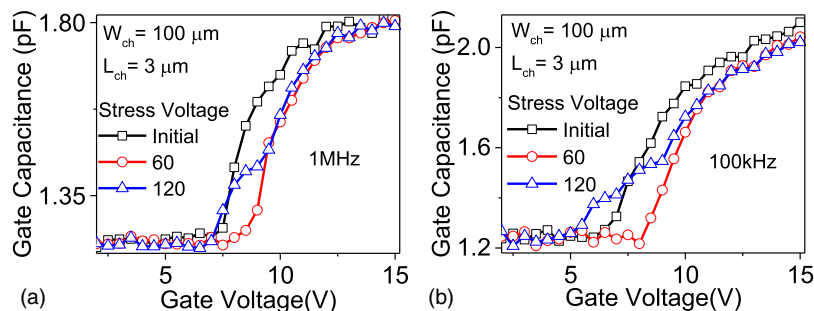

Fig. 4. (Color online) *C–V* characteristics of the device at different pulse voltage levels depicting the dominant instability mechanism in a-Si:H TFTs at (a) 1 MHz and (b) 100 kHz.
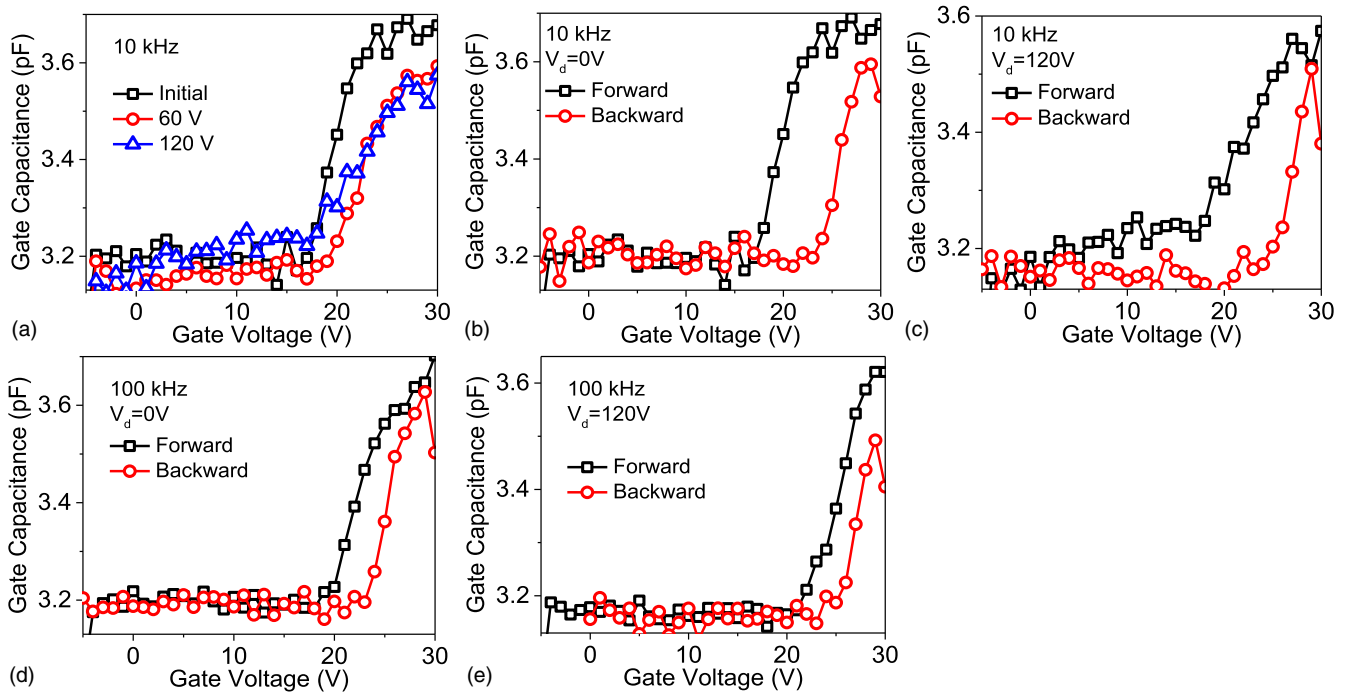
Fig. 5. (Color online) (a) *C–V* characteristics of the device at different pulse voltage levels. (b), (c) *C–V* hysteresis results at initial and 120 V stress level at 10 kHz frequency. (d), (e) *C–V* hysteresis results at initial and 120 V stress level at 100 kHz frequency. *C–V* hysteresis measurements are performed by sweeping the gate bias forward from −5 to 30 V and then reversing the sweep from 30 to −5 V.

counter-acted by empty donor states and thus leading to reduced hysteresis when compared to initial conditions. The generation of donor defects has been shown to take place in other investigations as well.[26] To investigate the material changes in the devices upon application of pulse voltage stress, Raman spectroscopy is done to measure any changes in the material properties (shown in supplementary material). It is observed that there is no shift in Raman peak and in full-width at half maximum on application of pulse voltage, establishing the fact that there are no changes in the material properties taking place in the a-Si:H layer with application of increased voltage levels.

To explore the spatial variation in the instability behavior across the a-Si:H channel, gate–source capacitance (C_{gs}) and gate–drain capacitance (C_{gd}) are measured post application of pulse stress at DUT. The corresponding curves are shown in Fig. 6. It can be observed that C_{gs} shows a monotonous parallel shift in *C–V* curve at both lower and higher stress levels indicating that the dominant degradation mechanism at the source side of the channel is the trapping of electrons in the dielectric. Contrary to C_{gs}, C_{gd} shows a non-monotonous shift in *C–V* curve with parallel shift taking place at lower

pulse stress level and a stretched-out behavior at higher stress levels (120 V). This also indicates that as the stress levels initially increases, electron trapping in the dielectric is the dominant mechanism across the entire channel. As the applied stress level is further increased, defect states are created near the drain contact. The observed defect accumulation near the drain contact is expected since the field across channel is maximum in the drain–gate overlap region. This also leads to an accumulation of optical phonons near the drain contact leading to formation of a localized hotspot, which further aids defect formation.

To further study the instability mechanism, stress pulses with higher pulse widths are applied across the device. Figure 7 shows the DC *I–V* and *C–V* characteristics of the device stressed through 1000 ns wide voltage pulses. It is observed that as the nanosecond pulse stress is initially applied, threshold voltage increases. Further application of voltage stress leads to a higher degree of V_T recovery as compared to 100 ns stress condition. It is also worth noting that the channel length of the device studied under 100 ns case is 3 μm while that of 1000 ns case is 20 μm. This is attributed either to the fact that in the case of 1000 ns pulse,
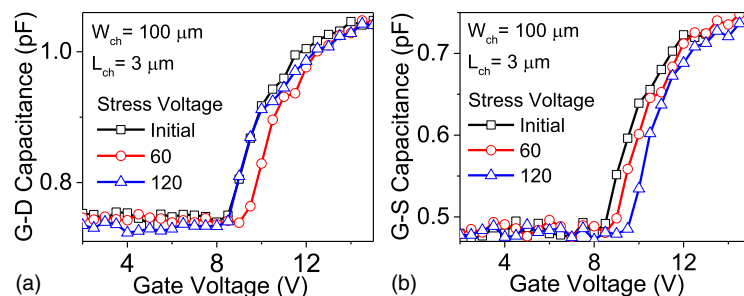

Fig. 6. (Color online) *C–V* characteristics of (a) gate–drain and (b) gate–source capacitance at 1 MHz. These measurements are performed by keeping the third contact [source in (a) and drain (b)] floating while the capacitance is measured across the probed contacts.
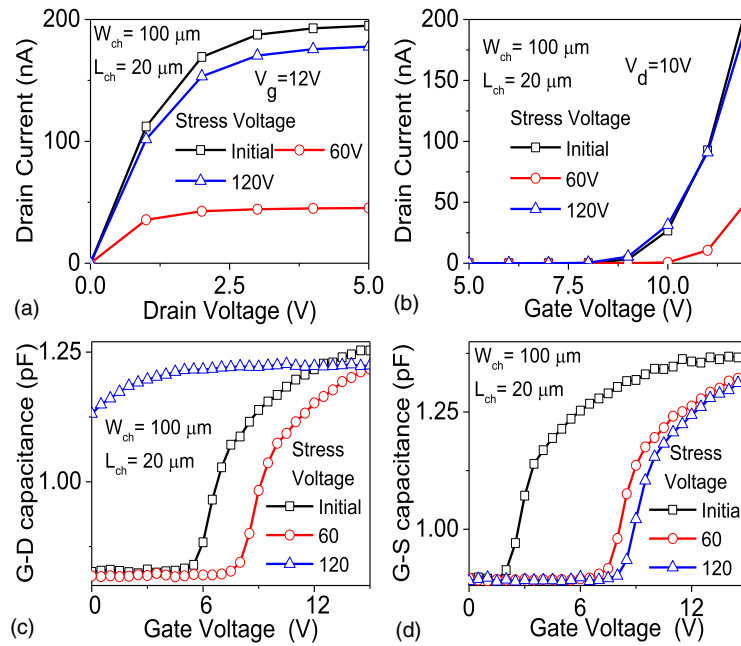
Fig. 7. (Color online) (a)–(b) DC *I–V* characteristics (c)–(d) *C–V* characteristics of a-Si:H TFTs stressed under nanosecond pulse voltage using a 1000 ns wide pulse. Higher stress width leads to self-heating induced defect states generation.

higher self-heating takes place (compared to 100 ns case), which leads to creation of higher number of defect states in the a-Si:H[35] or due to an increase in the channel conductance post stressing. It can also be observed from *C–V* characteristics that the creation of defect states still takes place in the drain side of the channel and that the dominant degradation phenomenon on the source side of the channel is charge trapping in the dielectric.

Further investigations on the instability behavior of a-Si:H TFTs is done by annealing the devices once a pre-determined stress level is reached (Fig. 8). To explore the impact of annealing, the devices are stressed and the degradation in the device performance is measured using DC *I–V*, *C–V* measurements. The devices are then thermally annealed at 423 K for a period of 1200 s under ambient conditions and the device electrical characteristics are measured again. This is followed by stressing the device further to a higher stress level and the same cycle is repeated. It can be observed that annealing leads to recovery of the threshold voltage in the case of both high and low stress induced instabilities. It was discussed earlier that in the case of low stress levels, electron trapping into the dielectric is the dominant instability mechanism and when the device is annealed, thermal energy
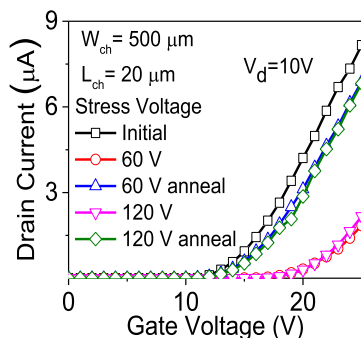
is transferred to the charge carriers, which enables them to cross the energy barrier of the traps. This de-trapping of the charge carriers leads to observed recovery of the threshold voltage of the a-Si:H TFT. Further increasing the stress levels, defect states are created in the a-Si:H channel. Annealing the device at this stage leads to recovery owing to removal of defects states.[36]

To understand the role of gate bias anneal in recovering the electrical characteristics of the device at various stress levels, thermal annealing in above sub-section is replaced by a gate bias anneal for a period of 1200 s. Figure 9 shows the transfer characteristics of the device with the application of gate bias of −10 V. It is observed that (i) at 60 V stress level, threshold voltage increase takes place (ii) at 120 V stress level, there is recovery in threshold voltage towards initial values and (iii) on application of a gate bias of −10 V for the case of both high and low voltage stress, threshold voltage shifts in the negative direction. While the other observations have already been discussed, the third observation could be explained either due to trapping of holes in the dielectric or due to creation of defect states in the a-Si:H channel due to the impact of vertical electric field. Exploration of gate bias effect is done through *C–V* measurements and the results are presented in Figs. 9(b)–9(c). It can be observed that the *C–V* curves obtained after the application of gate bias, present a parallel shift. This can be attributed to the fact that the threshold voltage recovery takes place due to hole trapping in the dielectric.

4. Conclusions

In this work, we have investigated the high frequency nano-second timescale field stress induced device degradation in a-Si:H TFTs in the condition when the stress is applied on the drain contact. Through real-time electrical and Raman characterization, it was found that as the stress levels are increased, electron trapping in the dielectric leads to the device degradation. With a further increase in the stress,
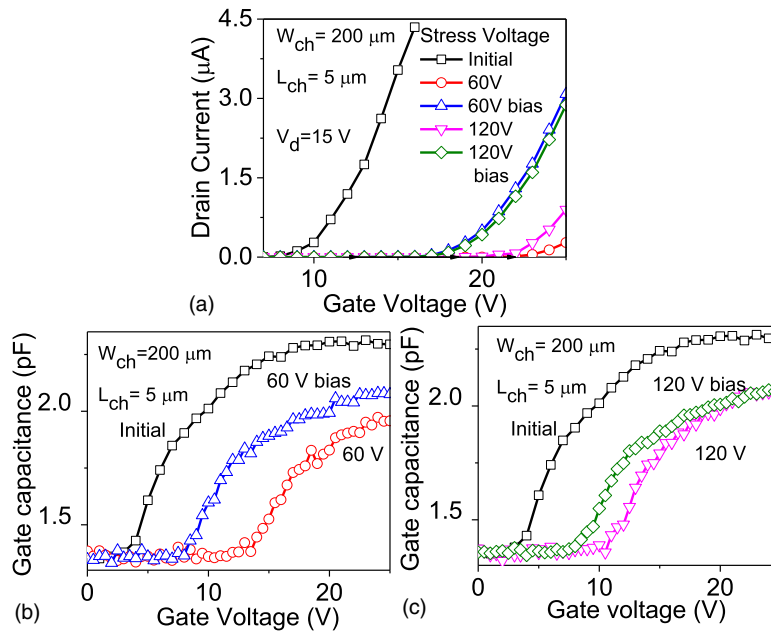

Fig. 8. (Color online) Transfer characteristics of the device annealed at different stress levels. Annealing the device leads to V_T recovery.

Fig. 9. (Color online) (a) Transfer characteristics of the device showing threshold voltage recovery on gate bais anneal. (b)–(c) C–V characteristics of the device at various stress levels.

positively charged defect states are formed at the semiconductor–insulator interface due to depletion of the channel and associated movement of the Fermi-level below the mid-gap level. It is also found that the defects are generated near the hot (drain) contact while electron trapping in the dielectric is dominant near the cold (source) contact. As a result, a positive V_T shift followed by a negative V_T shift is observed with stress across the a-Si:H layer. Raman spectroscopy reveals no change in the material properties of the a-Si:H layer with stress. Increased self-heating, as a result of increased pulse width of the field stress pulse, leads to an accelerated degradation behavior by aiding the defect states generation at the interface. A recursive cycle of measurement, stressing and annealing was done and a V_T recovery is observed through thermal annealing of the device through de-trapping of electrons and defect removal. A similar negative gate bias anneal cycle also leads to V_T recovery through hole trapping in the dielectric.

ORCID iDs

Rajat Sinha https://orcid.org/0000-0003-0169-2857

1) R. Street, X. Wu, R. Weisfield, S. Ready, R. Apte, M. Ngyuen, W. Jackson, and P. Nylen, "Two-dimensional amorphous silicon image sensor arrays," J. Non-Cryst. Solids **198–200**, 1151 (1996).
2) R. Street, R. Apte, T. Granberg, P. Mei, S. Ready, K. Shah, and R. Weisfield, "High performance amorphous silicon image sensor arrays," J. Non-Cryst. Solids **227–230**, 1306 (1998).
3) R. L. Weisfield, "Amorphous silicon TFT X-ray image sensors," Int. Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217), 1998, p. 21.
4) D. E. Carlson and C. R. Wronski, "Amorphous silicon solar cell," Appl. Phys. Lett. **28**, 671 (1976).
5) C.-W. Chen, T.-C. Chang, P.-T. Liu, H.-Y. Lu, K.-C. Wang, C.-S. Huang, C.-C. Ling, and T.-Y. Tseng, "High-performance hydrogenated amorphous-Si TFT for amlcd and amoled applications," IEEE Electron Device Lett. **26**, 731 (2005).
6) H. Lebrun, F. Maurice, J. Magarino, and N. Szydlo, "Amlcd with integrated drivers made with amorphous-silicon tfts," J. Soc. Inf. Disp. **3**, 177 (1995).
7) N. Ibaraki, "A-Si TFT technologies for am-lcds," MRS Proc. **345**, 3 (1994).
8) H. Gleskova, S. Wagner, V. Gašparık, and P. Kováč, "150 c amorphous silicon thin-film transistor technology for polyimide substrates," J. Electrochem. Soc. **148**, G370 (2001).
9) Y. Chen, K. Denis, P. Kazlas, and P. Drzaic, "12.2: A conformable electronic ink display using a foil-based a-Si TFT array," SID Symp. Dig. Tech. Pap. **32**, 157 (2001).
10) J. Lee, Y. Lim, C. Park, Y. Park, C. Kim, and Y. Hwang, "A-Si:H thin-film transistor-driven flexible color e-paper display on flexible substrates," IEEE Electron Device Lett. **31**, 833 (2010).
11) M. H. Lee, K. Ho, P. Chen, C. Cheng, S. T. Chang, M. Tang, M. H. Liao, and Y. Yeh, "Promising a-Si:H TFTs with high mechanical reliability for flexible display," 2006 Int. Electron Devices Meeting, 2006, p. 1.
12) M. J. Powell, S. C. Deane, and W. I. Milne, "Bias-stress-induced creation and removal of dangling-bond states in amorphous silicon thin-film transistors," Appl. Phys. Lett. **60**, 207 (1992).
13) M. J. Powell, C. van Berkel, A. R. Franklin, S. C. Deane, and W. I. Milne, "Defect pool in amorphous-silicon thin-film transistors," Phys. Rev. B **45**, 4160 (1992).
14) W. B. Jackson and M. D. Moyer, "Creation of near-interface defects in hydrogenated amorphous silicon–silicon nitride heterojunctions: the role of hydrogen," Phys. Rev. B **36**, 6217 (1987).
15) M. J. Powell and S. C. Deane, "Improved defect-pool model for charged defects in amorphous silicon," Phys. Rev. B **48**, 10815 (1993).
16) S. Deane, W. Milne, and M. Powell, "Reduction of threshold voltage shift by bias annealing of hydrogenated amorphous silicon thin film transistors," MRS Online Proc. Library Archive, 1991 **Vol. 219**.
17) A. R. Hepburn, J. M. Marshall, C. Main, M. J. Powell, and C. van Berkel, "Metastable defects in amorphous-silicon thin-film transistors," Phys. Rev. Lett. **57**, 1192 (1986).
18) M. J. Powell, "Charge trapping instabilities in amorphous silicon–silicon nitride thin-film transistors," Appl. Phys. Lett. **43**, 597 (1983).
19) R. A. Street and C. C. Tsai, "Fast and slow states at the interface of amorphous silicon and silicon nitride," Appl. Phys. Lett. **48**, 1672 (1986).
20) M. J. Powell, C. van Berkel, I. D. French, and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," Appl. Phys. Lett. **51**, 1242 (1987).
21) F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," Appl. Phys. Lett. **62**, 1286 (1993).
22) S. Sambandan, D. Striakhilev, P. Servati, and A. Nathan, "Markov model for threshold-voltage shift in amorphous silicon TFTs for variable gate bias," IEEE Electron Device Lett. **26**, 375 (2005).
23) S. Sambandan and A. Nathan, "Equivalent circuit description of threshold voltage shift in a-Si:H TFTs from a probabilistic analysis of carrier population dynamics," IEEE Trans. Electron Devices **53**, 2306 (2006).

24) K. S. Karim, A. Nathan, M. Hack, and W. I. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs," IEEE Electron Device Lett. **25**, 188 (2004).

25) Z. Tang, M. Park, S. Jin, and C. Wie, "Drain bias dependent bias temperature stress instability in a-Si:H TFT," Solid-State Electron. **53**, 225 (2009).

26) N. T. Golo, S. van der Wal, F. G. Kuper, and T. Mouthaan, "Estimation of the impact of electrostatic discharge on density of states in hydrogenated amorphous silicon thin-film transistors," Appl. Phys. Lett. **80**, 3337 (2002).

27) C.-Y. Huang, T.-H. Teng, J.-W. Tsai, and H.-C. Cheng, "The instability mechanisms of hydrogenated amorphous silicon thin film transistors under AC bias stress," Jpn. J. Appl. Phys. **39**, 3867 (2000).

28) A. G. Lewis, I. Wu, M. Hack, A. Chiang, and R. H. Bruce, "Degradation of polysilicon TFTs during dynamic stress," Int. Electron Devices Meeting 1991 [Technical Digest], 1991, p. 575.

29) P. Servati and A. Nathan, "Modeling of the reverse characteristics of a-Si:H TFTs," IEEE Trans. Electron Devices **49**, 812 (2002).

30) R. A. Street and M. J. Thompson, "Electronic states at the hydrogenated amorphous silicon/silcon nitride interface," Appl. Phys. Lett. **45**, 769 (1984).

31) R. A. Street, M. J. Thompson, and N. M. Johnson, "The electrical characterization of surfaces, interfaces and contacts to a-Si:H," Philos. Mag. B **51**, 1 (1985).

32) J. G. Shaw, M. G. Hack, and R. A. Martin, "Metastable effects in high-voltage amorphous silicon thin-film transistors," J. Appl. Phys. **69**, 2667 (1991).

33) S. C. Deane, R. B. Wehrspohn, and M. J. Powell, "Unification of the time and temperature dependence of dangling-bond-defect creation and removal in amorphous-silicon thin-film transistors," Phys. Rev. B **58**, 12625 (1998).

34) Y. Tai, J. Tsai, H. Cheng, and F. Su, "Anomalous bias-stress-induced unstable phenomena of hydrogenated amorphous silicon thin-film transistors," Appl. Phys. Lett. **67**, 2503 (1995).

35) S. Kao, H. Zan, J. Huang, and B. Kung, "Self-heating effect on bias-stressed reliability for low-temperature a-Si:H TFT on flexible substrate," IEEE Trans. Electron Devices **57**, 588 (2010).

36) J. Y. Lee, C. Lee, J. Jang, and B. S. Bae, "Annealing behavior of metastable defects created by bias stress in hydrogenated amorphous silicon thin film transistors," Solid State Commun. **83**, 833 (1992).