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Electrothermal transport induced material reconfiguration and performance degradation of CVD-grown monolayer MoS₂ transistors

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Device and material reliability of 2-dimensional materials, especially CVD-grown MoS₂, has remained un-addressed since 2011 when the first TMDC transistor was reported. For its potential application in next generation electronics, it is imperative to update our understanding of mechanisms through which MoS₂ transistors' performance degrades under long-term electrical stress. We report, for CVD-grown monolayer MoS₂, results on temporal degradation of material and device performance under electrical stress. Both low and high field regimes of operation are explored at different temperatures, gate bias and stress cycles. During low field operation, current is found to saturate after hundreds of seconds of operation with the current decay time constant being a function of temperature and stress cycle. High field operation, especially at low temperature, leads to impact ionization assisted material and device degradation. It is found that high field operation at low temperature results in amorphization of the channel and is verified by device and kelvin probe force microscopy (KPFM) analyses. In general, a prolonged room temperature operation of CVD-grown MoS₂ transistors lead to degraded gate control, higher OFF state current and negative shift in threshold voltage (V_T). This is further verified, through micro-Raman and photoluminescence spectroscopy, which suggest that a steady state DC electrical stress leads to the formation of localized low resistance regions in the channel and a subsequent loss of transistor characteristics. Our findings unveil unique mechanism by which CVD MoS₂ undergoes material degradation under electrical stress and subsequent breakdown of transistor behavior. Such an understanding of material and device reliability helps in determining the safe operating regime from device as well as circuit perspective.

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INTRODUCTION

2-dimensional (2D) transition metal dichalcogenides (TMDCs), owing to their layered structure, offer much better immunity against scaling related challenges posed by Moore's law for transistors¹. Besides, heavy electron effective mass in TMDCs strongly advocates their role as channel material for ultra-scaled field-effect transistors (FETs)² i.e. beyond 3 nm technology nodes. Looking at such promise as future device material, extensive research on FETs on various TMDCs has been conducted for more than a decade now. Several groups have reported few to single layer Molybdenum Disulfide (MoS₂) and other TMDC FETs^{3–6}. Preliminary reports suggested remarkable ON/OFF current ratio⁷, low sub-threshold slope (SS)⁸ and large current density⁵ - metrics important for acceptable transistor behavior for switching applications. However, large contact resistance (R_C) due to lack of covalent bonds⁹ at the metal-MoS₂ interface has strongly questioned the ultimate deployment of MoS₂, and TMDCs in general, in the semiconductor industry. Several approaches like degenerate doping via surface charge transfer^{10–13}, dopant introduction (substitutional doping) during material growth¹⁴, adding Chalcogen impurities at the contact¹⁵ and selective phase transition¹⁶ have been performed to get away with the R_C bottleneck. Besides, TMDC heterostructures are being investigated for optoelectronic^{17–19} and tunnel FET²⁰ applications. TMDC based memristors for neuromorphic applications^{21–23} is another prospect that has evolved lately. Such technology driven reports are extensively available, however, very few reports discuss another crucial aspect - reliability. Apart from environment induced

degradation of TMDCs^{24,25}, very few reports elucidate the mechanism of electrical stress induced 2D material and device degradation.

Dattatray et. al. have reported the effect of oxygen and moisture on the transistor behavior especially in the hysteretic behavior²⁴. In a separate effort, Bartolomeo et al. have reported oxygen and moisture induced instabilities in the threshold voltage (V_T) of MoS₂ transistors upon multiple electrical measurements²⁵. Besides environmental factors, material specific factors like intrinsic defects also affect material and device properties. Liu et al. and Kripalani et. al. have reported important insights on the role of specific kind of defects on material stability²⁶ and other properties like thermal conductivity²⁷ etc. Unlike other reports on material-device degradation, Dominik et al. reported the very first study on electrical breakdown of MoS₂ transistors with current densities 50 times higher than that of copper²⁸. Avalanche breakdown in exfoliated MoS₂ has been demonstrated and studied by Jinsu et al.²⁹ where critical field for avalanche multiplication in MoS₂ is calculated as a function of thickness of MoS₂ and temperature. Mishra et al. reported electrical stress dependent material and device co-degradation study of graphene transistors^{30,31}. They elucidated the failure mechanism which graphene transistors undergo in the presence of electrical stress and ambient oxygen. Stress induced temperature sets up favorable conditions for oxygen to react with graphene which proceeds in several steps until complete device failure is observed. Similar reports on electrical stress induced material and device performance degradation of TMDC FETs are unfortunately missing.

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Fundamental properties like electrical and thermal conductivity play dominant role in determining the current carrying capacity and breakdown field for a material. These properties for MoS₂ are different from other semiconductors like silicon and graphene, essentially, because of difference in their molecular arrangements. Naturally, response of MoS₂ to electric field and high current densities must be different from that of other materials. Similarly, the mechanism through which degradation occurs in TMDC devices under electrical stress, in principle, must be different from those observed in graphene or other semiconductors. In order to fabricate robust 2D TMDC transistors and mitigate reliability issues in these devices, to develop understanding of material and device degradation mechanisms is essential. Moreover, dynamic evolution of channel degradation and its impact on channel current can hinder critical electric field for acceptable device operation, especially in ultra-scaled transistors. As a result, reconsidering trends in voltage scaling for these materials may become imperative. Therefore, to understand the dynamics of material and device degradation in MoS₂ and subsequent failure of MoS₂ FETs, we start with observing steady state electrical behavior of chemical vapor deposited (CVD)-grown monolayer MoS₂ FETs and explain electro-thermal transport using the theory of electron-phonon scattering. Both high and low field transport are found to induce perturbations in the transistor behavior which is identified after every stress cycle. Taking inference from device characteristics and using detailed analyses of the micro-Raman & photoluminescence (PL) spectra, we eventually show that MoS₂ FETs undergo a unique failure mechanism wherein localized high conductance regions are formed within the MoS₂ channel. This phenomenon shows up as a result of field-induced material re-

configuration. Subsequently, complete device failure is observed due to field induced amorphization of the channel.

RESULTS AND DISCUSSION

Characterization setup

Field-effect transistors are fabricated on CVD monolayer MoS₂ for the back-gated configuration shown in Fig. 1a. A scanning electron microscopic (SEM) top-view of the as-fabricated monolayer MoS₂FET is shown in Fig. 1b. Uniform monolayer MoS₂ film is verified through Raman spectra, Fig. 1c.

In order to understand the effect of long-term electric field on device behavior, devices are stressed under different source-to-drain electric fields (E_{SD}) for hundreds of seconds under varying conditions like gate voltage (V_{GS}) and temperature (T). Current fluctuations during the stress period and low voltage device characteristics, before and after the stress cycle, are captured to identify the impact of specific stress conditions on transistor behavior. Preliminary output characteristics of a 1 μm long and 10 μm wide monolayer MoS₂ transistor, Fig. 2a, show decent transistor performance with the onset of current saturation at $E_{SD} > 0.09$ MV/cm and suggest two regimes of operation that may have more physical relevance: $E_{SD} \leq 0.1$ MV/cm as low-field and $E_{SD} \geq 0.2$ MV/cm as high-field. This is chosen as a result of current/velocity saturation and onset of breakdown observed in Fig. 2b. Hence, subsequent virgin devices (VD) are stressed under these two regimes of operation at different V_{GS} and T values for control over electron and phonon population in the monolayer MoS₂ channel respectively. It is important to note that all measurements are performed in vacuum (10^{-4} torr).

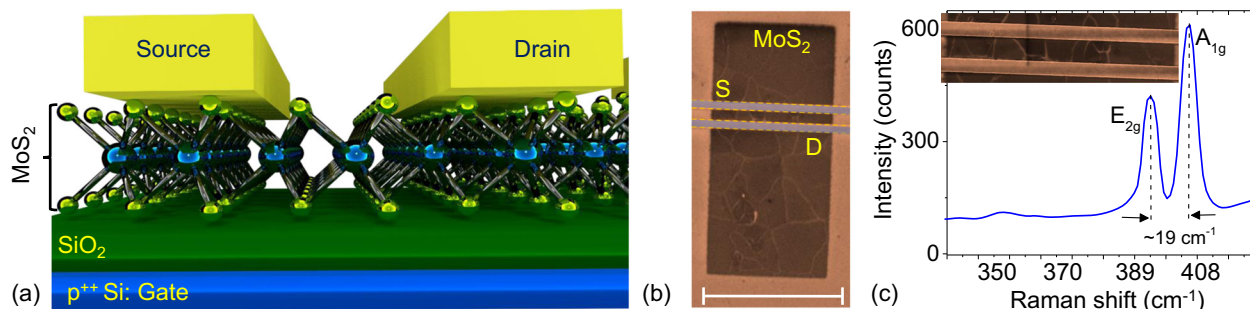


Fig. 1 Device fabrication and preliminary characterization. **a** Back-gated transistor configuration for CVD monolayer MoS₂ FETs used in this work for all the investigations. **b** SEM (scale bar: 10 μm) top-view of a fabricated back-gated FETs with following device dimensions: $L_{CH} = 1$ μm , $W = 10$ μm , $T_{ox} = 90$ nm. **c** Raman spectra of the CVD MoS₂ film transferred on SiO₂ showing characteristic in-plane (E_{2g}) and out-of-plane (A_{1g}) vibrational modes with the difference between phonon wavenumbers (~ 19 cm^{-1}) implying a monolayer. Inset: magnified SEM image of device channel.

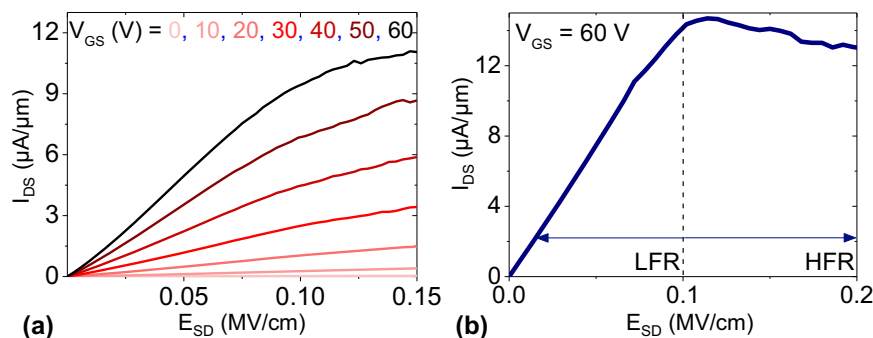


Fig. 2 Identifying low (LFR) and high (HFR) field regimes of operation. **a** Output characteristics of MoS₂ transistor exhibiting onset of current saturation at $E_{SD} = 0.09$ MV/cm. **b** Two different regimes of operation are identified on basis of current (velocity) saturation, observed in these devices. The transistor starts to settle in saturation at $E_{SD} = 0.1$ MV/cm and stays deep in saturation until $E_{SD} = 0.2$ MV/cm after which breakdown occurs. For the study intended in this work, none of the devices are stressed beyond 0.2 MV/cm so that the device operates like a transistor within the safe operating regime and effect of long-term electrical stress can be captured.

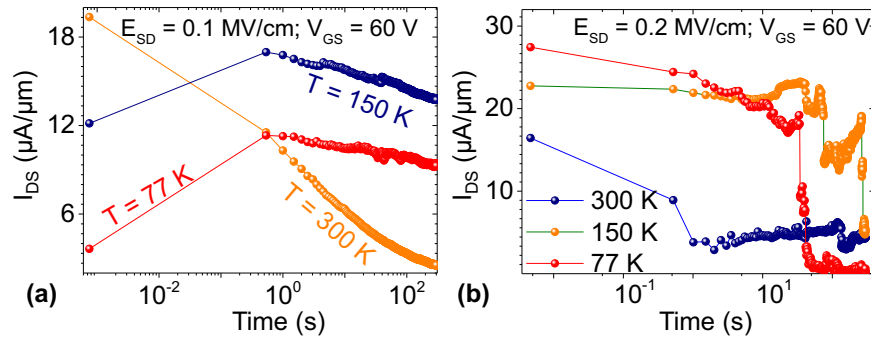


Fig. 3 Current dynamics under LFR and HFR operation. Temporal variation of current through MoS₂ channel under **a** LFR operation and **b** HFR operation at different temperatures. V_{GS} is constant, maintained at 60 V during the stress period.

Steady-state electro-thermal transport

As mentioned earlier, MoS₂ devices are stressed under low and high field regime: $E_{SD} = 0.1 \text{ MV/cm}$ (LFR) and 0.2 MV/cm (HFR) for several seconds and stress cycles. During the stress cycles, contribution from other parameters is studied by varying V_{GS} and T values. At $V_{GS} = 60 \text{ V}$ (ON state), when stressed in LFR, a monotonic decrease in the channel current is observed which eventually starts to saturate after $\sim 300 \text{ s}$ as shown in Fig. 3a. Similar variation in current at lower temperatures (150 K and 77 K) is observed however, with a small rate of decay in current. HFR operation at room temperature (300 K) results in an initial fall in current followed by sustained current through the channel, Fig. 3b. It is clear from Fig. 3 that HFR operation results in abrupt variations in current unlike that in LFR. During low temperature HFR operation, marginal decay in current is observed for the first $\sim 100 \text{ s}$ after which abrupt device failure occurs resulting in extremely low current, in the range of pico-ampere, through the device. It is interesting to note that, low temperature operation in HFR introduces permanent damage to the device channel. This is also validated by the device characteristics captured after the stress cycles, as discussed in subsequent sections.

Monotonically decreasing current and abrupt fall in current are observed for LF stress and HF stress during successive stress cycles. Interestingly, the thermal equilibrium point at the end of every stress cycle shifts upwards after every stress cycle at room temperature, see Supplementary Note 1 and Supplementary Fig. 1. In contrast, such a shift in the saturation point is not observed when devices are stressed at lower temperatures, see Supplementary Fig. 2. The authors have reported similar variation in current characteristics, Figs 2, 3, in a previous work³².

Device operation in LFR at different temperatures can be explained using phonon and impurity scattering theory of electrons at high and low temperature respectively in the diffusive channel. The temperature dependent average phonon population ($\langle n \rangle$) at an energy $E (= \hbar\omega)$ can be predicted using the famous Bose-Einstein distribution or Planck's distribution, i.e.

$$\langle n \rangle = \frac{1}{\exp\left(\frac{\hbar\omega}{kT}\right) - 1} \quad (1)$$

where \hbar = Planck's constant; k = Boltzmann constant; T = Temperature and ω = Phonon frequency are fundamental constants³³.

At any temperature, the low frequency phonon population (acoustic phonons) is much larger than the high frequency phonon population (optical phonons). Moreover, phonon population exponentially increases with temperature irrespective of phonon frequency. Therefore, events like electron phonon scattering, that involve optical phonons, have marginal probability of occurrence, especially at lower temperatures, when compared with the probability of occurrence of events like heat dissipation which essentially involves acoustic phonons. Moreover, impurity/coulomb scattering dominates at lower T whereas phonon

scattering dominates at higher T ^{33,34}. Keeping the above discussion in perspective, monotonic decay in current during room temperature LFR stress, as observed in Fig. 3a, is a result of electron-phonon scattering wherein an electron loses energy to the lattice and generates more phonons which manifests as heating of the channel and further scatter electrons. This continues until a thermal equilibrium is reached at $\sim 100 \text{ s}$ when the rate of energy lost by electron is balanced by the rate at which acoustic phonons dissipate the generated heat thereby keeping the optical phonon population constant, i.e. rate of optical phonons generated by electron-phonon scattering = rate of scattering of optical phonon into multiple acoustic phonons. Significantly small population of optical phonons and still large population of acoustic phonons at lower T and finite number of coulomb scattering sites by impurities in the channel result in a much smaller decay time constant and hence thermal equilibrium is reached much faster at lower T as shown in Fig. 3a. However, initial increase in the current, Fig. 3a, at lower T is attributed to acoustic phonon assisted propagation of heat dissipated by limited yet 'non-zero' number of electron-phonon scattering towards the contacts resulting in improved thermionic emission of carriers across the barrier as discussed by Mishra et. al. for CNT devices³⁵.

Similarly, HFR operation at room temperature results in an initial abrupt decay of current. This is attributed to remarkable increase in the probability of electron-phonon scattering events due to high energy electrons and abundance of optical phonons at 300 K. After the initial decay in current, significant loss in the kinetic energy of electrons along with heat dissipation via acoustic phonons establish thermal equilibrium between electrons and the lattice. However, HFR operation at lower T leads to longer diffusion length because of (i) weak (but non-zero) electron-phonon scattering at low T and (ii) weak impurity scattering of high energy electrons³³. As a result, electrons travel through the channel without losing much energy until they initiate impact ionization as shown in Fig. 3b. Increase in current followed by an immediate abrupt fall is a characteristic of impact ionization process. High energy (hot) electrons bombard the lattice and generate electron-hole pairs which are then captured by the high electric field. This manifests as increased current following physical damage of the lattice due to disruption of bonds by hot electrons observed as abrupt fall in current as shown in Fig. 3b³⁴.

So far, based on crude understanding of electron-phonon scattering processes, the observed current variation with time has been broadly attributed to generation of optical phonons in the channel as the device continues to operate for a prolonged period. In order to validate the anticipated cause of time dependence of current and observed electro-thermal transport mechanism in our devices, we extract field-effect mobility as a function of temperature at different time instances of device

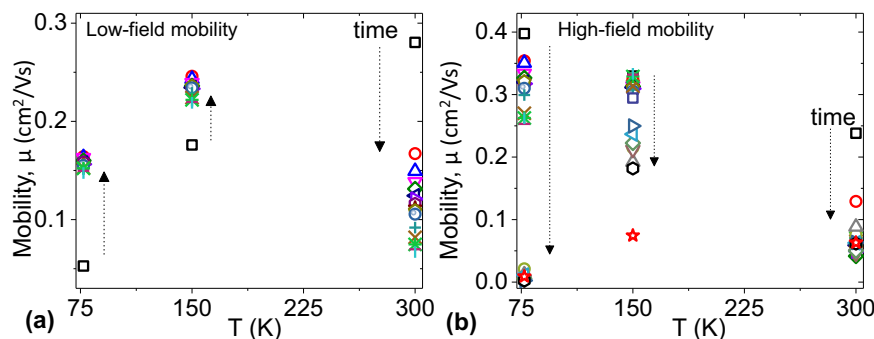


Fig. 4 Time-dependent mobility versus temperature to identify various scattering mechanisms. **a** Temperature dependence of field-effect mobility at various time instances during electrical stress under **a** low-field and **b** high-field operation. Black arrows imply increasing time.

operation. Temperature dependence of mobility at different time instances of LFR and HFR is shown in Fig. 4.

As shown in Fig. 4a, at $t = 500$ ms, mobility increases as a function of temperature. Such behavior is typically attributed to impurity scattering which dominates as the temperature decreases and vice versa. In MoS_2 , phonon scattering dominates only at temperatures above room temperature unlike silicon. This is attributed to a significant bandgap in the phonon bandstructure of MoS_2 and high optical phonon energies. As a result, ionized impurity scattering dominates the overall mobility of electrons in the given temperature range – 77 K to 300 K, as shown in Fig. 4a. At higher temperature, lattice vibrations or phonons significantly increase in number and scatter electrons thereby degrading the mobility. Owing to the energy range and occupancy of phonon states, high energy phonons (optical phonons) tend to scatter electrons more than low energy phonons (acoustic phonons). In MoS_2 , optical phonon scattering is expected to dominate at temperatures above room temperature and thereby degrade electron mobility. This is not seen in our devices mainly because of the temperature range within which the devices are operated. A prolonged operation of the transistor in the low-field regime is found to degrade the high temperature mobility and increase mobility at lower temperature as shown in Fig. 4a for $t > 500$ ms to $t = 300$ s. It is observed that for successive instances of time, high temperature mobility decreases significantly and eventually saturates. The observed mobility saturation primarily occurs because the rate of degradation is not constant and rather decreases with time. While high temperature mobility monotonically degrades during device operation, low temperature mobility increases and saturates after $t = 1000$ ms. This is attributed to initial current annealing in the device which tends to eliminate most of the process induced impurities, i.e., organic residue and other adsorbed species like moisture, which are potential coulomb scattering sites and degrade low temperature carrier mobility. Inference made from the time dependence mobility versus temperature data is in agreement with the physics expected to cause time dependent variation in current, discussed earlier. We further validate the proposed introduction of optical phonons and reduction in impurity scattering sites with time by using various theoretical models³⁶ representing the physics of different scattering mechanisms like ionized impurity scattering, acoustic phonon scattering and optical phonon scattering that degrade mobility in MoS_2 . A detailed discussion on how time dependence, when included in the already existing models, yields similar trend in the time dependence of mobility versus temperature curve as that identified from the experimental data, is provided in Supplementary note 2 (see Supplementary Fig. 3).

High-field mobility is also shown as a function of temperature and time in Fig. 4b. Unlike low temperature mobility at low field, it is observed that high field mobility at low temperature decreases with temperature. Such a behavior suggests that II scattering

mechanism, which is typically dominant at lower temperatures, becomes dormant during high field transport. This is attributed to higher energy of electrons due to which they successfully escape the coulombic field of impurity sites present in the channel³³. A typical high-field phenomenon – impact ionization is believed to be present in MoS_2 as discussed earlier. In order to validate the occurrence of impact ionization, rate of increase in current at critical instances is extracted from Fig. 3b. It is known that impact ionization rate (α_{ij}) is proportional to the rate of increase in the current during hot-electron induced ionization and decreases as a function of temperature³⁷. This variation of α_{ij} with temperature is attributed to the fact that at higher temperature enough phonon scattering mechanisms decrease the energy of electron thereby making it difficult for it to achieve enough energy and knock-off additional electrons, and generate electron-hole pairs, from the lattice and trigger impact ionization³⁷. It is observed that the rate of increase in current decreases with temperature and thereby validates the occurrence of impact ionization in our devices, discussed in Supplementary note 3. Temperature dependence of rate of increase in current at critical time instances is extracted from Fig. 3b and shown in Supplementary Fig. 4.

As discussed earlier, HFR transport in the ON state of MoS_2 FET results in a complete failure of the device after ~ 300 s of operation at lower temperatures. Partial breakdown of the device is observed at 300 K after an abrupt fall in current within few milliseconds of operation, Fig. 3b. Further, electron-phonon scattering rate is a function of both electron as well as phonon population³³ which are, in principle, controlled by gate bias (V_{GS}) and temperature (T) respectively. Moreover, onset of device failure because of damage to the lattice due to impact ionization is determined by two quantities: high energy electron population determined by V_{GS} , and electron energy determined by E_{SD} . In order to observe the effect of electron population on the HF transport, devices are kept in HFR of operation at different gate voltages and current fluctuation is captured as a function of time, Fig. 5.

At $V_{GS} = 60$ V, as shown in Fig. 5, the FET is in ON state and an initial decay followed by a constant current is observed for reasons discussed earlier. However, when the carrier concentration in the channel is tuned low (via V_{GS}), current reduces by ~ 2 orders of magnitude, electron-phonon scattering is significantly suppressed³³. This is reflected in the marginal variation in current at $V_{GS} = 0$ V in Fig. 5. Interestingly, on further reduction of carrier concentration at $V_{GS} = -60$ V, after ~ 100 s of stress, current rises abruptly by 3 orders of magnitude, Fig. 5. This is a unique behavior that cannot be explained using the electron-phonon scattering model at room temperature, discussed earlier. However, such a rise in current in the OFF state is possible if (i) electrons in the channel gain sufficient energy via current induced self-heating of the channel and transit from low to higher energy sub-bands in the bandstructure or (ii) significant increase in the density of states

within the bandgap which facilitate current conduction through the channel in the OFF and sub-threshold region via variable range hopping at room temperature³⁸ or (iii) both. Among these two possible reasons, the latter must introduce permanent change in the material, unlike former, which can be identified in successive stress cycles and/or transistor behavior. Moreover, current in the range of pico-ampere is not sufficient to introduce self-heating and hence transfer sufficient energy to electrons for inter-band transition. Therefore, the possibilities of the first reason for observed rise in current are minimal and a field-assisted permanent change in the material seems to be a more plausible reason. Nevertheless, to understand this behavior, impact of steady-state electrical stress on transistor behavior is studied next. Intuitively, it reveals more about the electro-thermal stress induced perturbation in MoS₂ and its manifestation in transistor behavior after different stress conditions, which is discussed in the next section.

It is worth highlighting that the devices under test, due to its polycrystalline/CVD nature, exhibit significantly lesser drive current compared to the same reported on highly crystalline material³⁹. It is however important to note that a reasonable transistor action with very high ON-OFF ratio was observed in all

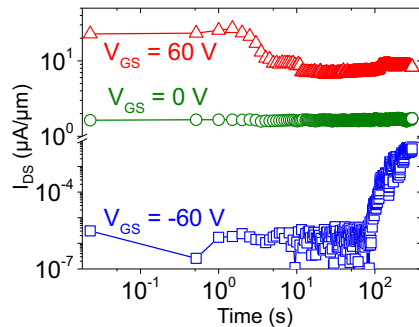


Fig. 5 Impact of gate voltage. Effect of room temperature steady-state electrical stress (in HFR i.e., $E_{SD} = 0.2$ MV/cm) on MoS₂ FETs at different V_{GS} .

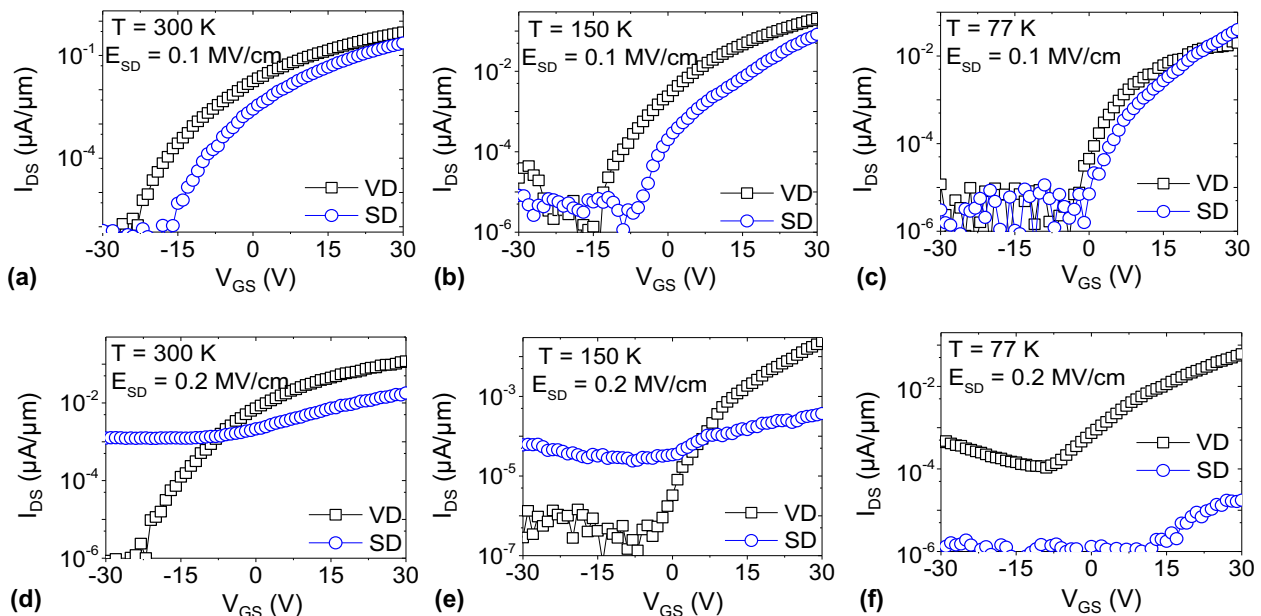


Fig. 6 Impact on transistor behavior. Transfer characteristics of unstressed/virgin (VD) and stressed (SD) FETs stressed in **a–c** LFR and **d–f** HFR of operation at different temperatures. Degraded OFF state performance, loss of gate control and reduced ON state current are the major implications of HF stress. All devices are measured at $V_{DS} = 1$ V.

the devices¹⁵ and hence all gate-dependent mechanisms are believed to persist in all MoS₂ FETs, irrespective of the material quality. Higher drive current, in a high performing device, in fact may result in enhanced self-heating and thereby increase the channel temperature. This may lead to a smaller current decay time constant. This is attributed to requirement of critical channel temperature, as discussed above, to trigger stress induced material reconfiguration. However, in general, the trends presented above would still remain the same for a better performing device.

Impact on transistor behavior

Low voltage transfer characteristics ($V_{DS} = 1$ V) of MoS₂ FETs are captured for virgin (VD) and stressed devices (SD). Both HFR and LFR of operation are investigated and it is found that long-term electrical stress (both LFR and HFR) induces remarkable deviation from the original device behavior (i.e. VD), Fig. 6. Note that following are the stress conditions: $E_{SD} = 0.2$ MV/cm (HFR) or 0.1 MV/cm (LFR) and $V_{GS} = 60$ V unless specified.

After LF stress, devices exhibit higher threshold voltage (V_T) irrespective of temperature as shown in Fig. 5a–c. For higher temperatures ($T = 300$ K and 150 K), the ON state current degrades after stress. On the other hand, at $T = 77$ K, ON state current is found to have increased marginally (by a factor of 2) as a result of LF stress. Increase in V_T is not trivial to contemplate and needs further investigations, however, decrease in ON state current at higher temperatures (Fig. 6a, b) is attributed to physical damage of the lattice caused by relatively high electron-phonon scattering. This results in significant decrease in the field-effect mobility as shown in Fig. 7a, b. However, increase in ON state current after stress at 77 K (Fig. 6c) is believed to have improved because of reduction in the number ionized impurity scattering events that led to increased field-effect mobility, Fig. 7c.

HF stress, on the other hand, leads to significant increase in the OFF-state current (3 to 4 orders of magnitude) and loss of gate control. This happens especially when the device is stressed at 300 K and 150 K, as shown in Fig. 6d, e. Another impact of HF stress at these temperatures is that the ON-state current degrades (2 to 3 orders of magnitude). However, HF stress at 77 K results in

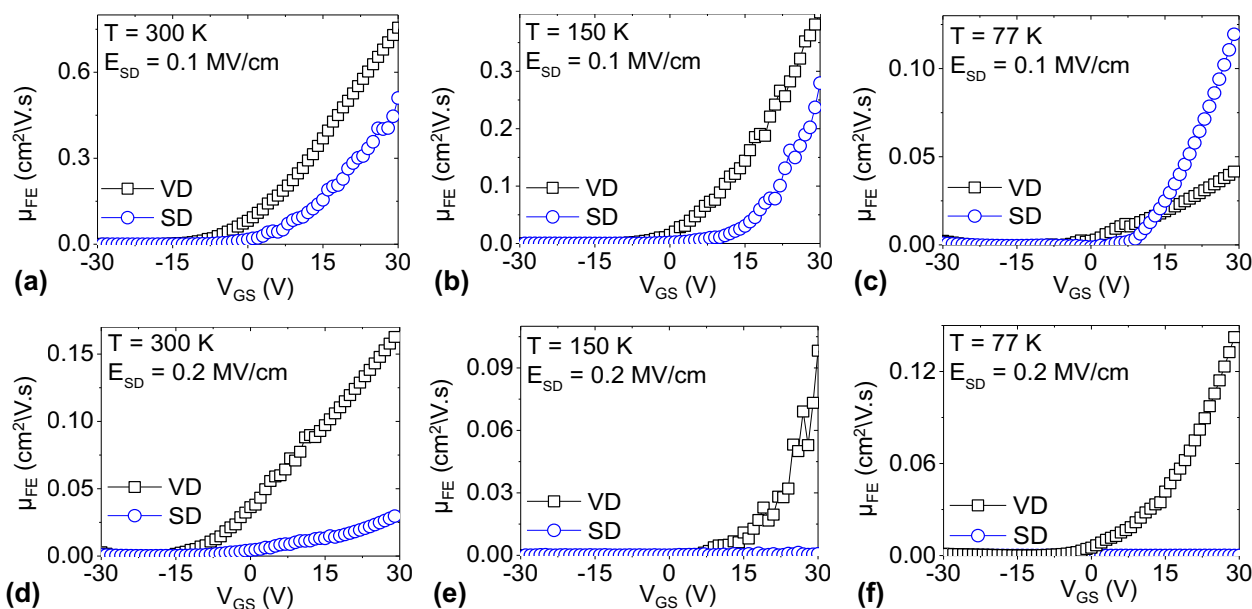


Fig. 7 Impact on carrier mobility. Field-effect mobility extracted from transfer characteristics shown in Fig. 6. Effect of electron-phonon scattering (a, b and d) and impact-ionization (e, f) lead to significant damage of the channel and hence reduction in mobility. (Black curve: VD & Blue curve: SD).

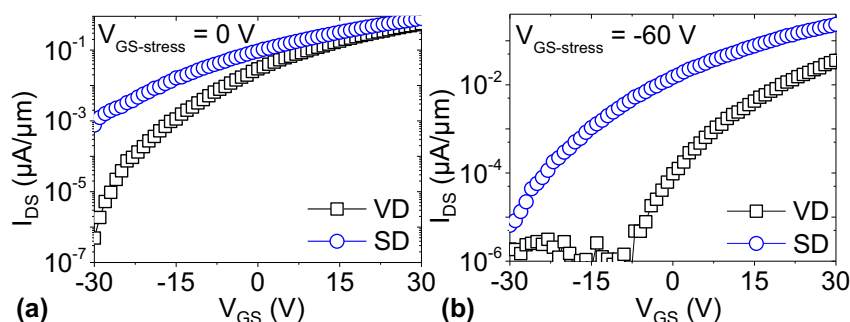


Fig. 8 Impact of stress-gate voltage on transistor behavior. Transfer characteristics of unstressed (VD) and stressed (SD) FETs. SD is stressed at $E_{SD} = 0.2$ MV/cm and $V_{GS} =$ a 0 V and b -60 V.

an overall loss of current, Fig. 6f. Degraded ON state performance is a result of electron-phonon scattering induced partial physical damage to the lattice at 300 K and impact-ionization induced almost complete lattice damage at 150 K and 77 K. This is well corroborated from the observed degradation of field-effect mobility as shown in Fig. 7d–f. Increase in the OFF state current and loss of gate control are attributed to electrical stress induced metal-like transport. A detailed discussion and validation of such a metal-like transport is provided in the next section.

Interestingly, devices stressed at lower gate voltages, shown in Fig. 5, also exhibit high OFF state current and poor gate control as shown in Fig. 8. However, in this case the ON state current increased after the stress cycle. Whereas, as discussed earlier, a stress cycle of $E_{SD} = 0.2$ MV/cm at $V_{GS} = 60$ V leads to abrupt current decay with time and correspondingly results in higher OFF state current, poorer gate control and smaller ON state current. It is important to note that HF stress results in higher OFF state current and degraded gate control of the transistor channel irrespective of the gate voltage during stress cycle. However, ON state current depends on the gate voltage which essentially determines the number of electron-phonon scattering events at room temperature. It appears that higher OFF state current and poor gate control are fallout of a certain lateral field-dependent phenomenon that results in a highly conductive (metal-like) channel when the device is in the OFF state (Figs 5d and 8). Along

with electron-phonon scattering, the same phenomenon determines ON state current i.e. higher (lower) gate voltage during stress degrades (improves) ON state current as shown in Fig. 6d (Fig. 8).

In order to validate stress-enhanced conductance of the channel, 2T terminal channel current (I_{DS} at gate open condition-Fig. 9a) of VDs are measured and compared with that of SDs stressed in the HFR. As shown in Fig. 9b, d, devices stressed at $V_{GS} = 60$ V and $T = 300$ K (to be identified as D-HF-60-300 throughout the text henceforth) and 77 K (to be identified as D-HF-60-77 throughout the text henceforth) exhibit lower conductance after stress. However, stress at 150 K (to be identified as D-HF-60-150) (Fig. 9c) results in increased channel conductance. Similarly, when devices are stressed at $V_{GS} = 0$ and -60 V, the device conductance is found to have increased as shown in Fig. 9e, f. Interestingly, upon successive stress cycles, higher conductance in D-HF-60-300 whereas lower conductance in D-HF-60-150 are observed, Fig. 9b, c (green curve) respectively. Increase in conductance after different stress conditions and cycles can be correlated with poor gate control and higher OFF state current observed in the transfer characteristics earlier. These observations clearly imply that the channel certainly becomes more conductive upon stress under specific conditions and extent to which the channel conductance increases upon stress depends on the gate voltage applied during the stress cycle; for example 1(5) order(s) of

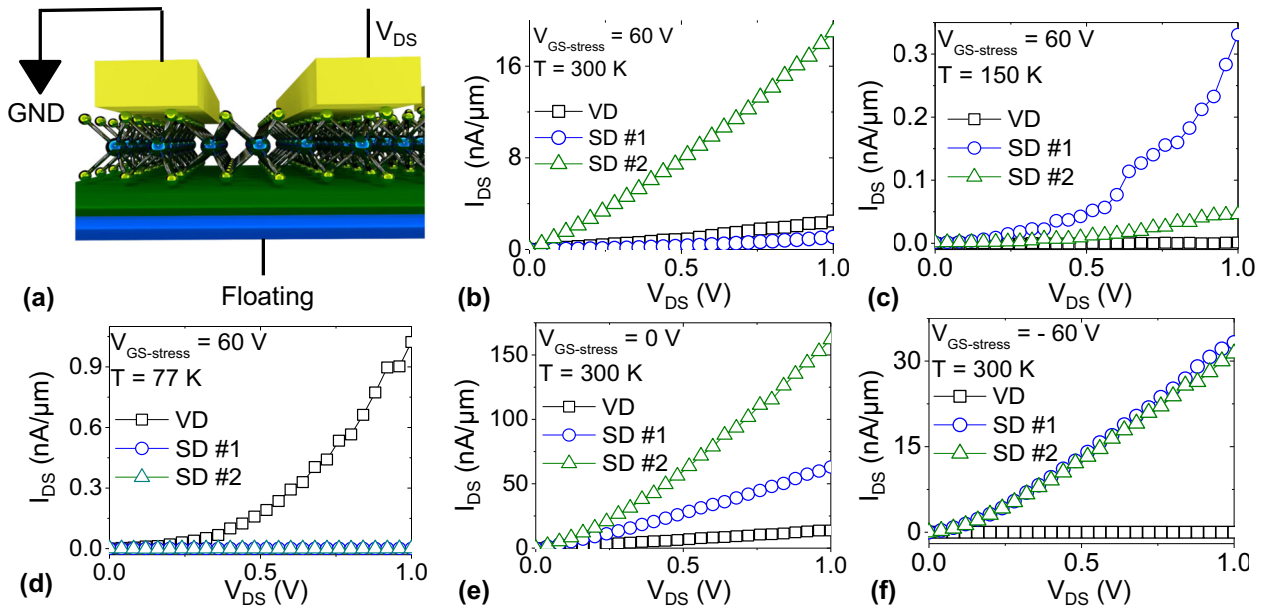


Fig. 9 Measuring two-terminal resistance/current before and after steady-state electrical stress. **a** Bias condition for measuring the 2-terminal current in the channel i.e., when the transistor behaves like a 2-terminal resistor. 2-terminal current of unstressed (VD) and stressed (SD) devices in the HFR at **b** 300 K, **c** 150 K and **d** 77 K is measured as a function of V_{DS} . In order to observe the effect of gate voltage variation, 2-terminal current is measured before and after stressing the device under two different conditions: **e** HFR at $V_{GS-stress} = 0$ V and **(f)** at $V_{GS-stress} = -60$ V both at $T = 300$ K. Here SD #1 (SD #2) implies that the SD device is stressed once (twice).

magnitude increase in conductance at $V_{GS-stress} = 0$ V (-60 V). Note that this comparison is between VD and SD #2. This is attributed to interplay between two mechanisms, (i) electron-phonon scattering resulting in reduced carrier mobility in the channel and (ii) speculated material re-configuration resulting in higher conductance. Under other stress conditions like HF stress at 77 K and subsequent stress cycle at 150 K, channel conductance decreases significantly. This is attributed to impact ionization-induced wide spatial distribution of physical damage of the material under these stress conditions as observed earlier in current versus time curve in Fig. 3. It is important to note that, multiple randomly tested devices have exhibited similar trends in current-time dynamics and stressed induced perturbation in transistor behavior, discussed in Supplementary note 4 and Supplementary Figs. 5–8. This verifies that the observed phenomena occur consistently on all devices and hence are fundamental to CVD monolayer MoS_2 .

Increase in the conductance of the device along with poor gate control and negative shift in V_T implies increase in free-electron concentration in the channel that prevents gate electrode to effectively tune the channel conductance. Moreover, increase in the density of mid-gap states may cause higher sub-threshold and OFF state current by increasing the probability of variable range hopping of electrons between mid-gap states at room temperature³⁶. In order to validate the presence of electrical stress induced increase in the electron concentration, Raman and PL spectroscopy of stressed MoS_2 is performed which is discussed in the next section.

Electrical stress induced material degradation

Raman spectra of different locations across the channel are captured and compared with that of unstressed MoS_2 . As shown in Fig. 10a, the out-of-plane mode, A_{1g} , is found red shifted at multiple positions of MoS_2 channel stressed in the HFR at 300 K. A red shift implies reduced energy of that mode which is essentially the out-of-plane vibrations of the S atoms in MoS_2 . This has been related to increased electron population in MoS_2 ⁴⁰. Further, MoS_2 stressed at 150 K also exhibits signs of increased electron population with a marginal red shift of the A_{1g} mode,

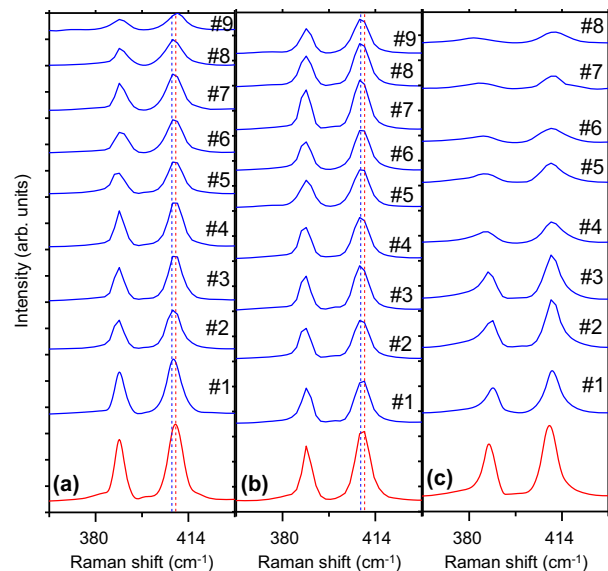


Fig. 10 Impact of stress on material properties. Raman spectra of stressed (under different stress conditions: HF stress with $V_{GS} = 60$ V at $T =$ **a** 300 K, **b** 150 K and **c** 77 K. MoS_2 channel at 10 different spots (blue curves) along the width of the device, $W = 10$ μm , compared with that of an unstressed MoS_2 (red curve) region. Note that raman laser spot size is 1 μm in diameter.

Fig. 10b. These results strongly validate that, as observed earlier in device characteristics, electrical stress induces localized regions with excess electrons that can potentially lead to increased OFF state current, poor gate control and negative shift in V_T . However, for MoS_2 stressed at 77 K, it is observed that the characteristic peaks are not prominent. Moreover, non-zero intensity peaks of the Raman characteristic modes are distributed throughout the range of Raman shift shown in Fig. 10c. This is attributed to amorphization of the MoS_2 and implies physical breakdown of the channel has not occurred. This is in-agreement

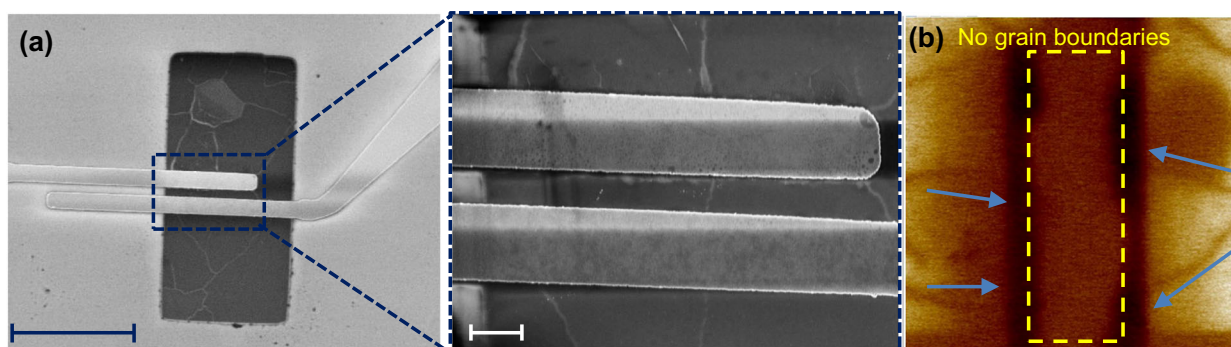


Fig. 11 Impact of impact ionization on channel. **a** SEM (scalebar: 10 μm) top view image of D-HF-60-77 and inset (scalebar: 1 μm) showing continuous channel. This implies that impact ionization did not result in physical discontinuities in the channel. **b** KPFM image of the same device implying that the stressed channel does not have grain boundaries that are otherwise expected because of their orientation outside the channel depicted by blue arrows. Dark regions in the image are metal electrodes, grain boundaries between two MoS_2 grains and other impurities that may have low potential. Bright region is MoS_2 grains that have higher potential than metal and grain boundaries.

with (i) earlier observations of device failure after HF stress at 77 K (Fig. 6f) and (ii) scanning electron microscope (SEM) top view shown in Fig. 11a where a physical break in the channel is not observed. Another important evidence of amorphization is the kelvin probe force microscopy (KPFM) image of the device stressed in HF at 77 K shown in Fig. 11b. KPFM is used to measure surface potential where grain boundaries, mostly S defects, show up as low potential regions. Another low potential region in a typical device scan is the metal electrode. In an arbitrary CVD MoS_2 device, grain boundaries run randomly in and out of the channel without a specified orientation. Typically, if the grains are moderate in size and channel length of the device is large enough, multiple grain boundaries are found to be present within the channel, as shown in Supplementary Fig. 9a. However, in a device stressed in HFR at 77 K, grain boundaries are not observed anywhere within the channel which is attributed to complete amorphization of material resulting in multiple orientations of the crystal at molecular level, difficult to resolve in KPFM. This is also observed in the KPFM scan of a device stressed at 150 K, Supplementary Fig. 9c. Another possibility, complete crystallization of MoS_2 (also without grain boundaries), however, is not obvious because of disagreement with device results in Figs 3 and 6f. KPFM scan of devices stressed in HFR at $V_{\text{GS}} = 60\text{V}$ and 0V are shown in Supplementary Fig. 9b, d. Unusual low potential (dark) regions are observed in the channel between source and drain contacts. These regions are believed to be the source of metal-like behavior observed in transistor behavior where gate control over channel current is lost after the stress. Details of the KPFM measurement setup are discussed in Supplementary Note 5 and Supplementary Fig. 10.

Besides transistor characteristics and micro-Raman spectra, PL spectra of stressed and unstressed MoS_2 channel is also found to strongly validate the presence of electrical stress-induced formation of highly conductive localized regions within the channel. Monolayer MoS_2 is known to exhibit strong PL due to its direct bandgap and strong excitonic features encouraged by its atomically thin structure where electrons and holes are strongly constrained within the monolayer resulting in, strong coulombic force. This facilitates sustained formation of various excitonic species. As shown in Fig. 12a, PL spectra of pristine monolayer MoS_2 has three characteristic peaks: (i) B exciton, (ii) neutral A^0 exciton and (iii) negative A^- trion, which are obtained after deconvoluting the effective PL signal obtained from the CCD detector⁴¹. These peaks correspond to the various photon emission events that occur after incident photons with certain energy create electron-hole pairs which subsequently recombine. While B and A^0 excitons are single electron-single hole pairs that emit characteristic photons due to conduction band (CB) to

light hole and heavy hole valence bands (LHVB and HHVB) respectively, A^- trion is a two electron-single hole pair which emits a relatively low energy photon on recombination from CB to VB^{340} . PL spectra of stressed and unstressed regions are captured at different positions along the width of the channel and deconvoluted to identify different peaks, see Supplementary Note 6 and Supplementary Fig. 11.

In Fig. 12b, it is observed that the intensity ratio of trion peak to neutral exciton peak significantly increases at multiple locations of the device stressed in the HFR at 300 K. For devices stressed at 150 K and 77 K, this ratio remains closer to that in a virgin device, as denoted by dotted horizontal line in Fig. 12b. Remarkable increase in this ratio implies that the number of photons emitted due to negative trion is larger than that emitted from annihilation of a neutral exciton. This suggests that there are more number of trion species formed in the channel stressed at 300 K than neutral exciton species. This is attributed to increase in the free electron concentration⁴¹ and hence validates that, devices stressed at 300 K have multiple localized regions within the channel with higher conductance. Moreover, regions (from position #7 to #9) within the channel of device stressed at 77 K fail to exhibit any of the characteristic peaks. This is attributed to significant damage to the lattice and is also validated by full-width half-maximum (FWHM) values shown in Fig. 12c–e. FWHM of PL characteristic peaks, especially A^0 and A^- , increases for devices stressed at 150 K and 77 K, Fig. 12d, e. While for devices stressed at 150 K, a decent increase in FWHM is observed, for devices stressed at 77 K, FWHM is found to have increased by $\sim 2\times$ for A^0 peak and $\sim 3\times$ for the A^- peak along with huge deviation in FWHM from one channel region to another, as depicted by the error bar in Fig. 12c–e. Typically, FWHM of a PL peak is related to the density of defects in the region of scan. A roughly defined (broad) PL peak (large FWHM) denotes large density of defects as compared to a sharp (small FWHM) PL peak. Therefore, Fig. 12c–e validates the fact that HF stress at lower temperature induces significant damage to the lattice, amorphized channel as discussed above, which eventually results in marginal current through the device.

While it is clearly identified that CVD-grown monolayer MoS_2 undergoes amorphization before complete device failure, the origin of enhanced conductance upon electrical stress is not clear, even after enough validation. Interestingly, this behavior is similar to the one observed by Sangwan et. al. where MoS_2 exhibits resistance switching at SET voltages as high as 30V^{42} . This is attributed to migration of Sulfur vacancies within the channel under the effect of external electric field. Such a behavior has been found to be assisted by grain boundaries present in CVD monolayer MoS_2 . S vacancy migration under electric field

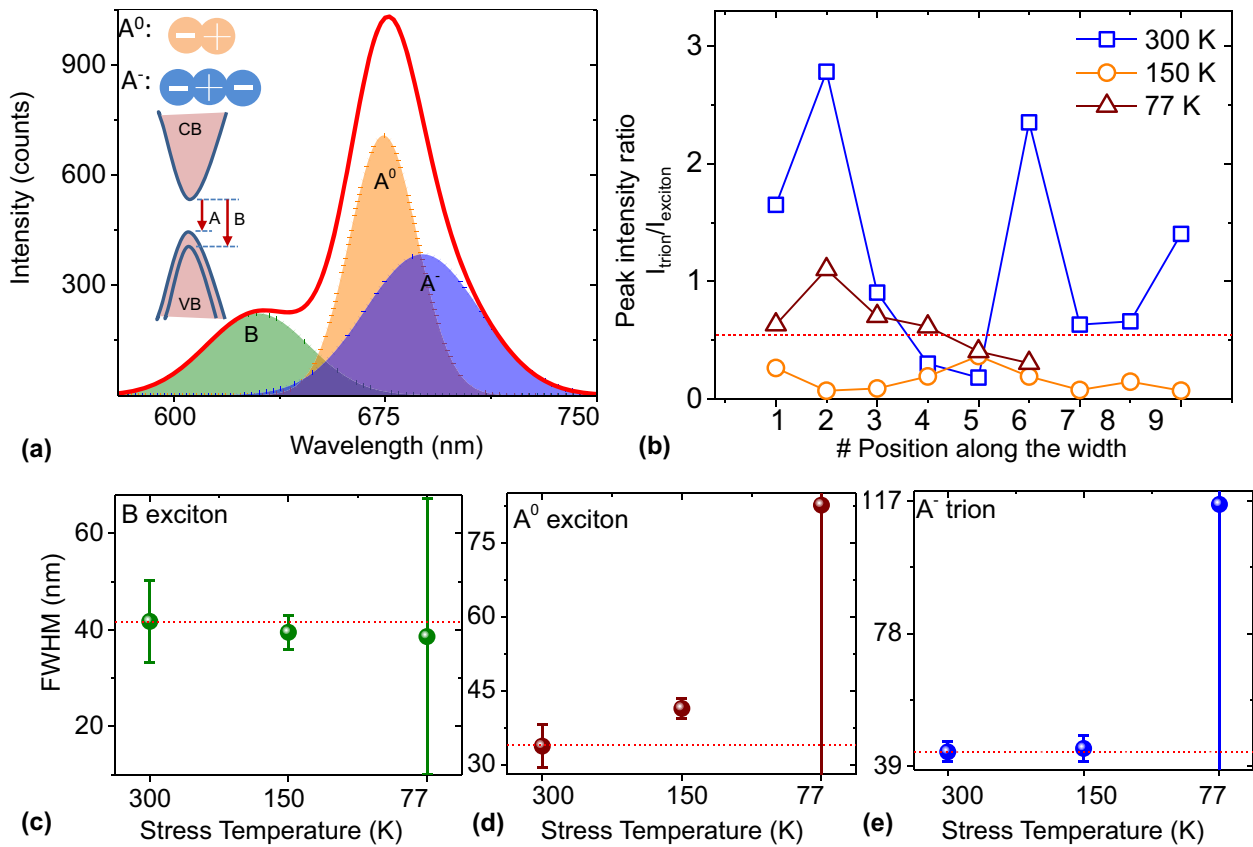


Fig. 12 Impact of stress on various excitonic transitions. **a** PL spectra of monolayer MoS₂ consisting three characteristic peaks corresponding to three different direct energy transitions: B exciton, A⁰ neutral exciton and A⁻ trion. **b** Intensity ratio of trion and neutral exciton peaks at different locations along the width of the channel of devices stressed at different temperatures: 300 K, 150 K and 77 K. The dotted horizontal line denotes intensity ratio in a virgin monolayer MoS₂ channel. Increase in the trion to exciton peak ratio for device stressed at $T = 300$ K implies that the electron concentration is higher than that in a virgin channel. For devices stressed at 77 K, there is no PL signal beyond position 6 which is attributed to physical damage led discontinuity in the lattice. Physical damage or increases in defect concentration can be qualitatively understood by increase in the full-width half maximum (FWHM) of various peaks in the PL spectra. Average FWHM (averaged over different locations along the width of the stressed channel) of **c** B exciton peak, **d** neutral exciton peak and **e** negative trion peak as a function of temperature during electrical stress implies that high voltage electrical stress at lower temperature induces significant damage to the lattice. The dotted red line is the FWHM of different peaks in a virgin MoS₂ channel. Peak intensity ratio and comparison of FWHM for different peaks are extracted from PL spectra for these devices which are shown in Supplementary Fig. 11.

is a potential justification of the observed localized region with excess electrons in an appropriately stressed MoS₂ channel. These localized regions could possibly have accumulated S vacancies and once aligned continuously between source and drain, they result in loss of gate control, negative shift in V_T and higher OFF state current in MoS₂ transistor. The fact that S vacancies in MoS₂ manifest as mid-gap states within the bandgap, justifies that long-term electrical stress increases the density of these mid-gap states, as speculated earlier in sections 3 and 4, by re-distributing the S vacancies in the channel. Moreover, when stressed at lower $V_{GS-stress}$, the channel also exhibits high ON state current due to two reasons: (i) formation of localized high conductive regions, as discussed earlier and (ii) significantly lower electron-phonon scattering induced lattice damage.

In summary, CVD monolayer MoS₂ FETs are operated under low and high field regimes to unveil electro-thermal transport in MoS₂. Low field transport in MoS₂ can be well explained using electron phonon scattering model at different temperatures and gate field. High field transport triggers impact ionization led device failure which is relatively easier to accomplish at lower temperatures. Moreover, it turns out that device failure occurs due to amorphization of the channel due to high field steady state operation. Before complete failure, both low and high field

steady state device operation at room temperature lead to perturbation in transistor behavior wherein the OFF-state performance and gate control degrade which imply metal-like behavior. This unconventional device behavior depends on stress conditions like gate bias, stress voltage and number of stress cycles and is validated by 2-terminal current measurement and micro-Raman & photoluminescence (PL) spectra. While 2-terminal current increased after high field stress, red shift in the A_{1g} mode and enhanced negative trion peaks of different regions within the channel clearly imply the presence of localized regions with higher free-electron concentration. This proves that the performance of MoS₂ transistor degrades under long-term electrical stress by inducing highly conductive regions within the channel and a subsequent loss of gate control. Such a failure mechanism is unusual and understanding its origin is critical for determining a regime for safe operation of MoS₂ transistors. Moreover, such a mechanism limits the terminal voltages for which transistors exhibit acceptable performance. These findings also suggest that voltage scaling employed for silicon transistors may not be the same for MoS₂ and one needs to be more careful in determining these limits because unlike in silicon, a prolonged operation of an MoS₂ transistor leads to

significant increase in the channel current which can have detrimental effects on the overall circuit performance.

METHODS

Device fabrication

Monolayer CVD MoS₂ film grown on Sapphire is transferred onto a 90 nm thick thermally grown SiO₂ on Si substrate and cleaned in acetone and IPA to ensure minimum organic residue on the film. The sample is patterned (using electron beam lithography) in order to define regions for device fabrication. By using oxygen plasma, unwanted MoS₂ is etched out inside a reactive ion etching (RIE) chamber followed by patterning (via electron beam lithography) of regions for source/drain electrode (Ni/Au: 10/50 nm) deposition inside an electron beam evaporator. Subsequent metal lift-off and vacuum anneal for 10 min at 250 °C ensure removal of unnecessary metal from the sample and formation of high-quality metal-MoS₂ interface.

Kelvin probe force microscopy

All KPFM measurements are performed using Bruker dimension icon AFM setup under ambient conditions. The AFM tips used here are Pt/Ir coated silicon probes-SCM-PIT-V2 with a radius of ~25 nm. Scanning a surface to capture potential profile using this AFM setup is a two-pass method in which the tip first scans the surface via line scans in tapping mode followed by a second scan (second pass) during which the tip is lifted at a height (15 nm in this case) and a DC bias is applied to the tip (7 V for these measurements) along with a small AC signal while scanning along the same line with a scan rate of 0.7 Hz. During the first pass, the cantilever is made to oscillate close its resonant frequency.

DATA AVAILABILITY

The data to support findings of this work are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

Ansh and G.S. fabricated all the devices. Ansh performed electrical measurements along with SEM imaging and KPFM scans. Ansh, M.S. and J.K. analyzed the data. Ansh and M.S. wrote the paper.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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