Trap-Assisted and Stress Induced Safe Operating Area Limits of AlGaN/GaN HEMTs

Bhawani Shankar, *Member, IEEE*, Ankit Soni, *Member, IEEE*, Srinivasan Raghavan, and Mayank Shrivastava, *Senior Member, IEEE*

***Abstract*—This experimental study reports a systematic investigation of Safe Operating Area (SOA) limits in AlGaN/GaN HEMT using sub-μs pulse characterization. During stress, on-the fly Raman and CV characterization is done to probe mechanical strain evolution and the resultant defect/ trap generation across HEMT. Role of carrier trapping induced electric field shift and associated piezoelectric strain in SOA degradation is investigated. SOA is reported to recovery under sub-bandgap UV exposure. Impact of gate recess depth on SOA boundary is discovered and its related physics is unveiled. Post failure analysis done using cross-sectional SEM, EDX and HR-TEM corroborates well with the failure physics proposed in this work.**

***Index Terms*—GaN HEMT, safe operating area, stress, trapping.**

I. Introduction

THE OUTSTANDING properties of Gallium Nitride (GaN) such as wide bandgap (3.4 eV), high breakdown field (3.3 MV/cm), good thermal conductivity (1.3 W/cm-K) and low dielectric constant (9) have triggered the replacement of Si by GaN in power device applications. GaN based high electron mobility transistor (HEMT) have shown outstanding performance in high power and high frequency domain [1]. The attractive performance/ cost ratio of GaN HEMT technology have accelerated its penetration in the power device market. However, the failure physics of GaN HEMT is still not clearly understood [2]. A clear understanding of degradation mechanisms in GaN HEMT is required to develop its lifetime models and operate it closer to the GaN material limit. Therefore, reliability of AlGaN/GaN HEMT is now a topic of intense research. Long term reliability of these devices has been studied in greater details in the recent literature [1], [3]–[8]. However, a clear understanding of the physical phenomena active under high electric field and high current injection conditions [9], which define the Safe Operating Area (SOA) limit in GaN HEMT, is still missing in the literature [10], [11]. Therefore, a study to gain insight into possible degradation mechanisms which limit the SOA reliability in GaN HEMT is a worthwhile effort. The present experimental study aims to systematically investigate the evolution and influence of mechanical stress and defects across AlGaN/GaN system, using on the fly Raman spectroscopy during high field and current stress. Raman spectroscopy has been widely used to study piezoelectric stress in GaN devices [12]–[16]. In this work, which is an extension of our earlier study [17], Raman spectroscopy is used for the first time, to probe dynamics of trap induced stress and SOA limits in AlGaN/GaN HEMT. Pulse electrical characterization of HEMTs is done under stress conditions which are more frequently encountered in practical applications. Impact of various technology parameters on SOA reliability is studied. TCAD simulation and post failure analysis of devices is done to gain insight into the degradation physics. The manuscript is structured as follows; details about device fabrication and experimental characterization are presented in Section II. SOA boundary of GaN HEMT and associated degradation trends are presented in Section III. Results showing the impact of carrier trapping and mechanical strain on SOA limit are discussed in Section IV. Section V discloses the roles of gate recess depth in SOA tuning. In Section VI, results from post failure analysis of devices are discussed and physics limiting the SOA in GaN HEMT is proposed. Finally, key findings and conclusive remarks are drawn in Section VII.

Manuscript received May 30, 2020; revised July 27, 2020; accepted October 21, 2020. Date of publication October 26, 2020; date of current version December 8, 2020. This work was supported by the Department of Science and Technology, Government of India, under Grant DST/TSG/AMT/2015/294. *(Corresponding author: Bhawani Shankar.)*

Bhawani Shankar, Ankit Soni, and Mayank Shrivastava are with the Department of Electronic Systems Engineering, Indian Institute of Science, Bengaluru 560012, India (e-mail: bhawani@iisc.ac.in).

Srinivasan Raghavan is with the Center for Nanoscience and Engineering, Indian Institute of Science, Bengaluru 560012, India.

Color versions of one or more of the figures in this article are available online at https://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TDMR.2020.3033522

II. Device Fabrication & Characterization

AlGaN/GaN HEMTs were fabricated on the layer stack as shown in Fig. 1, which was grown on Si (111) using MOCVD, with and without carbon doping in buffer. Ti/Al/Ni/Au metal stack was deposited using e-beam evaporation and later annealed at 870 °C to realize source/drain Ohmic contacts. Devices were MESA isolated on wafer using Chlorine chemistry by Inductively Coupled Plasma - Reactive Ion Etching. O_2/BCl_3 based atomic layer etching was employed to achieve controlled gate recess. D-mode and E-mode devices with varying recess depths were fabricated. Post dielectric deposition and dielectric anneal, Ni/Au gate was deposited followed by soft anneal. All the devices consist of dielectric passivation and field plate.

Pulse I-V characterization of HEMT devices was done to determine the SOA boundary and failure threshold. Voltage pulses of 100 ns duration with 1 ns rise time were generated

1530-4388 © 2020 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See https://www.ieee.org/publications/rights/index.html for more information.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:13:45 UTC from IEEE Xplore. Restrictions apply.

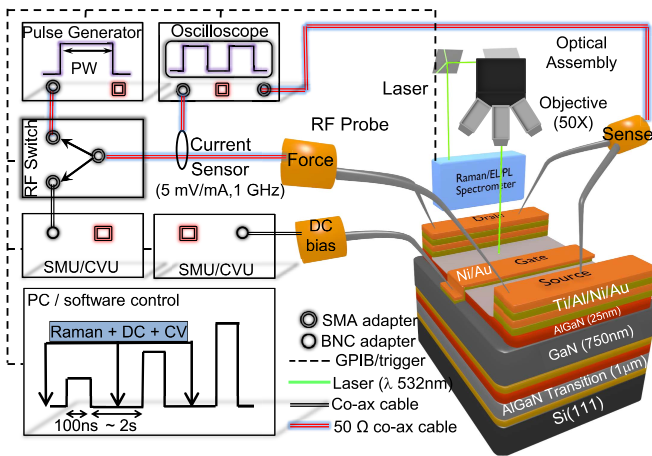

Fig. 1. Experimental set-up with integrated Raman and sub-μs pulse generator used for pulse IV characterization to determine SOA behavior of AlGaN/GaN HEMTs. Schematic of HEMT shows details of different layers present in the AlGaN/GaN stack. The stack is capped with a 3 nm GaN cap (not shown).

using a setup which applies a voltage discharge through a charged transmission line [18]. Pulse voltage was applied at drain using a 50 Ω RF probe (Picoprobe Model 10) while the gate was DC biased using a Source Measure Unit (Keithley 2400). Device voltage and current waveforms were recorded on a digital storage oscilloscope (Tektronix DPO 70404C) with 4 GHz bandwidth, at 25 Gps sampling rate. Recorded waveforms were averaged over 60 to 80 percent window of pulse width (PW) to generate a family of I-V characteristics of the device under test. After each pulse, linear drain-to-source DC current (I_{DC}) was spot measured at small drain-to-source DC voltage to monitor device degradation. DC I-V and capacitance-voltage (C-V) characterization was done at regular intervals between stress routine to record the change, if any, in device parameters and capture the evolution of traps in different regions of the device with stress. C-V characteristics were measured at low frequency (20 kHz). Here, low frequency C-V is used to capture response from the deep level traps, present in GaN, which respond slowly due to their large trapping/ de-trapping time constant [19]. Sub-bandgap UV of wavelength 365 nm, has slightly lower energy than GaN bandgap hence, it can de-trapping carriers from all the deep trap levels present in GaN [20], [21]. Therefore, devices were tested under dark or with UV to study the impact of trapping on SOA reliability. Piezoelectric nature of GaN introduces mechanical strain in device during operation. The increment and nature of mechanical strain can be measured by shift in Raman peaks native to GaN. Therefore, 2D stress profile was recorded across source-drain region, at regular intervals during the test, using on the fly 2D Raman mapping at 532 nm wavelength, as depicted in Fig. 1. All the experiments were conducted at room temperature (300 K).

III. Safe Operating Area

The pulse drain voltage was swept at a fixed gate bias, until the device faced permanent failure. A locus of the failure points defined SOA boundary of the device. Initially, a

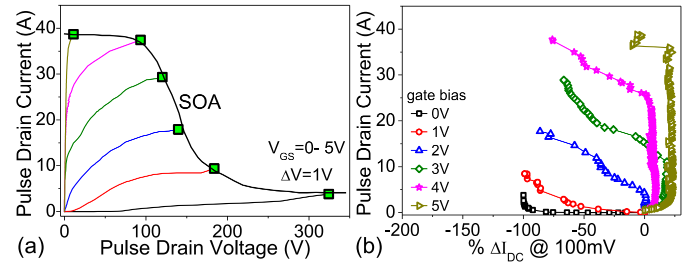

Fig. 2. (a) Pulse IV characteristics of a commercial GaN HEMT with SOA boundary marked. (b) Percentage change in linear drain-to-source DC current (I_{DC}) measured at 100 mV V_{DS} under 2 V V_{GS}, after each stress pulse is applied at drain. Severe degradation is observed at different gate bias with highest degradation (∼100%) under OFF-state.

200 V, 5 A DC rated commercially available E-mode HEMT was characterized to determine its SOA boundary. A family of pulse I-V curves was recorded for gate voltage varied from 0 to 5 V with increment of 1 V. For each curve in the I-V family, a new/ pristine device was measured. During measurement, no recovery was done between two consecutive pulses. Figure 2(a) shows the pulse I-V characteristics of the commercial device with SOA. The device showed high OFF-state leakage beyond 50 V. Also, the drain-to-source DC current (I_{DC}) was spot measured at 100 mV V_{DS} under 2 V gate bias, after each stress pulse. Figure 2(b) shows the percentage change in I_{DC} (on x-axis) with pulse stress current (on y-axis) at different gate bias. Any change in I_{DC} compared to its unstressed/ pristine value, is considered as marker of device degradation [11]. The result discloses the following; (i) Device degrades (I_{DC} drops) with each stress pulse. (ii) Degradation occurs to a different extent depending on the gate bias. (iii) Maximum degradation occurs in the OFF state where I_{DC} changes by ∼ 100%. This corroborates well with the high OFF state leakage as evident in Fig. 2(a).

Next, SOA characterization of fabricated device was done. Firstly, devices were tested in dark to obtain their IV characteristics. During normal HEMT operation, a significant carrier trapping occurs in different regions of the device which deteriorates its performance. However, there exists a limited understanding on the trap dynamics under high current injection and high electric field, and its impact on the HEMT's SOA boundary. To investigate the role of traps on SOA boundary, if any, devices were studied in dark and under sub-bandgap UV. Fig. 3(a) compares the IV characteristics and SOA of a device extracted in dark and under sub-bandgap UV. Following observations are worth noting; (i) Drain current suffered significant collapse, (ii) device exhibited higher R_{ON} (see Fig. 3a-Inset) and (iii) lower breakdown voltage in ON-state when tested under dark condition. Device I-V characteristics obtained under UV showed no current collapse, possessed lower R_{ON} (see Fig. 3a-Inset) and improved I_{ON} and V_{BD} in ON-state. It is worth highlighting that, ∼ 35% broader SOA was observed under UV than in dark. SOA improvement with UV exposure signifies a hidden role of surface and/or buffer traps on SOA reliability. Figure 3(b) shows the variation in spot measured drain current of the corresponding device tested in dark and UV conditions. Drain current degraded step-by-step with each stress pulse under dark, similar to that in the

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:13:45 UTC from IEEE Xplore. Restrictions apply.

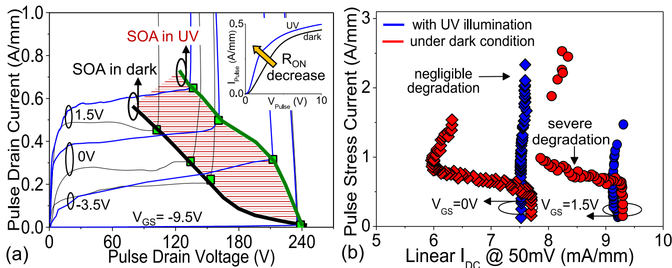

Fig. 3. (a) Safe Operating Area of AlGaN/GaN HEMT under dark and UV condition. Figure highlights the trapping limits SOA boundary. (b) Comparison of degradation in linear drain current measured after each stress pulse, under dark and UV conditions. UV illumination effectively suppresses degradation by assisting in the carrier de-trapping.

commercial device (Fig. 2b). However, a negligible degradation can be observed in the device when stressed in presence of UV. Same behaviour persists at different gate bias. The above observations hint that carrier trapping plays decisive role in device failure physics and SOA degradation and is discussed next.

IV. Trapping and Stress Induced SOA Limit

To understand the role of traps in degradation physics of SOA, a HEMT structure was simulated in TCAD Sentaurus at different trap concentrations. Polarization charges were considered at all material interfaces present in the HEMT stack. Impact ionization based on Chynoweths Law, was considered with critical field set to 3 MV/cm for GaN. Hot electron effects were considered as they can influence the trap dynamics and create new traps. Further details of the simulation setup and its calibration can be found in our other work [22]. Surface and buffer traps can have significant effect on field distribution in HEMT [23]. Therefore, acceptor trap with energy level; $E_V + 1.3$eV was considered in undoped GaN buffer with Gaussian distribution. This particular acceptor trap is intrinsic to GaN material and corresponds to V_{Ga}-O_N complex commonly found in undoped GaN buffers [24]. Oxygen and Nitrogen impurities introduce donor levels in GaN and give rise to unintentional background doping (UID) of n-type (~1E15 cm^{-3}) in undoped buffer. In simulation, influence of donor traps on HEMT, is accounted by considering 1E15 cm^{-3} UID in GaN buffer. No impact of donor traps, on channel electric field was noticed, since the donor concentration is typically 3 orders lower than the acceptor trap concentration in undoped GaN. Trapping effect from the surface states were not studied because the devices used in this study were passivated. The total electric field in gate-drain access region, was simulated at different acceptor buffer trap concentrations. Field distribution was extracted in GaN, at 4 nm away from AlGaN/GaN interface where 2DEG existed. Figure 4 shows distribution of the total electric field between gate and drain, simulated for different buffer trap concentrations in HEMT under V_{DS} 60V and V_{GS} −6V bias condition. Without traps, the peak electric field resides at gate edge as expected ideally. This is the case, when the device is expose to sub-bandgap UV which de-traps carriers from deep levels. Therefore, under UV exposure, the peak electric field lies at drain side gate edge. On the other hand, device under dark, suffers significant carrier trapping which increases with stress level and time. Therefore, as the concentration of trapped charges increases, the peak field at gate edge suppresses while field enhances at drain end. Consequently, under dark the peak field resides at drain unlike that under UV. In summary; simulation results revealed that the peak electric field in the channel shifts from gate to drain edge in presence of high buffer trap density, which is equivalent to the case of I-V measurements done under dark. In absence of traps the electric field peaks at the gate edge which occurs when the UV exposure was present while stressing the device. Therefore, traps can modify the field distribution and hereby potentially govern the device degradation via field driven mechanisms like inverse piezoelectric effect as discussed next.

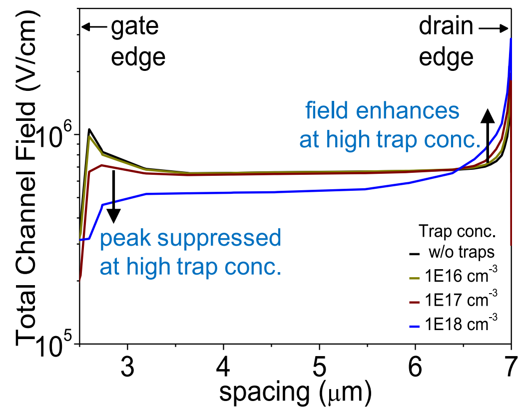

Fig. 4. Simulated electric field profile in channel, with and w/o buffer traps under 60 V V_{DS} and −6 V V_{GS} bias condition.

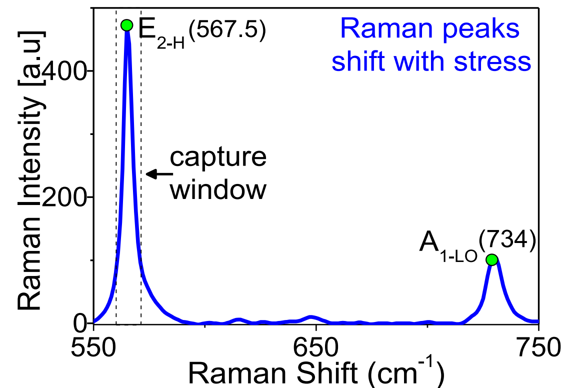

Fig. 5. Spot measured Raman spectra of bulk GaN showing the dominant Raman modes.

A. Influence of Stress

Electric field introduces mechanical strain in GaN devices as GaN is a piezoelectric material. And traps modify the field distribution in GaN HEMT, as discussed above. So, any change in field distribution is also expected to alter the mechanical stress profile within the device. To have clear understanding of the trap induced stress redistribution, if any, the device's mechanical strain profile is determined in presence and absence of traps. For this, a device was stressed under dark and UV conditions. In dark, the device undergoes significant trapping. UV

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:13:45 UTC from IEEE Xplore. Restrictions apply.

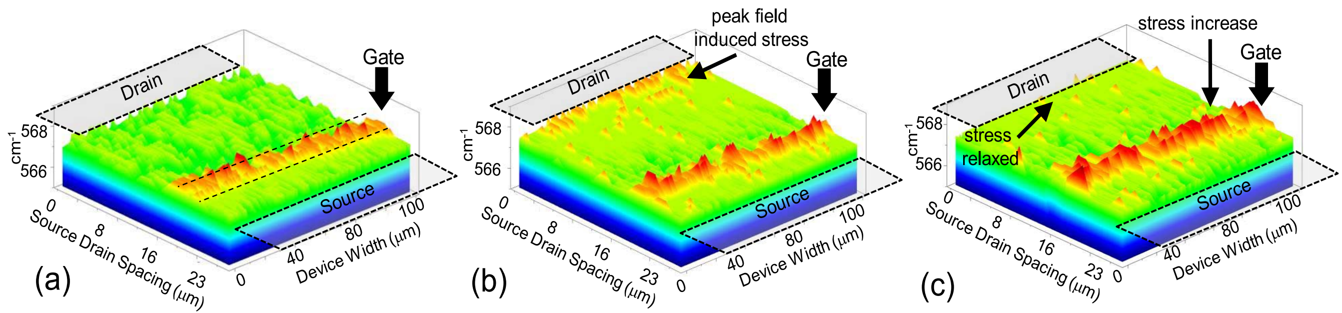

Fig. 6. (a) Raman map captured in source-drain region of pristine device, before stress. On the fly Raman map was captured during OFF-state stress (V_{DS} 60V@ V_{GS} −6V) (b) in dark and (c) with UV illumination on device.

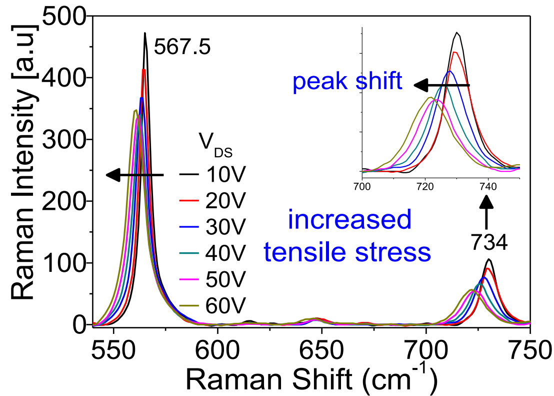

Fig. 7. Raman spectra spot measured, under ON-state, at gate edge towards drain at different drain stress. Left shifting in E_{2-H} (567.5 cm^{-1}) and A_{1-LO} (734 cm^{-1}) Raman peaks of GaN reveal increased tensile stress at gate edge with increase in drain voltage.

exposure assists in carrier de-trapping and is considered here as the case without traps. Figure 5 shows the Raman peaks namely; E_{2-H} / 567.5 cm^{-1} and A_{1-LO} / 734 cm^{-1} for GaN, recorded at room temperature. The phonon frequency reduces in presence of tensile strain and its vice a versa for compressive strain [12]. 2D map of the stress distribution in source to drain region was recorded using on the fly Raman spectroscopy at regular intervals during the pulse stress. The device was mounted on a motorized x-y stage which moved in steps of 0.5 micron while Raman spectra was acquired over frequency range 550-750 cm^{-1} with spot size 1 micron at room temperature. Firstly, Raman map of the device was recorded in unstressed pristine state. As mentioned earlier, a shift in E_{2-H} Raman mode represents a biaxial strain in GaN epi films, therefore the Raman map corresponding to the E_{2-H} analysis window (shown in Fig. 5) represents the distribution of mechanical strain in the device. Figure 6(a) shows a spatial variation of Raman map recorded in the pristine device, before stress that is under zero bias condition. It unveils the presence of residual compressive stress under the gate finger which originates from CTE (coefficient of thermal expansion) mismatch in gate metals and underlying GaN during fabrication process. Source and drain contact edges appeared relaxed.

1) Stress Evolution in OFF-State: Next, stress profile is investigated in device's OFF-state where maximum trapping occurs. With no current flowing in OFF-state, the thermoelastic stress associated with self-heating is absent in device and only piezoelectric stress gets recorded. The device is stressed at drain under gate pinch-OFF condition in dark and stress map as shown in Fig. 6(b) is acquired during the test. Figure 6(b) reveals that in addition to the gate, a compressive stress also builds up at the drain contact edge at several points in gate-drain drift region when device is stressed under dark. On the other hand, when test is repeated under UV illumination, the compressive stress at drain and in drift region was missing. Only a high compressive stress was present at the gate as depicted in Fig. 6(c). Comparison of Fig. 6(a) and Fig. 6(c) reveals that apart from residual stress, an additional stress builds up at gate. This indicates the presence of high field at gate edge in absence of traps (under UV). However, in presence of trapping (under dark), stress accumulation occurs at the otherwise relaxed drain edge and points to field enhancement at drain edge in presence of traps. These observations corroborate well with simulation results in Fig. 4 which shows trap induced peak field shift from gate to drain edge in device. Now it is clear that when device is stressed under dark, carrier trapping in buffer and barrier region causes peak electric field to shift from gate to drain edge and causes stress accumulation at drain edge. UV exposure, suppresses trapping by de-trapping carriers and restored the peak field back to drain side gate edge and builds up stress at gate edge.

2) Stress Evolution in ON-State: Next, mechanical stress distribution is investigated during ON-state stress. A device is stressed at drain with gate biased at 1 V under dark. During test, Raman spectra is spot measured at gate edge at different stress levels as shown in Fig. 7. E_{2-H} (567.5 cm^{-1}) and A_{1-LO} (734 cm^{-1}) frequencies reduces and the Raman signature shifts towards left with increasing stress at the drain as depicted in Fig. 7. This shows that the tensile strain present in gate vicinity increases with drain stress voltage. Increased mechanical strain leads to increment in stored elastic energy. Beyond a certain strain level, defects/cracks are formed in gate vicinity and gate-drift region when elastic energy hits its critical value [8]. To verify this, DC I-V and C-V characterization were done at regular intervals during the stress. C_{GS}, C_{GD} and C_{GG} capacitance were measured at 20 kHz and trap density was determined using capacitance-conductance technique [25], [26] in gate, gate-to-source and gate-to-drain regions, at different stress levels. Here, low frequency was used to capture the maximum trap response. Figure 8(a) shows the variation in trap density in various regions of the device.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:13:45 UTC from IEEE Xplore. Restrictions apply.

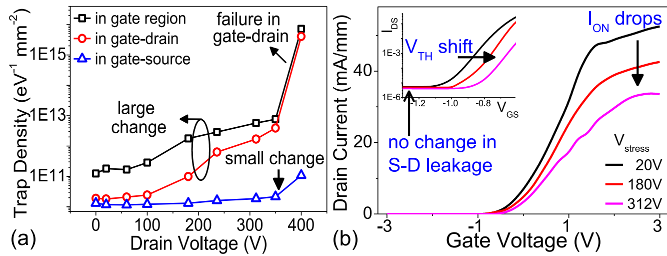

Fig. 8. (a) Increase in trap density captured after each stress voltage pulse. Rapid increase in trap density in gate-drain region can be seen. (b) Transfer characteristics of HEMT recorded at regular intervals during the test shows positive shift in threshold voltage and drop in I_{ON} with increase in drain stress.

Till 50 V stress, no change was noticed in trap density all three regions. Beyond 50 V stress, the trap density in gate-drain region began to increase rapidly however, trap conc. in gate-source region still stayed unchanged. The significant rapid increase in trap density in the gate-drain region is attributed to the thermoelastic stress developed in gate vicinity due to presence of hotspot [11] at gate edge which generates new defects in already strained high field gate-drain region. In absence of any serious field in gate-source region, its trap density remained unaltered. However, at device failure a slight increase in trap conc. was noticed which was a manifestation of partial damage in gate-source region on device failure as confirmed in post failure analysis of the device. Increased strain introduces new defects/trap levels in device and can potentially degrade its performance over time. DC IV characteristics of device were measured at predefined pulse stress level. Fig. 8(b) shows the variation in transfer characteristics of the device after 20 V, 180 V and 312 V stress applied at drain. A positive V_{TH} shift is noticed with increase in stress, as depicted in Inset of Fig. 8(b) and points to accumulation of negative charge underneath gate via electron trapping. I_{ON} constantly drops with stress which is a result of (i) positive V_{TH} shift which reduces gate over drive and (ii) increased R_{ON} due to defect generation and trapping in gate-drain region as discussed above.

V. Gate Recess Dependent SOA Tuning

In previous section, trapping driven SOA degradation was discussed. The findings revealed that, traps in buffer, modulated the field profile in channel and shifted the peak electric field from gate to drain edge which lead to stress accumulation / defect generation at drain end and limited device's SOA boundary. SOA degradation was studied in devices with different gate recess depth. For this study, devices were realized having gate recess depth 12 nm, 15 nm, and full-recess (28 nm recess depth). Pulse I-V characteristics and SOA boundary of devices with different recess depth was determine as shown in Fig. 9(a)-(d). It is worth mentioning that, to nullify the effect of V_{TH} variation across devices with different recess depth, effective gate voltage (V_{GS}-V_{TH}) was considered. Following are the key observations to highlight; (i) increase in recess depth increases I_{ON}. For instance, in device with recess depth (t_R) 0, 12, 15 nm I_{ON} is 0.25, 0.3, 0.4 A/mm respectively

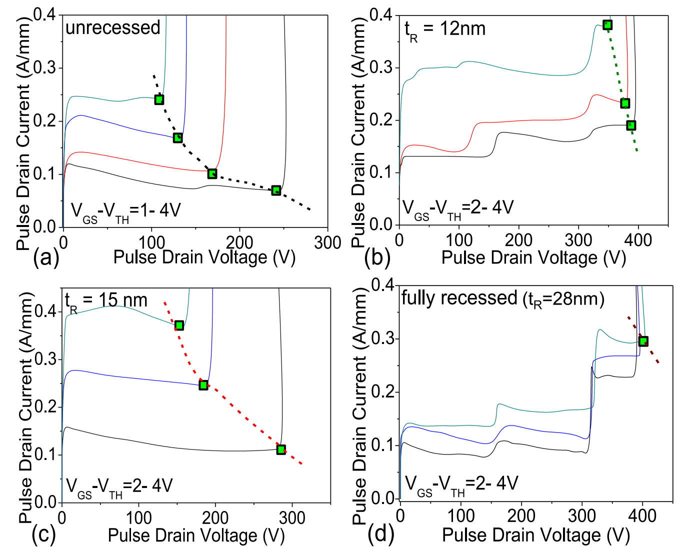

Fig. 9. (a) SOA boundary of devices with different gate recess depth (t_R). (a) Figures shows narrow SOA boundary in HEMT without recess. (b)-(d) shows SOA of devices with increasing recess depth. Figure reveals that with gate recess the SOA broadens however, with fully recessed gate as in (d) device failure occurred at a fixed drain voltage irrespective of the gate bias and reveals field limited SOA in fully recessed structure.

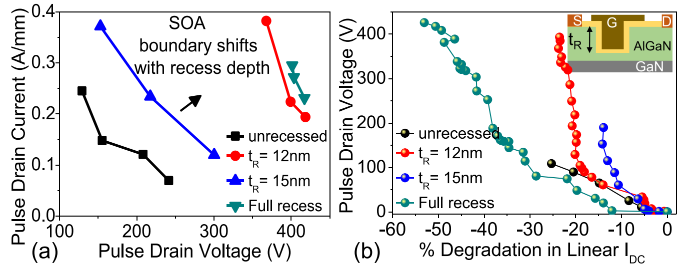

Fig. 10. (a) Shift in SOA boundary with gate recess depth is observed, with optimum SOA achieved with 15 nm recess depth. (b) Percentage degradation in linear drain current for devices of different recess depth, drain stressed under ON-state (V_G-V_{TH} = 4 V). Inset shows schematic of HEMT with recessed gate where recess depth (t_R) is varied.

at effective gate voltage 4V. (ii) In fully recessed structure, very low I_{ON} is observed. The high channel resistance in fully recessed structure limited device current exhibiting minimum gate influence. (iii) Device without gate recess exhibited a narrower SOA as depicted in Fig. 9(a), while in device with full recessed gate, the failure occurred around 400 V drain voltage independent of applied gate bias as seen in Fig. 9(d). This reveals field limited SOA in fully recessed structure and points to a possibility of field modulation with recess depth, as discussed later. Step increase in drain current at higher drain voltage in Fig. 9(b) and Fig. 9(d) is attributed to the Kink Effect [27]. Figure 10 presents a comparison of SOA boundaries of devices with different recess depth extracted from their pulse IV characteristics shown in Fig. 9. It reveals that SOA boundary shifts with change in gate recess depth. Device with unrecessed gate showed narrow SOA (black line) while SOA boundary also shrunk in fully recessed gate structure. Comparatively, broader SOA was observed in partially recessed structures (t_R = 12 nm, 15 nm). These observations hint that device SOA can be tuned with recessed gate. To

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:13:45 UTC from IEEE Xplore. Restrictions apply.

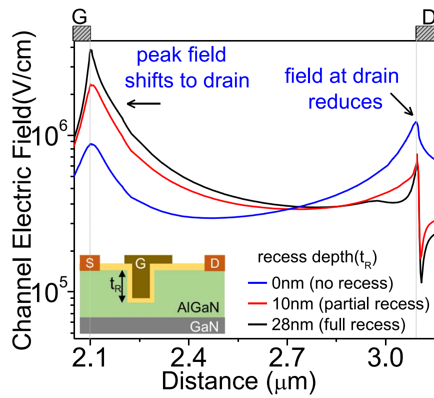

Fig. 11. Electric field profile in gate-drain access region simulated for different gate recess depth. Inset shows schematic of HEMT with recessed gate where recess depth (t_R) is varied.

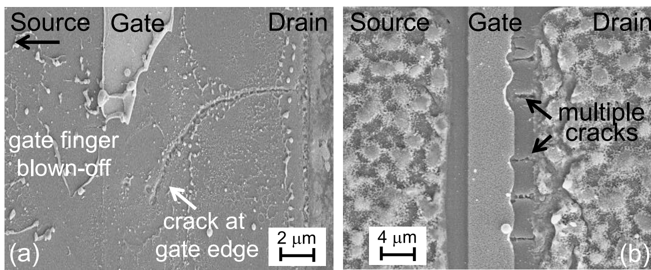

Fig. 12. (a) Post failure SEM image of device failed under OFF-state in UV exposure. Figure shows cracking underneath gate blew-off the gate finger which was already under compressive stress as clear from Raman plots. (b) SEM image of device failed in OFF-state under dark. Multiple damages observed in gate-drain region reveal failure due to non-uniform trapping and stress distribution along device width as shown in Fig. 6(a)–(c).

understand the root cause of SOA dependence on recess depth, linear drain to source current was spot measured in each case. Figure 10(b) presents a comparison of distinct degradation trends in drain current as function of gate recess depth. Devices without recess undergo up-to 30% degradation in drain current, while devices with 15 nm recess depth degrades only up-to 10%. On the other hand, fully recessed devices suffered from maximum degradation of 90%. It unveils that the percentage degradation in the device reduces with increase in recess depth however, fully recessed structure exhibited maximum degradation. As highlighted in discussion above, device with full recess gate faced field dependent failure (Fig. 9(d)) and SOA limit (Fig. 10(a)). Further, it suffered maximum degradation (Fig. 10(b)). All these observations point to possible field variation with recess depth and is worth investigating.

To investigate the physics of SOA variation with gate recess, HEMT structure with recessed gate was simulated in TCAD. Gate recess depth was varied and electric field distribution in channel was determined for different recess depths. Figure 11 shows a variation in electric field distribution in gate-drain region with increase in gate recess depth (t_R). In non-recessed structure, electric field peaks at drain in presence of high buffer trap density as discussed above (Fig. 4). On the other hand, peak field lies at the gate edge in fully recessed structure. So, with increase in recess depth, peak field shifts from drain to gate edge in high buffer trap density scenario. Furthermore, for an intermediate optimum recess depth, the field redistributes such that peak field gets suppressed both at gate and drain edges. Field suppression at drain reduces impact ionization rate and avoids early avalanche in device. Low field at gate, slows the hotspot formation and hot electron induced degradation. Therefore, redistribution of electric field in access region with suppressed peaks at optimum recess depth, improves device reliability and broadens the SOA. This explains the as observed dependence of SOA on recess depth as seen in Fig. 10(a).

To summarize; the SOA boundary in HEMT varied with recess depth. Devices degraded to different extent when stressed under similar conditions. Fully recessed structure faced rapid degradation with increasing stress whereas devices with partial gate recess encountered relatively low degradation. In depth analysis revealed channel field redistributed with variation in gate recess depth which altered field dependent degradation in device and resulted in SOA boundary shift with recess depth. At optimum gate recess, peak field in channel gets suppressed resulting in maximum SOA in HEMT.

VI. Failure Analysis

After pulse characterization, the damaged regions of failed devices were analyzed using Scanning Electron Microscopy (SEM), Energy Dispersive X-Ray Spectroscopy (EDX) and Transmission Electron Microscopy (TEM) to gain physical insight into the underlying degradation mechanism.

A. *OFF-State Failure*

Figure 12(a) shows the post failure SEM micrograph of a device which failed in OFF-state under UV condition. It depicts a part of gate metal finger blown-off at failure without any trace of material melting. This highlights the possibility of purely field driven failure. Presence of crack underneath gate edge towards drain side, confirmed that the damage occurred due to high mechanical strain at gate edge in absence of trapping in presence of UV. This observation nicely corroborates with the Raman stress map of device under UV as shown in Fig. 6(c) where the region under gate finger was found under a high compressive stress. The inverse piezoelectric effect introduced mechanical strain at gate because the channel electric field peaked at the gate edge in absence of carrier trapping (under UV) as revealed by TCAD results in Fig 4. SEM image of a device which failed under OFF-state stress in dark is shown in Fig. 12(b). It unveils cracking in gate-drain region and damaged drain edge. In presence of high trap density, the peak field lies at drain edge under dark condition as disclosed by results in Fig. 4. Peak field led to mechanical stress accumulation at drain end as captured in Raman map shown in Fig. 6(b). Beyond critical strain magnitude, cracks seed at drain edge and damage the gate-drain region. Multiple cracks are observed along device width because the MOCVD grown AlGaN/GaN stack, possess a finite defect density which can introduce non-uniformity in carrier trapping and associated peak field shift, at drain, along the device width. Enhanced impact ionization and carrier injection into the buffer, in these localized high field regions invokes avalanche instability and causes multiple damages [11] as seen in Fig. 12(b).

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:13:45 UTC from IEEE Xplore. Restrictions apply.

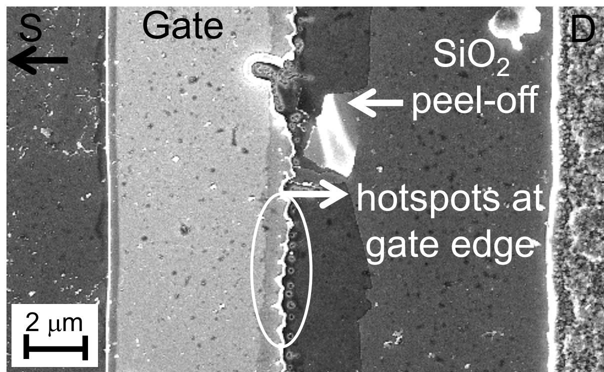

Fig. 13. On-state failure in device occurred with multiple damages/hotspots along the gate edge. Surface passivation is also observed to peel-off in gate vicinity.

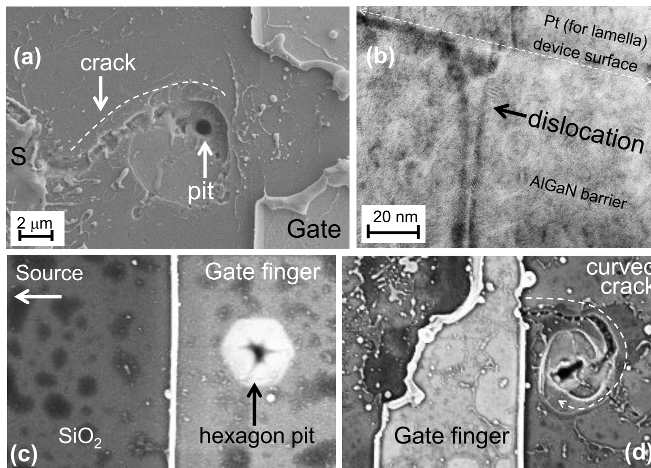

Fig. 14. (a) Failure image of a device which faced premature failed under ON-state. Damage occurred in gate-source region, at a pit located near gate edge. (b) Cross-section TEM image taken across the pit in (a), shows presence of dislocation underneath the pit. (c) A hexagonal pit present under gate finger in a pristine device. (d) A crack originating from a pit present in gate-drain region. Interestingly, the crack followed curved trajectory as in (a).

B. ON-State Failure

Devices under ON-state stress, failed with multiple damages along gate edge as shown in Figure 13. The localized pit-like damages with metal melting, highlight thermal nature of the failure mechanism. Presence of hotspot at gate edge under ON-state possibly led to these localized failures along gate width [28]. Moreover, the increment in tensile thermoelastic stress in gate vicinity as unveiled by Raman spectra in Fig. 7, caused surface SiO_2 passivation to peel-off as seen in Fig. 13.

C. Parasitics Induced Failure

Device can face premature failure due to secondary effects like parasitics. Figure 14(a) shows failure image of a device which faced premature breakdown under ON-condition. It reveals that presence of a pit triggered device failure in gate-source region. A cross-section TEM image taken across the pit unveiled presence of a dislocation as seen in Fig. 14(b). Pits and dislocations are native to AlGaN/GaN material system and originate from lattice mismatch between GaN and underlying substrate. They pierce through the material stack and terminate into hexagon-shaped pits at device surface. Dislocation cores can be electrically charged and provide unwanted current leakage path if present in active region of device as seen in Fig. 14(c) where a hexagonal pit is present underneath the gate finger. Such pits or dislocation are also path for material diffusion and can potentially weaken the material locally [29] and trigger cracking as shown in post failure image of a device in Fig. 14(d) which prematurely failed in ON-state.

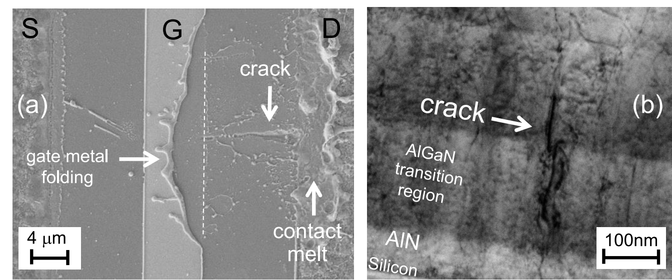

Fig. 15. (a) OFF-state failure occurred with crack in gate-drain region with gate metal folding. (b) TEM cross-section image taken across the crack along the white dotted line in (a), shows damage in bulk reaching till Si substrate.

Another device failed in UV under OFF-state showed an interesting observation. Its post failure image in Fig. 15(a) shows that failure occurred with a crack in gate-drain region and gate metal folding exclusively at the drain side gate edge. TEM cross-section was taken along the gate edge (white dotted line in Fig. 15(a). It unveils that a damage also occurred deep in the GaN buffer with the newly formed crack reaching till the Si substrate. Possibly the stress accumulation occurred in presence of peak field at gate, without traps (under UV), also influenced the bulk material. However, further investigations are required to draw a complete failure picture in this case and is presently beyond the scope of this work.

VII. Conclusion

This work investigates influence of key technology parameters on the SOA limits of AlGaN/GaN HEMTs. SOA boundary in OFF-state was found to deteriorate due to compressive strain at drain edge. Carrier trapping shifts peak electric field towards drain which results in strain accumulation at drain edge. ON-state SOA limited by tensile strain in the gate-to-drain region. Increased strain leads to defect generation and increased trap density in gate-drain region. OFF-state failure was found to be field driven while ON-state failure exhibited thermal nature. It is found that electric field profile in channel and buffer can be tuned by controlling the gate recess depth which directly affects device degradation. Dependence of SOA boundary on gate recess is discovered and is exploited to maximize the SOA boundary in AlGaN/GaN HEMTs. Proposed failure modes under ON and OFF state corroborate well with post failure analysis done using cross-sectional SEM, EDX and HR-TEM.

Acknowledgment

Bhawani Shankar would like to acknowledge Sayak D. Gupta and Abhishek Mishra for the hardware support.

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:13:45 UTC from IEEE Xplore. Restrictions apply.

References

[1] G. Meneghesso *et al.*, "Reliability of GaN high-electron-mobility transistors: State of the art and perspectives," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 332–343, Jun. 2008. [Online]. Available: https://doi.org/10.1109/TDMR.2008.923743

[2] B. Shankar *et al.*, "Time dependent early breakdown of AIGaN/GaN epi stacks and shift in SOA boundary of HEMTs under fast cyclic transient stress," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2018, pp. 1–4. [Online]. Available: https://doi.org/10.1109/IEDM.2018.8614690

[3] J. del Alamo and J. Joh, "GaN HEMT reliability," *Microelectron. Rel.*, vol. 49, nos. 9–11, pp. 1200–1206, 2009. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0026271409002364

[4] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 560–566, Mar. 2001. [Online]. Available: https://doi.org/10.1109/16.906451

[5] S. C. Binari *et al.*, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 465–471, Mar. 2001. [Online]. Available: https://doi.org/10.1109/16.906437

[6] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi, and E. Zanoni, "Current collapse and high-electric-field reliability of unpassivated GaN/AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2932–2941, Dec. 2006. [Online]. Available: https://doi.org/10.1109/TED.2006.885681

[7] J. Joh and J. A. del Alamo, "A current-transient methodology for trap analysis for GaN high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 132–140, Jan. 2011. [Online]. Available: https://doi.org/10.1109/TED.2010.2087339

[8] B. Shankar, S. Raghavan, and M. Shrivastava, "Distinct failure modes of AlGaN/GaN HEMTs under ESD conditions," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1567–1574, Apr. 2020.

[9] B. Shankar and M. Shrivastava, "Unique ESD behavior and failure modes of AlGaN/GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Pasadena, CA, USA, 2016, pp. 1–5. [Online]. Available: https://doi.org/10.1109/IRPS.2016.7574608

[10] X. Huang *et al.*, "Experimental study of 650V AlGaN/GaN hemt short-circuit safe operating area (SCSOA)," in *Proc. IEEE 26th Int. Symp. Power Semicond. Devices IC's (ISPSD)*, Waikoloa, HI, USA, Jun. 2014, pp. 273–276. [Online]. Available: https://doi.org/10.1109/ISPSD.2014.6856029

[11] B. Shankar *et al.*, "Trap assisted avalanche instability and safe operating area concerns in AlGaN/GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, Apr. 2017, pp. 1–5. [Online]. Available: https://doi.org/10.1109/IRPS.2017.7936414

[12] A. Sarua *et al.*, "Piezoelectric strain in Al Ga N/Ga N heterostructure field-effect transistors under bias," *Appl. Phys. Lett.*, vol. 88, no. 10, 2006, Art. no. 103502. [Online]. Available: https://doi.org/10.1063/1.2182011

[13] M. Power *et al.*, "Reverse-biased induced mechanical stress in AlGaN/GaN power diodes," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Prague, Czechia, Jun. 2016, pp. 103–106. [Online]. Available: https://doi.org/10.1109/ISPSD.2016.7520788

[14] B. Shankar, A. Soni, and M. Shrivastava, "Electro-thermo-mechanical reliability of recessed barrier AlGaN/GaN schottky diodes under pulse switching conditions," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 2044–2051, May 2020.

[15] B. Shankar *et al.*, "Trap assisted stress induced ESD reliability of GaN schottky diodes," in *Proc. 40th Elect. Overstress/Electrostat. Discharge Symp. (EOS/ESD)*, Reno, NV, USA, 2018, pp. 1–6.

[16] B. Shankar *et al.*, "Time dependent shift in SOA boundary and early breakdown of epi-stack in AlGaN/ GaN HEMTs under fast cyclic transient stress," *IEEE Trans. Device Mater. Rel.*, vol. 20, no. 3, pp. 562–569, Sep. 2020. [Online]. Available: https://doi.org/10.1109/TDMR.2020.3007128

[17] B. Shankar *et al.*, "On the trap assisted stress induced safe operating area limits of AlGaN/GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Burlingame, CA, USA, Mar. 2018, pp. 1–5. [Online]. Available: https://doi.org/10.1109/IRPS.2018.8353596

[18] W. Simburger, D. Johnsson, and M. Stecher, "High current TLP characterisation: An effective tool for the development of semiconductor devices and ESD protection solutions," in *Proc. ARMMS RF Microw. Soc.*, Nov. 2012, pp. 1–9.

[19] D. Bisi *et al.*, "Deep-level characterization in GaN HEMTs-part I: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013. [Online]. Available: https://doi.org/10.1109/TED.2013.2279021

[20] B. Shankar, A. Soni, H. Chandrasekar, S. Raghavan, and M. Shrivastava, "First observations on the trap-induced avalanche instability and safe operating area concerns in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3433–3440, Aug. 2019. [Online]. Available: https://doi.org/10.1109/TED.2019.2919491

[21] S. Dutta Gupta, V. Joshi, B. Shankar, S. Shikha, S. Raghavan, and M. Shrivastava, "UV-assisted probing of deep-level interface traps in GaN MISHEMTs and their role in threshold voltage & gate leakage instabilities," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, 2019, pp. 1–5. [Online]. Available: https://doi.org/10.1109/IRPS.2019.8720595

[22] V. Joshi, A. Soni, S. P. Tiwari, and M. Shrivastava, "A comprehensive computational modeling approach for AlGaN/GaN HEMTs," *IEEE Trans. Nanotechnol.*, vol. 15, no. 6, pp. 947–955, Nov. 2016. [Online]. Available: https://doi.org/10.1109/TNANO.2016.2615645

[23] V. Joshi, B. Shankar, S. P. Tiwari, and M. Shrivastava, "Dependence of avalanche breakdown on surface & buffer traps in AlGaN/GaN HEMTs," in *Proc. Int. Conf. Simulat. Semicond. Process. Devices (SISPAD)*, Kamakura, Japan, 2017, pp. 109–112.

[24] O. Aktas and I. C. Kizilyalli, "Avalanche capability of vertical GaN p-n junctions on bulk GaN substrates," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 890–892, Sep. 2015. [Online]. Available: https://doi.org/10.1109/LED.2015.2456914

[25] S. K. Gupta, B. Shankar, W. R. Taube, J. Singh, and J. Akhtar, "Capacitance–conductance spectroscopic investigation of interfacial oxide layer in Ni/4H–SiC (0 0 0 1) schottky diode," *Physica B, Condensed Matter*, vol. 434, pp. 44–50, Feb. 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0921452613006601

[26] B. Shankar *et al.*, "On the ESD behavior of AlGaN/GaN schottky diodes and trap assisted failure mechanism," in *Proc. 39th Elect. Overstress/Electrostat. Discharge Symp. (EOS/ESD)*, Tucson, AZ, USA, Sep. 2017, pp. 1–6.

[27] L. Fu *et al.*, "Field-dependent carrier trapping induced kink effect in AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 98, no. 17, 2011, Art. no. 173508. [Online]. Available: https://doi.org/10.1063/1.3584861

[28] B. Shankar and M. Shrivastava, "Safe operating area of polarization super-junction GaN HEMTs and diodes," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4140–4147, Oct. 2019. [Online]. Available: https://doi.org/10.1109/TED.2019.2933362

[29] M. Kuball, M. Tapajna, R. J. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes," *Microelectron. Rel.*, vol. 51, no. 2, pp. 195–200, 2011, [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271410004786

Authorized licensed use limited to: J.R.D. Tata Memorial Library Indian Institute of Science Bengaluru. Downloaded on October 04,2022 at 05:13:45 UTC from IEEE Xplore. Restrictions apply.