Interplay Between Surface and Buffer Traps in Governing Breakdown Characteristics of AlGaN/GaN HEMTs—Part II

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***Abstract*— Physical insights into the complex interplay of surface and (GaN) buffer traps governing breakdown characteristics of AlGaN/GaN HEMTs are developed by well-calibrated TCAD simulations. Impact of surface traps in correlation with 1) acceptor traps in case of Fe doping and 2) self-compensating traps (corresponding to C doping) in the GaN buffer on breakdown characteristics of AlGaN/GaN HEMTs is discussed. The explorations include defect-related traps as well as traps induced by intentional buffer doping by carbon/iron. The computational findings corroborate well with the experimentally observed electric field profile for devices with different buffer doping conditions. Developed insights have allowed to discuss the collective impact of surface as well as buffer traps on device design to improve breakdown characteristics.**

***Index Terms*— AlGaN/GaN HEMTs, buffer traps, carbon doping, device breakdown, electric field engineering, surface traps.**

I. Introduction

INCREASED focus on development of AlGaN/GaN HEMT technology on a Si substrate has made GaN buffer designing one of the most challenging tasks and therefore, a topic of research interest for several groups [1]–[7]. The root cause is high lattice and thermal mismatch between Si and GaN, which lead to dislocations/defects-induced traps in GaN buffer, leading to buffer trap-related reliability issues [2]–[4], [6], [7]. Besides, the GaN buffer, being unintentionally n-type doped, is often doped with carbon or iron to reduce leakage and improve breakdown voltage (V_{BD}) [8]–[10]. These dopants are well known to induce acceptor-type traps in the GaN buffer [3], [7] making buffer designing a challenging task. While buffer engineering is a widely accepted technique for improving V_{BD}, in this work we have suggested strong interplay of surface and buffer traps in governing the breakdown characteristics of the AlGaN/GaN HEMTs. This is in corroboration with experimental work by Tanabe *et al.* [11], which hinted surface morphology and carbon doping to be correlated in determining V_{BD} of AlGaN/GaN HEMT device. While previous works have attempted to model the role of buffer traps on electric field distribution, vertical leakage, or breakdown characteristics [9], [10], [12], [13], interplay of surface traps was not studied earlier. For example, an elaborate study done by Uren *et al.* [13] though gives detailed insight into the electric field distribution, however, was limited to isolated impact of buffer traps. Similarly, while Joshi *et al.* [9], [10] discussed the impact of carbon doping-induced traps in GaN buffer on vertical electric field and V_{BD} of the device, its impact on correlation with surface traps was not explored. In general, physical mechanism governing breakdown characteristics of the device involving interplay of surface and buffer traps is less explored and not well understood. Given this gap in earlier works and keeping in mind the recent studies suggesting interaction between surface and buffer properties governing device characteristics [2], [6], [12], it is of prime importance to develop physical insight into this unique interplay. Motivated by TCAD-based explorations in recent past unraveling unique physical phenomena in GaN-based devices [9], [14]–[17], this work uses a well-calibrated computational framework to address this gap in V_{BD} analysis of AlGaN/GaN HEMTs.

While part I of this work discussed the impact of surface traps on breakdown characteristics, this part presents an interplay of buffer traps and surface traps governing electrical breakdown of AlGaN/GaN HEMTs. Section II briefly explains the calibrated computational setup adopted from Part-I of this work for electrical breakdown analysis. Section III discloses and explains the surface-buffer interplay and its impact on electric field distribution and V_{BD} characteristics. Section IV discusses the impact of self-compensating traps in GaN buffer, resembling conditions of carbon doping, on V_{BD} of the device. Section V validates the developed physical insights using electro-luminescence (EL)-based electric field analysis on devices with different buffer conditions, confirming measured field profiles to be in complete agreement with the computational findings. Device design for achieving high V_{BD} in AlGaN/GaN HEMTs in the resence of buffer and surface traps is discussed in Section VI. Section VII concludes the work.

II. Device Structure and Simulation Setup

Fig. 1 shows the AlGaN/GaN HEMT structure used in this work. All the device parameters specified in Fig. 1 are used throughout this work unless stated otherwise.

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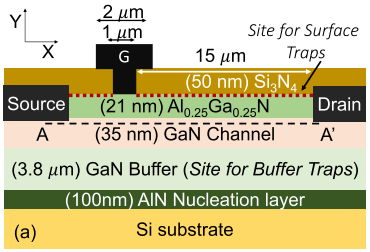

Fig. 1. Device schematic used for computational and experimental explorations in this work specifying the physical location of surface and buffer traps. AA' denotes the cut-line along which electric field plots discussed in this work are extracted. Here direction x is parallel to the flow of source–drain current.

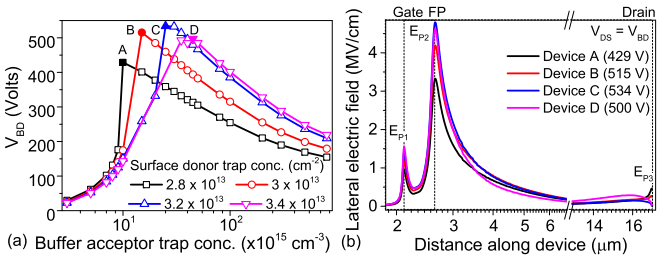

Fig. 2. (a) V_{BD} of the device as a function of acceptor-type traps in GaN buffer extracted for different surface donor trap concentrations. (b) Channel lateral electric field (x-direction) extracted at the onset of breakdown for devices with maximum V_{BD} [devices A, B, C, and D in (a)]. Electric field is extracted along cut-line AA' shown in Fig. 1.

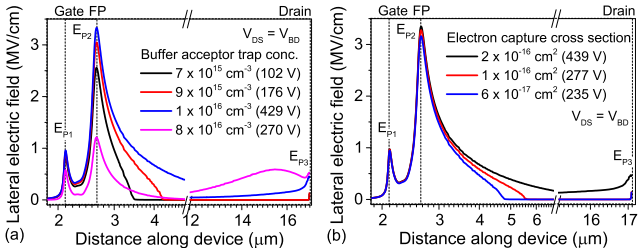

Fig. 3. Lateral electric field extracted at the onset of breakdown (a) for devices with different buffer acceptor trap concentrations and a surface donor trap concentration of 2.8 × 10^{13} cm^{-2} and (b) as a function of electron capture cross section of buffer acceptor traps. Electron capture cross section modulates the trapping probability of electrons generated due to impact ionization near the FP edge and hence, affects the V_{BD}.

The computational framework used in this work is adopted from our earlier works in [9], [10], and [18] and is discussed in detail in Part I of this work. Drift diffusion transport and high field-induced mobility degradation are considered to account for carrier dynamics in 2-D electron gas (2DEG). Source/drain Ohmic contacts are modeled as Schottky contact with lower work function and high n-type doping at the contact/GaN interface [18]. Impact ionization is taken into account according to the Chynoweth law [19] with critical field for GaN set as ∼3 MV/cm [9]. Donor-type traps are considered on the device surface with an activation energy of $E_C - 0.68$ eV [20]. Acceptor-type traps are considered in the GaN buffer with activation energy of $E_C - 0.96$ eV, which is associated with dislocations in GaN buffer [20]. As discussed in Part I of this work, the results obtained with the computational framework were in excellent agreement with the experimentally reported V_{BD} as well as leakage current. OFF-state V_{BD} of the device was evaluated at a drain current of 1 μA/mm. Further, as discussed in Part I of this work, gate-stack has no impact on channel field modulation by trap-induced charges on the device surface. Hence, Schottky-gated devices were considered for simplicity. However, it should be noted that the observations and results discussed here are also applicable to MIS-gated devices.

For experimental determination of impact of buffer quality on electric field distribution, devices were fabricated on two different GaN buffers. Both the stacks have SiN_X as surface passivating layer on AlGaN barrier ensuring surface conditions to be similar. Fabrication on the two buffers was carried out in a single run using a well-established fabrication technology demonstrated in our earlier work [21]. This ensures minimal variability across devices on the two buffers, ensuring any changes in the measured electric field to be caused by buffer conditions only.

III. Interplay of Surface Traps and Acceptor Only Buffer Traps

This section considers impact of traps present in GaN buffer, in correlation with surface traps, on V_{BD} of the device. As acceptor-type traps are known to be present in GaN buffer to make it semiinsulating, acceptor-type traps are discussed first.

A. Implications on V_{BD}

Fig. 2(a) shows the V_{BD} of the device as a function of buffer acceptor trap concentration for different surface donor trap concentrations. As seen in Fig. 2(a), V_{BD} initially increases when acceptor trap concentration in the buffer region was increased, however, after reaching a peak value it reduces gradually as the trap concentration is increased further. Interestingly, the buffer acceptor trap concentration for which peak V_{BD} is observed as well as the value of peak V_{BD} depends on surface donor trap concentration. Initially, the peak V_{BD} increases when surface trap concentration was increased; however, a further increase in surface trap concentration lowers the peak V_{BD} value. These observations highlight a strong interplay between surface and buffer conditions while governing V_{BD} of the device.

To further probe into the observed breakdown characteristics, electric field profile for devices with maximum V_{BD}, marked as A, B, C, and D in Fig. 2(a), is compared in Fig. 2(b). The electric field profile shows three distinct peaks, near the gate edge (E_{P1}), near the field plate (FP) edge (E_{P2}), and near the drain edge (E_{P3}). The lateral electric field profile reveals a higher electric field peak near FP edge (even higher than critical GaN field ($E_{C,GaN}$) of ∼3 MV/cm) for devices showing higher V_{BD}. This establishes that breakdown is observed in these devices for field values much higher than the $E_{C,GaN}$ and it further increases as buffer acceptor trap concentration is increased. To analyze any impact of buffer acceptor traps on channel electric field and to isolate the impact of buffer traps, Fig. 3(a) compares the lateral field profile for devices with similar surface donor trap concentration. The impact of increase in buffer acceptor trap concentration on field profile depicts three different components: 1) devices show breakdown at a higher field value near the gate/FP edge (a higher value of E_{P1} and E_{P2} at $V_{DS} = B_{BD}$); 2) the electric field spreads to a larger length in access region; and

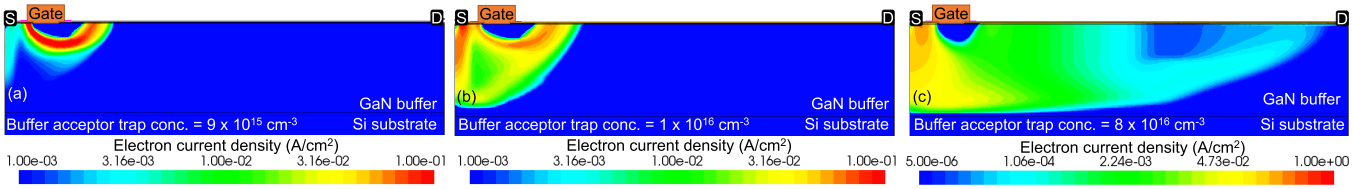

Fig. 4. Leakage contours extracted at the onset of device breakdown for devices with buffer acceptor trap concentration of (a) 9×10^{15} cm^{-3}, (b) 1×10^{16} cm^{-3}, and (c) 8×10^{16} cm^{-3}. The contours indicate that as the buffer acceptor trap concentration is increased, the leakage path shifts from the gate edge to the drain edge. A surface donor trap concentration of 2.8×10^{13} cm^{-2} was considered.

3) a secondary peak is formed near the drain edge for much higher buffer acceptor trap concentrations. These aspects are discussed as follows.

B. Limiting Impact Ionization

The observed breakdown at higher peak field value near the FP edge with increase in buffer acceptor trap concentration can be explained by considering trapping of impact ionization generated electrons in the buffer traps. Electron trapping inhibits further multiplication and impact ionization, thereby preventing device failure. To modulate the electron trapping probability, electron capture cross section for buffer traps was varied. The resulting field profile at the onset of breakdown, shown in Fig. 3(b), shows a reduction in V_{BD} and breakdown field value near the FP edge as the electron capture cross section is reduced. A reduced electron capture cross section lowers the electron trapping probability by the buffer acceptors, thereby allowing impact ionization generated electrons to multiply even at lower field values. Above observations clearly indicate that the presence of acceptor traps in GaN buffer significantly affects the impact ionization multiplication factor thereby modulating V_{BD}.

This explains the observed increase in V_{BD} with buffer acceptor trap concentration. However, the observed reduction in V_{BD} as buffer acceptor trap concentration is increased to even higher values, as seen in Fig. 2(a), suggests the presence of an additional phenomenon governing breakdown characteristics of the device.

C. Impact on Channel Depletion and Lateral Electric Field

Fig. 3(a) also suggested an impact of buffer acceptor trap concentration on channel electric field distribution. For lower buffer acceptor trap concentration, a higher magnitude of E_{P1} and E_{P2} is observed at the onset of breakdown. This suggests that the breakdown hotspot to be near the gate/FP edge. An increase in buffer acceptor trap concentration leads to relaxation in magnitude of E_{P1} and E_{P2} while E_{P3} considerably increases. Hence, with further increase in buffer acceptor trap concentration, E_{P3} increases in magnitude suggesting a shift in breakdown hotspot from gate edge to drain edge. With further increase in buffer acceptor trap concentration, V_{BD} starts reducing. The shift in breakdown hotspot from gate edge to drain edge is further evident from Fig. 4. It indicates that the buffer leakage path is located near the gate/FP edge for lower buffer acceptor trap concentration [Fig. 4(a) and (b)] and shifts near the drain edge for higher buffer acceptor trap concentration [Fig. 4(c)], suggesting a shift in breakdown

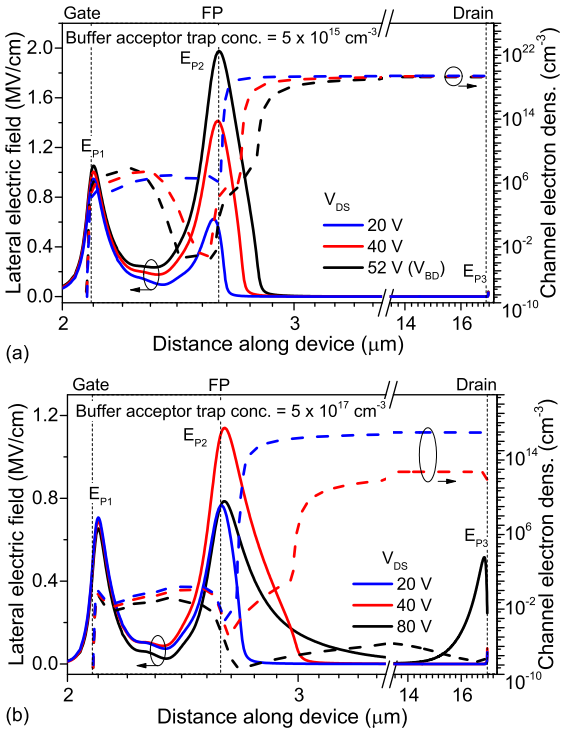

Fig. 5. Channel electric field and electron density extracted for buffer acceptor trap concentration of (a) 7×10^{15} cm^{-3} and (b) 8×10^{16} cm^{-3}. It shows the dependence of lateral electric field on buffer acceptor trap concentration to be driven by trap induced channel depletion modulation.

hotspot from gate edge to drain edge. It is worth mentioning here that as the breakdown hotspot shifts to drain edge, Fig. 3(a) illustrates that the breakdown happens for much lower lateral field values near drain edge. This is attributed to combined action of vertical and lateral electric field near drain edge leading to device breakdown. The impact of vertical field on device breakdown near the drain edge is considered in detail in our earlier work [9]. It was noted in [9] that buffer trap-induced space charge modulation affects vertical field distribution near drain edge and becomes important only when field extends up to drain edge.

To further probe into the influence of buffer acceptor traps on lateral electric field, the field profile was evaluated as a function of channel depletion and drain stress voltage. Fig. 5(a) and (b) compare channel electric field and electron density distribution for two different buffer acceptor trap concentrations. Fig. 5(a) shows the electric field to be confined in the proximity of the gate/FP electrode with negligible redistribution in the drain-gate access region. This directly correlates with the channel depletion being confined near the gate electrode [Fig. 5(a)]. On the other hand, for devices with

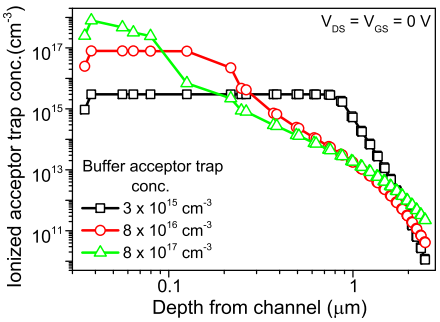

Fig. 6. Ionized acceptor trap concentration extracted under thermal equilibrium condition with grounded terminals. It indicates a higher ionization rate in the proximity of GaN channel. A surface donor trap concentration of 3.2×10^{13} cm^{-2} was considered.

relatively higher buffer acceptor trap concentration, Fig. 5(b) shows the channel depletion to be extended up to the drain edge for similar stress conditions. This leads to an increased field redistribution in the access region. Fig. 5(a) and (b) establish that the buffer acceptor trap concentration affects channel depletion at a particular drain bias and as a result affects the channel electric field.

The observed impact of acceptor traps in the GaN buffer on channel depletion can be explained by considering the charges presented by ionized buffer acceptor traps. Fig. 6 depicts the vertical ionized buffer acceptor trap profile in initial rest condition. The figure suggests an increase in ionized trap density in proximity of the channel as the buffer acceptor trap concentration is increased. On the other hand, the depth up to which buffer traps are ionized reduces as the buffer acceptor trap concentration is increased. This fact ensures that the net negative charge presented by ionized buffer acceptor traps remains approximately similar while the ionized trap concentration near the channel increases as buffer acceptor trap concentration is increased. This ensures approximately similar n_S in all the cases. However, increase in negative charge near the GaN channel results in an electric field directed toward the device surface. This field works opposite to the field due to polarization charges and hence, reduces the channel confinement. This results in a reduced field requirement for depleting the channel and hence, a larger depletion width is observed for similar V_{DS} with higher buffer acceptor trap concentration. The volume charge presented by buffer region with traps will have a lateral field component acting on the channel as well. Channel depletion profiles, shown in Fig. 5, suggest that this lateral field due to ionized buffer acceptor traps assists drain field in depleting the channel. This explains the channel field modulation due to acceptor traps present in the GaN buffer and resulting V_{BD} modulation.

D. Interplay of Acceptor-Type Buffer Traps and Donor-Type Surface Traps

Fig. 2(a) showed that peak V_{BD} was observed at a higher buffer acceptor trap concentration as the surface donor trap concentration was increased, suggesting an interplay between impact on channel depletion by surface donor and buffer acceptor traps. This effect can be explained by considering the combined impact of surface and buffer traps on channel depletion. As discussed in previous section, an increase in ionized buffer acceptor traps results in a larger depletion width for similar V_{DS}. On the other hand, as discussed in part I of this work, an increase in ionized surface donor trap concentration results in a shorter depletion width for similar V_{DS}. Surface donor traps and buffer acceptor traps thus have an opposite impact on channel depletion at a given V_{DS}. This implies that for a higher surface donor trap concentration a higher buffer acceptor trap concentration will be required to increase the depletion width to the desired value for similar V_{DS}. Considering the observations from Fig. 3 and the related discussion, peak V_{BD} point in Fig. 2(a) marks a shift in breakdown hotspot from gate edge to drain edge for a given drain bias. The point thus shifts toward right as surface donor trap concentration is increased owing to a higher buffer acceptor trap concentration now required to extend depletion region up to the drain edge. This establishes a strong correlation between surface and buffer design.

IV. Interplay of Surface Traps and Self-Compensating Buffer Traps

Apart from acceptor traps, carbon doping introduces self-compensating traps in GaN buffer [7], [9]. This trap profile results in both acceptor and donor traps being present simultaneously in the GaN buffer.

A. Impact on V_{BD}

Fig. 7(a)–(d) depict the impact of acceptor traps in the presence of a background donor trap concentration in the GaN buffer on V_{BD} of the device for different surface donor trap concentrations. Fig. 7(a) shows that irrespective of buffer donor trap concentration, V_{BD} of the device shows similar dependence on buffer acceptor trap concentration, as seen in previous section. However, with increase in buffer donor trap concentration, the curve and V_{BD} peak shift toward higher acceptor trap concentration. Moreover, as the buffer donor trap concentration is increased beyond a particular threshold value, the peak V_{BD} improves significantly. Further, Fig. 7(a)–(d) show an increase in peak V_{BD} with right shift in the position of peak V_{BD} when surface donor trap concentration is increased. This further confirms a strong interplay in buffer and surface trap configuration while defining V_{BD}.

B. Trap Induced Electric Field Modulation

Fig. 7 showed an improvement in V_{BD} at higher acceptor trap concentrations and improvement in peak V_{BD} with an increase in buffer donor trap concentration and surface donor trap concentration. This behavior can be explained by space charge modulation-induced vertical field relaxation near the drain edge, discussed in detail in our earlier work [9].

The right shift in the breakdown characteristics with an increase in buffer donor trap concentration can be explained by considering the lateral electric field profile. As shown in Fig. 8(a), as buffer donor trap concentration is increased for a given buffer acceptor trap concentration, lateral electric field becomes increasingly confined near the FP edge. This leads to an increase in magnitude of E_{P2} while E_{P3} reduces in magnitude. This behavior is opposite to the impact of buffer acceptor traps on lateral electric field and can be considered as

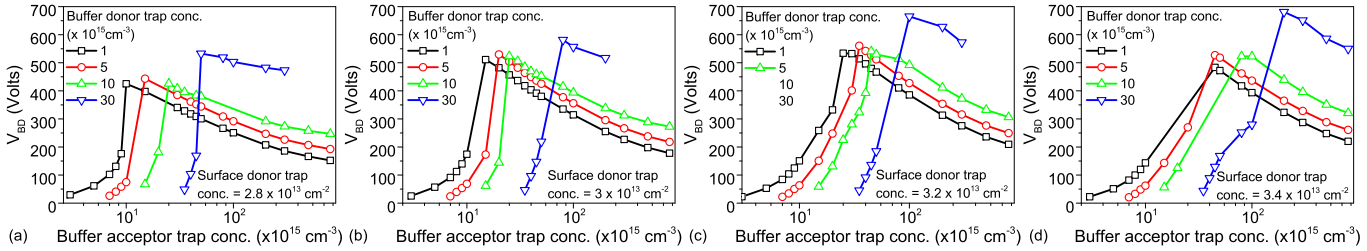

Fig. 7. V_{BD} of the device extracted as a function of buffer acceptor and donor trap concentration for a surface donor trap concentration of (a) 2.8×10^{13} cm^{-2}, (b) 3×10^{13} cm^{-2}, (c) 3.2×10^{13} cm^{-2}, and (d) 3.4×10^{13} cm^{-2}. Buffer donor traps were considered to be shallow donors ($E_C - 0.11$ eV) [9].

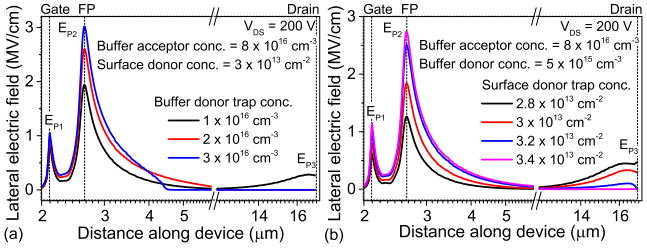

Fig. 8. (a) Lateral electric field extracted for devices with (a) different buffer donor trap concentration for a fixed buffer acceptor and surface donor trap concentration and (b) different surface donor trap concentrations with a compensating trap configuration in the GaN buffer.

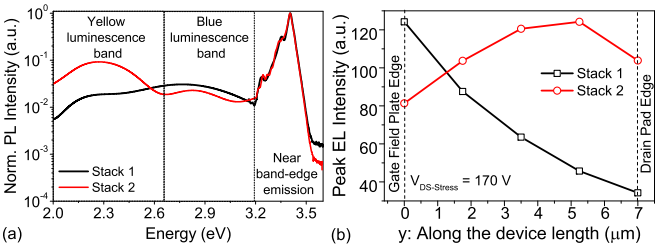

Fig. 9. (a) PL intensity comparison of two different buffer stacks used for fabrication of devices with identical surface conditions depicting Stack 2 to have higher buffer trap concentration. (b) EL intensity extracted in the gate–drain access region for devices having similar surface conditions but different buffer stack conditions. The experimentally obtained EL line scans are in complete agreement with the proposed model.

reduction in the effective buffer acceptor trap concentration. This results in a right shift in the breakdown characteristics with an increase in donor trap concentration in the GaN buffer, as seen in Fig. 7(a)–(d).

A similar increase in peak V_{BD} and right shift is observed with an increase in surface donor trap concentration as well. As discussed in previous section, surface donor trap concentration has an effect on channel depletion and electric field that is opposite to that of buffer acceptor traps. This is further verified by the lateral electric field profile extracted for different surface donor trap concentrations, as shown in Fig. 8(b). It shows an increase in magnitude of E_{P1} and E_{P2} as surface donor trap concentration is increased for a given buffer trap configuration. It should be noted that both surface and buffer donor traps oppose the effect of buffer acceptor traps on channel electric field. As a result, a right shift in breakdown characteristics is observed as surface or buffer donor trap concentration is increased [Fig. 7(a)–(d)].

V. Experimental Validation

To validate the observed impact of buffer acceptor traps on electric field and V_{BD}, EL line scans were employed to estimate depletion width in devices having similar surface conditions but different buffer stacks (Stack 1 and Stack 2), as discussed in Section II. To compare trap conditions in both the stacks, photo-luminescence (PL) spectra of both the stacks were extracted and are shown in Fig. 9(a). Two distinct features can be observed from the figure: 1) Stack 2 has a dominant yellow luminescence (YL) band with one order higher intensity than that in Stack 1, and, 2) The intensity ratio of the blue luminescence (BL) peak to that of the YL peak (I_{BL}/I_{YL}) is lower for Stack 2 (∼0.25) as compared to that of Stack 1 (∼1.88). These features indicate that Stack 2 has higher carbon concentration ($C_{[C]}$) in the GaN buffer compared to Stack 1, based on the fact that there is a strong correlation between $C_{[C]}$ and I_{BL}/I_{YL} [22]. Since, carbon doping is known to induce self-compensating traps in GaN buffer with a higher concentration of acceptor traps, Stack 2 will have a higher acceptor trap concentration in the GaN buffer compared to Stack 1.

Fig. 9(b) compares EL line scans for devices fabricated on Stack 1 and Stack 2 extracted at similar drain stress voltage. It shows EL intensity to be confined in a narrow region near the FP edge with negligible EL intensity near the drain edge for devices fabricated on Stack 1 having lower C_C (lower buffer acceptor trap concentration). On the other hand, EL line scan for devices fabricated on Stack 2 having higher C_C (higher buffer acceptor trap concentration) shows a rather uniform distribution of EL intensity in the gate–drain access region with a peak near the drain edge as well. Since, devices fabricated on Stack 2 have higher buffer acceptor trap concentration, depletion region extends up to the drain edge at lower drain stress voltages thereby resulting in a uniform EL profile with peak at the drain edge. On the other hand, given similar surface conditions, devices fabricated on Stack 1 have a lower buffer acceptor trap concentration resulting in a confinement of depletion region near the FP edge at similar drain stress voltage. These observations are in complete agreement with the computational findings.

VI. Device Design in the Presence of Traps

A. Drift Region Engineering in the Presence of Traps

Fig. 10 shows impact of acceptor traps in GaN buffer on device design with respect to gate–drain length (L_{GD}) and gate connected FP length L_{FP} for a constant surface donor trap concentration. The surface donor trap concentration is taken such that the electric field peak for lower buffer acceptor

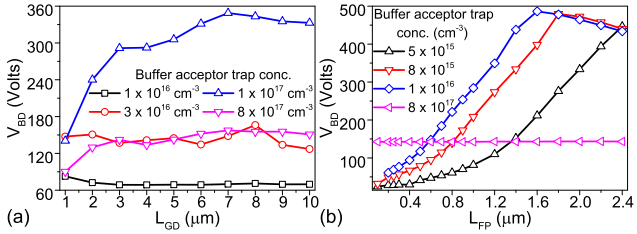

Fig. 10. Impact of device scaling on breakdown voltage of the device extracted as a function of buffer acceptor trap concentration. (a) Denotes scaling with respect to L_{GD} for a constant L_{FP} of 250 nm and (b) denotes scaling with respect to L_{FP} for an L_{GD} of 5 μm. Surface and buffer donor trap concentrations of 3.2×10^{13} cm^{-2} and 1×10^{15} cm^{-3}, respectively, were considered for these calculations.

trap concentrations is located near the gate/FP edge, which is expected to redistribute in the access region with a peak near drain edge as buffer acceptor trap concentration is increased. Since the surface and buffer donor trap concentration affected the absolute V_{BD} and had negligible impact on dependence of V_{BD} on buffer acceptor traps (Fig. 7), a constant surface and buffer donor trap concentration was assumed here.

Fig. 10(a) shows an improvement in V_{BD} as L_{GD} is increased for moderate buffer acceptor trap concentration. On the other hand, V_{BD} shows negligible dependence on L_{GD} for low as well as high buffer acceptor trap concentrations. A similar dependence of V_{BD} scaling with L_{GD} on carbon doping concentration was observed experimentally in [8], wherein V_{BD} improved with an increase in L_{GD} as carbon doping concentration was increased. As carbon doping induces traps in GaN buffer, it can be considered as an increase in trap concentration in GaN buffer. The behavior observed in Fig. 10 can be explained with the help of channel electric field. Fig. 11(a) compares channel electric field at the onset of breakdown for devices with lower and moderate buffer acceptor trap concentrations. While for both the trap concentrations breakdown is determined by E_{P2}, devices with lower trap concentration show field confinement near FP edge leading to earlier device breakdown. On the other hand, devices with moderate trap concentration showed an improved field redistribution in the access region leading to improvement in V_{BD} with an increase in L_{GD}. For higher buffer acceptor trap concentration confinement of electric field near drain edge is observed, as shown in Fig. 11(b). This again leads to negligible improvement in V_{BD} as L_{GD} is increased.

On the other hand, an improvement in V_{BD} with an increase in L_{FP} is observed for devices with lower buffer acceptor trap concentration, as shown in Fig. 10(b). However, for devices with higher buffer acceptor trap concentration, V_{BD} is independent of L_{FP}. This behavior can again be explained by a comparison of channel electric field profile for devices with lower and higher buffer acceptor trap concentrations, shown in Fig. 12(a) and (b), respectively. Fig. 12(a) shows a significant magnitude of E_{P1} with negligible magnitude of E_{P3}. The breakdown in this case is thus controlled by E_{P1}. As L_{FP} significantly relaxes E_{P1}, shown in Fig. 12(a), breakdown voltage improves as L_{FP} is increased. On the other hand, Fig. 12(b) shows a higher magnitude of E_{P3} for devices with higher buffer acceptor trap concentration. This indicates breakdown hotspot to be located near the drain edge. As FP

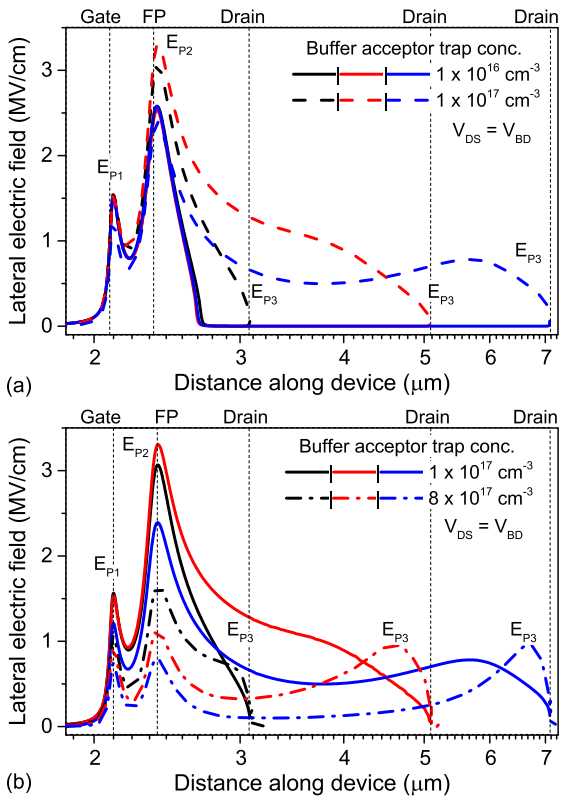

Fig. 11. Lateral channel electric field profile extracted for devices with different L_{GD} values for (a) lower and moderate buffer acceptor trap concentrations and (b) moderate and high buffer acceptor trap concentrations.

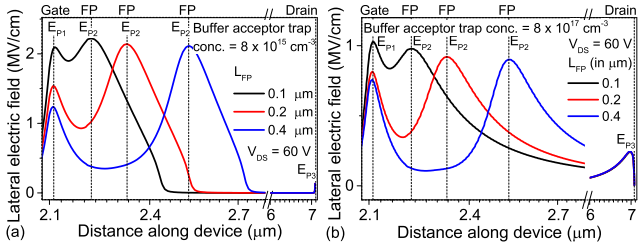

Fig. 12. Lateral channel electric field extracted as a function of L_{FP} for buffer acceptor trap concentration of (a) 8×10^{15} cm^{-3} and (b) 8×10^{17} cm^{-3}.

relaxes E_{P1} and has negligible impact on E_{P3}, the breakdown voltage does not show any dependence on L_{FP}. The electric field modulation by acceptor-type buffer traps is attributed to channel depletion modulation by negatively ionized buffer acceptor traps as discussed in Section III-C.

B. Trap Aware Device Design

This work has established that traps on device surface and in GaN buffer significantly affect electric field distribution and V_{BD} of the device. In our earlier work in [10], a method to independently engineer acceptor and donor traps in GaN buffer was proposed using codoping of GaN buffer by carbon and silicon. Further, in part I of this work, surface passivation by a p-type oxide proved to be an effective method in engineering surface traps. These methods combined give us an effective tool to independently engineer surface traps as well as acceptor and donor traps in GaN buffer. Fig. 13 shows the collective

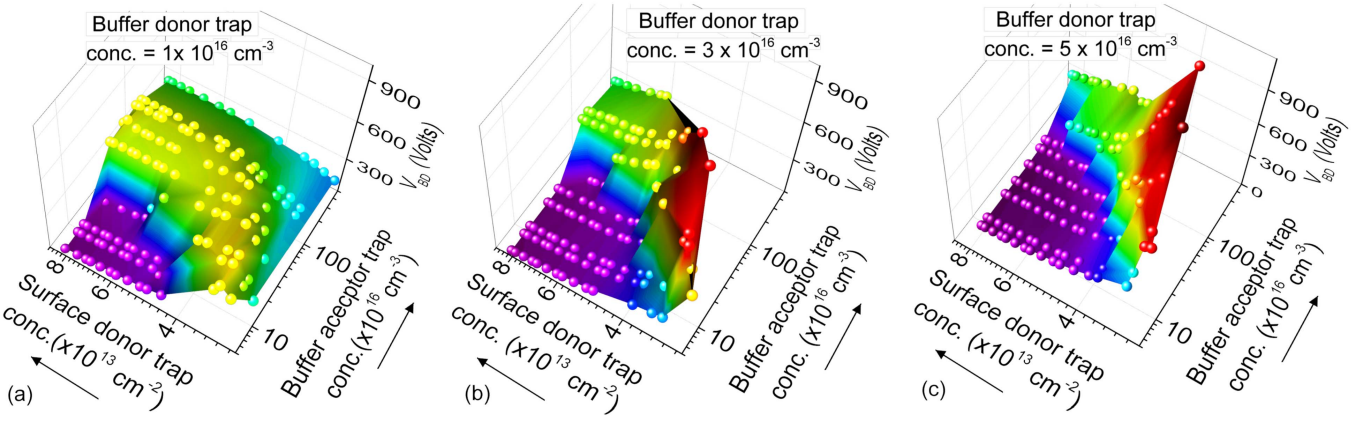

Fig. 13. Breakdown voltage as a function of surface donor and buffer acceptor trap concentrations for a buffer donor trap concentration of (a) 1×10^{16} cm^{-3}, (b) 3×10^{16} cm^{-3}, and (c) 5×10^{16} cm^{-3}. The figure shows buffer and surface properties to be correlated in defining breakdown voltage of the device.

impact of surface donor traps in the presence of buffer acceptor traps for three different buffer donor trap concentrations. Fig. 13(a) shows that for lower buffer acceptor trap concentration, there exists a narrow range of surface donor trap concentration values where maximum V_{BD} can be achieved. On the other hand, as buffer acceptor trap concentration is increased, the device shows capability to tolerate surface donor trap concentration for a larger range of values. However, as the buffer acceptor trap concentration is increased to much higher values, the V_{BD} starts reducing but is less dependent on surface donor trap concentration. Further, Fig. 13(b) shows that for higher buffer donor trap concentration, the peak V_{BD}, which can be achieved, significantly improves. The reason behind this improvement in peak V_{BD} with buffer donor trap concentration is attributed to improved voltage handling capability of GaN buffer due to vertical field relaxation and is discussed in detail in our earlier work [9]. However, it is worth mentioning here that for improved voltage withstanding capability of GaN buffer, the device shows reduced tolerance to surface trap concentration or surface quality. In these cases, the V_{BD} reduces drastically at much lower surface trap concentrations as compared to the devices with lower buffer donor trap concentration shown in Fig. 13(a). As the buffer donor trap concentration is further increased [Fig. 13(c)], the design window becomes even narrower and V_{BD} starts falling for even lower surface donor trap concentration for a given buffer acceptor trap concentration.

Results in Fig. 13 suggest a higher buffer trap concentration to be beneficial for maximizing breakdown voltage. However, it is worth highlighting here that traps in GaN buffer and device surface are known to contribute to the degradation of other performance figure of merit parameters like dc-RF dispersion. Therefore, the upper side of the trap concentration must be cooptimized while keeping in mind the other performance figure of merit parameters.

VII. Conclusion

Using a well-calibrated computational framework, impact of traps in GaN buffer on the breakdown characteristics of AlGaN/GaN HEMTs is discussed in correlation with traps on device surface. Traps in the GaN buffer were found to affect channel depletion and hence, the channel electric field. Experimentally extracted electric field profile validated dependence of channel electric field on buffer conditions. Device design guidelines extracted under the influence of surface and buffer traps reveal an optimum moderate buffer acceptor trap concentration for maximizing the breakdown voltage as a function of gate–drain distance and FP length. Above this optimum range, breakdown voltage becomes insensitive to gate–drain distance or FP length. These findings establish the surface and buffer design to be correlated in defining channel electric field profile and V_{BD} of AlGaN/GaN HEMTs. While a GaN buffer with lower voltage handling capacity offers larger design window for surface engineering, it offers a lower peak V_{BD}. On the other hand, increasing voltage handling capability of GaN buffer by increasing donor trap concentration in the GaN buffer results in devices susceptible to surface quality and very narrow window for surface engineering.

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References

[1] D. Bisi *et al.*, "Hot-electron degradation of AlGaN/GaN high-electron mobility transistors during RF operation: Correlation with GaN buffer design," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1011–1014, Oct. 2015, doi: 10.1109/LED.2015.2474116.

[2] Y. Saito, R. Tsurumaki, N. Noda, and K. Horio, "Analysis of reduction in lag phenomena and current collapse in field-plate AlGaN/GaN HEMTs with high acceptor density in a buffer layer," *IEEE Trans. Device Mater. Rel.*, vol. 18, no. 1, pp. 46–53, Mar. 2018, doi: 10.1109/TDMR.2017.2779429.

[3] G. Verzellesi *et al.*, "Influence of buffer carbon doping on pulse and AC behavior of insulated-gate field-plated power AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 443–445, Apr. 2014, doi: 10.1109/LED.2014.2304680.

[4] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng, and K. J. Chen, "Impact of substrate bias polarity on buffer-related current collapse in AlGaN/GaN-on-Si power devices," *IEEE Trans. Electron Devices*, vol. 64, no. 12, pp. 5048–5056, Dec. 2017, doi: 10.1109/TED.2017.2764527.

[5] M. Tao *et al.*, "Buffer-induced time-dependent OFF-state leakage in AlGaN/GaN high electron mobility transistors on silicon," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4860–4864, Dec. 2016, doi: 10.1109/TED.2016.2614332.

[6] W. M. Waller *et al.*, "Control of buffer-induced current collapse in AlGaN/GaN HEMTs using SiNx deposition," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4044–4049, Oct. 2017, doi: 10.1109/TED.2017.2738669.

[7] M. J. Uren *et al.*, "'Leaky dielectric' model for the suppression of dynamic R_{ON} in carbon-doped AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2826–2834, Jul. 2017, doi: 10.1109/TED.2017.2706090.

[8] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Wurfl, and G. Trankle, "AlGaN/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1 kV and low $R_{ON} \times A$," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 3050–3058, Nov. 2010, doi: 10.1109/TED.2010.2069566.

[9] V. Joshi, S. P. Tiwari, and M. Shrivastava, "Part I: Physical insight into carbon-doping-induced delayed avalanche action in GaN buffer in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 561–569, Jan. 2019, doi: 10.1109/TED.2018.2878770.

[10] V. Joshi, S. P. Tiwari, and M. Shrivastava, "Part II: Proposals to independently engineer donor and acceptor trap concentrations in GaN buffer for ultrahigh breakdown AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 570–577, Jan. 2019, doi: 10.1109/TED.2018.2878787.

[11] S. Tanabe, N. Watanabe, M. Uchida, and H. Matsuzaki, "Effects of surface morphology and c concentration in C-doped GaN buffer on breakdown voltage of AlGaN/GaN HEMTs on free-standing GaN substrate," *Phys. Status Solidi (A)*, vol. 213, no. 5, pp. 1236–1240, May 2016. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/pssa.201532781, doi: 10.1002/pssa.201532781.

[12] T. Kabemura, S. Ueda, Y. Kawada, and K. Horio, "Enhancement of breakdown voltage in AlGaN/GaN HEMTs: Field plate plus high-k passivation layer and high acceptor density in buffer layer," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3848–3854, Sep. 2018, doi: 10.1109/TED.2018.2857774.

[13] M. J. Uren, M. Caesar, S. Karboyan, P. Moens, P. Vanmeerbeek, and M. Kuball, "Electric field reduction in C-Doped AlGaN/GaN on Si high electron mobility transistors," *IEEE Electron Device Lett.*, vol. 36, no. 8, pp. 826–828, Aug. 2015, doi: 10.1109/LED.2015.2442293.

[14] M. Borga *et al.*, "Modeling of the vertical leakage current in AlN/Si heterojunctions for GaN power applications," *IEEE Trans. Electron Devices*, vol. 67, no. 2, pp. 595–599, Feb. 2020, doi: 10.1109/TED.2020.2964060.

[15] J. Sun *et al.*, "Substantiation of buried two dimensional hole gas (2DHG) existence in GaN-on-Si epitaxial heterostructure," *Appl. Phys. Lett.*, vol. 110, no. 16, Apr. 2017, Art. no. 163506, doi: 10.1063/1.4980140.

[16] L. Sayadi *et al.*, "The role of silicon substrate on the leakage current through GaN-on-Si epitaxial layers," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 51–58, Jan. 2018, doi: 10.1109/TED.2017.2773670.

[17] D. Cornigli *et al.*, "Numerical investigation of the lateral and vertical leakage currents and breakdown regimes in GaN-on-silicon vertical structures," in *IEDM Tech. Dig.*, Dec. 2015, pp. 5.3.1–5.3.4, doi: 10.1109/IEDM.2015.7409633.

[18] V. Joshi, A. Soni, S. P. Tiwari, and M. Shrivastava, "A comprehensive computational modeling approach for AlGaN/GaN HEMTs," *IEEE Trans. Nanotechnol.*, vol. 15, no. 6, pp. 947–955, Nov. 2016, doi: 10.1109/TNANO.2016.2615645.

[19] A. G. Chynoweth, "Ionization rates for electrons and holes in silicon," *Phys. Rev.*, vol. 109, no. 5, pp. 1537–1540, Mar. 1958, doi: 10.1103/PhysRev.109.1537.

[20] D. Bisi *et al.*, "Deep-level characterization in GaN HEMTs–Part I: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013, doi: 10.1109/TED.2013.2279021.

[21] S. Dutta Gupta *et al.*, "Positive threshold voltage shift in AlGaN/GaN HEMTs and E-mode operation by Al_xTi_{1-x} o based gate stack engineering," *IEEE Trans. Electron Devices*, vol. 66, no. 6, pp. 2544–2550, Jun. 2019, doi: 10.1109/TED.2019.2908960.

[22] F. Liang *et al.*, "Role of Si and c impurities in yellow and blue luminescence of unintentionally and Si-doped GaN," *Nanomaterials*, vol. 8, no. 12, p. 1026, Dec. 2018, doi: 10.3390/nano8121026.