Unified Mechanism for Graphene FET's Electrothermal Breakdown and Its Implications on Safe Operating Limits

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***Abstract*— Unique electrothermal properties of graphene and the chemical nature of its degradation present a compelling set of conditions for the exploration of its breakdown at different time scales. In this work, we give a phenomenological description of graphene's electrical breakdown ranging from a nonequilibrium (transient) electrothermal state to far-equilibrium state while spanning a time scale from few nanoseconds to few minutes. The intricate roles of Pauli-blocked states, intraband heating, and mechanism of degradation in defining a safe operating area (SOA) have been explored. The time and field evolution of defects, resulting in defect-by-defect breakdown, have been studied using Raman spectroscopy. The unified mechanism of breakdown discussed here provides a basic understanding of reliability of graphene-based devices under high-current and/or high-field conditions as well as degradation due to its prolonged operation.**

***Index Terms*— Electrical overstress (EOS)/electrostatic discharge (ESD), electrothermal transport, graphene, safe operating area (SOA), time-dependent failure.**

I. Introduction

GRAPHENE is gradually entering into the design space of RF transistors [1], [2], interconnects [3], sensors, heat spreaders, and electrodes. The material shows various unique properties, including high mobility [4] and thermal conductivity [5] and gate-controlled conduction through the channel [6]. A practical deployment of graphene in various applications requires a comprehensive investigation of potential reliability issues. Unlike conventional semiconductors, which fail via electromigration, melting, or crack formation [7], a channel made of graphene, or 2-D materials in general, undergoes chemical breakdown. Such reactions are triggered by dissipation of excess heat of hot electrons to the lattice, with Arrhenius-like dependence of their rate on the lattice temperature and activation energy [8]. An out-of-equilibrium population of hot electrons dissipates their excess energy to the heat sink via a sequence of processes involving thermalization via carrier–carrier scattering and phonon emission [9], followed by formation of hot spot and diffusion of heat via acoustic phonons. The diffusion of heat results in three different states of electrothermal transport (see Fig. 1): 1) nonequilibrium; 2) near-equilibrium; and 3) far-equilibrium or steady state. A transition from nonequilibrium to near-equilibrium can be approximated by the characteristic thermal diffusion time of the device (t_{diff}). A comprehensive assessment of reliability of 2-D materials requires investigations from a transient state of electrothermal nonequilibrium to a state of far-equilibrium. For example, measurements performed during a transient state of electrothermal nonequilibrium ($t \leq t_{\text{diff}}$) can provide valuable insights into the effects of various electrostatic conditions on breakdown while suppressing the deleterious effects of self-heating. Similarly, the mechanism of degradation can be captured by studying the breakdown at various isothermal conditions, which require operation of the devices in steady or far-equilibrium state ($t \gg t_{\text{diff}}$). With a thermal diffusion time constant of tens of nanoseconds [10], the reliability assessment of a graphene-based transistor requires investigation of electrothermal transport from few nanoseconds to few seconds.

In this work, we give a phenomenological description of electrothermal breakdown of graphene channel at a time scale ranging from few nanoseconds to few seconds while considering operations at different Fermi levels, time evolution of oxidative breakdown, and efficiencies of pathways to the heat sinks. The discussion presented in this work not only provides an understanding of dynamics of breakdown at different time scales but also reveals the breakdown mechanisms under various reliability conditions. The time scales in the range of nanoseconds emulate high-field electrostatic discharge (ESD) and electrical overstress (EOS) events, while longer time

Manuscript received December 7, 2020; revised January 25, 2021 and March 3, 2021; accepted March 17, 2021. Date of publication April 1, 2021; date of current version April 22, 2021. This work was supported by Extramural Research & Intellectual Property Rights (ER & IPR), Defence Research and Development Organisation (DRDO). The review of this article was arranged by Editor F. Schwierz. *(Corresponding author: Abhishek Mishra.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3068081.

Digital Object Identifier 10.1109/TED.2021.3068081

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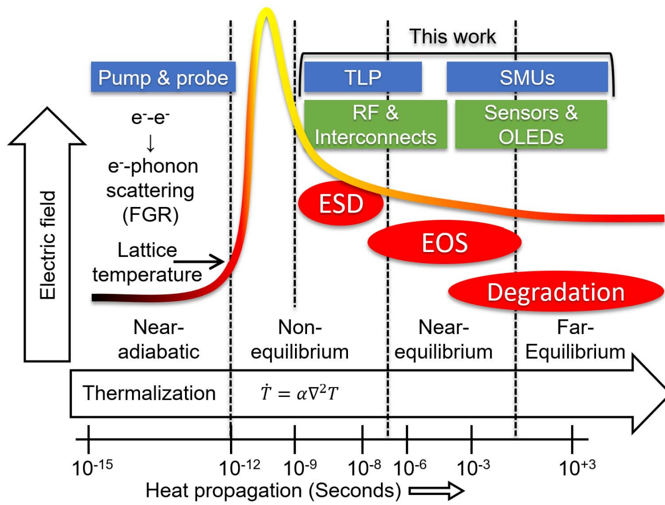

Fig. 1. Various transient states and associated reliability events discussed in this work, targeting different kinds of applications. The time scale of a particular state necessitates deployment of a specific measurement system. The phonon modes contributing to lattice heating are defined by FGR, while the time span of the nonequilibrium state is defined by thermal diffusivity (α).

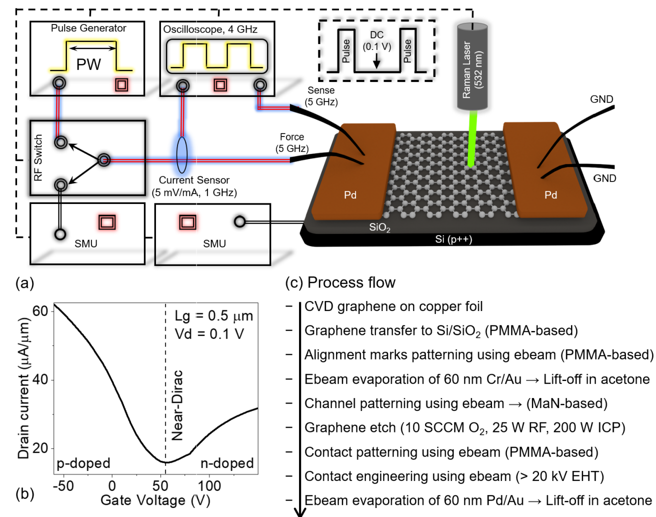

Fig. 2. (a) Electro-optical technique used to inflict controlled breakdown to a graphene channel while capturing their signatures through Raman spectroscopy and low-bias dc measurements. (b) Representative I_d–V_g characteristic of devices used for pulse measurements. (c) Process flow used to fabricate back-gated graphene-based devices.

scales (seconds) are used to study material degradation during prolonged operations at low electric fields. The results acquired from the analysis of temporal evolution of electrothermal transport are further used to gain insights into safe operating area (SOA) of graphene-based devices. Interestingly, the analysis of temporal evolution of electrothermal transport over a time scale from few nanoseconds to few seconds also covers a wide range of applications. A schematic depicting the temporal evolution of electrothermal transport, associated measurement techniques, time-dependent applications, and various reliability events is shown in Fig. 1. It is worth highlighting that the study of temporal evolution of electrothermal transport provides a complementary understanding to rich literature on high-field transport through graphene [10]–[18] and operational reliability of graphene transistors [19]–[25]. The rest of this article is organized as follows. Section II discusses the experimental techniques. The effects of various electrostatic conditions are explored in Section III. A discussion on isothermal heating is presented in Section IV. The effects of pathways to the heat sinks on breakdown are discussed in Section V. The unified mechanism of failure and SOA are discussed in Section VI. The overall work is concluded in Section VII.

II. Device Fabrication and Characterization

Devices used in the work were fabricated using a bottom-up approach. In brief, a monolayer of polycrystalline CVD-grown graphene [26] was first transferred on SiO_2/Si stack, followed by thermal annealing at 250 °C in ambient air for 20 min. The thermal annealing removes trapped water molecules and improves adhesion between graphene and the substrate. The channel and contact patterning were done using O_2 plasma and e-beam lithography. Before metallization of contacts, defects were deterministically introduced through controlled exposure to electron beam [27]. After metal deposition, the devices were annealed in Ar/H_2 ambient at 300 °C for 30 min. The detailed process flow and a representative characteristic of the devices are shown in Fig. 2. The pulse measurements have been performed on HfO_2 passivated devices, while unpassivated devices have been used to study the time degradation (constant voltage stress). The breakdown investigation begins with infliction of a series of defects by two different approaches: 1) time-dependent breakdown involves application of moderate fields for prolonged durations until a complete breakdown is achieved and 2) field-dependent breakdown involves application of high field for few nanoseconds and increasing the magnitude until breakdown. The low-bias (0.1 V) resistance of the device and evolution of defects are monitored using interpulse resistance measurements and Raman spectroscopy, respectively. In case of pulse measurements, a pulse-to-pulse delay of 200 ms has been used, during which the device cools down to ambient temperature and low-bias resistance is monitored. A rise time of 1 ns and single-shot rectangular pulses have been used to avoid the secondary effects that are generally associated with pulse measurements. Prior to measurements, the system is calibrated using standard passive resistors and Zener diodes. The current and voltage data points are acquired after averaging from 70% to 90% of the transient waveform. The dc transients have been acquired by running the source measurement units (SMUs) in sampling mode and monitoring the drain current at every 500 ms. A 532-nm laser with a spot size of around 700 nm has been used to perform the Raman spectroscopy. To avoid any unintentional damage to the material, the Raman maps have been acquired with reduced laser power and a slow scan of 4 s. All electrical and Raman measurements discussed in this work have been performed under ambient conditions. A schematic of the measurement system is shown in Fig. 2.

III. Intrinsic Heating of Graphene

The application of high electric fields across a graphene channel results in a substantial population of hot electrons,

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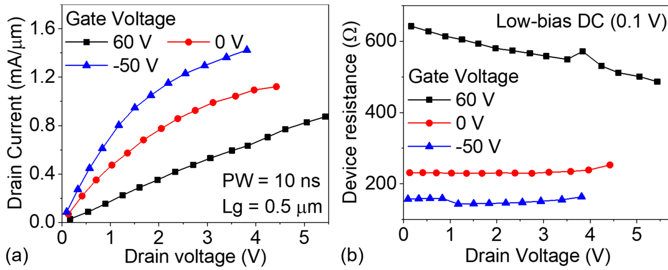

Fig. 3. (a) Pulse I–V characteristics capturing intrinsic heating while highlighting a linear response for $V_g = 60$ V and saturation for $V_g < 60$ V. The current and voltage data points have been acquired after averaging the respective transients from 70% to 90% of the pulse width. (b) Low-bias dc resistance shows a gradual decrease after every high-bias pulse for $V_g = 60$ V. The transistors operated at $V_g = 0$ and -50 V do not show any substantial changes in resistance, except a slight increase near prebreakdown region. All the devices showed abrupt permanent damage for the voltages higher than the maximum drain voltages shown here.

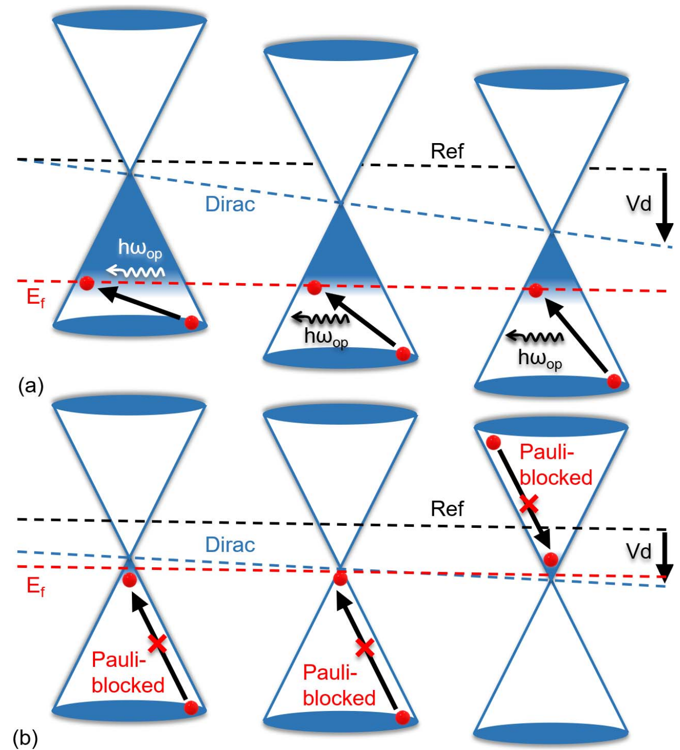

Fig. 4. Relaxation of hot electrons across a graphene channel. (a) Intraband heating in p-doped graphene via emission of phonons, resulting in current saturation. (b) Restricted intraband heating near the Dirac point. The vanishingly small density of states near the Dirac point prohibits the relaxation of hot electrons and fosters a linear rise in current with voltage. The black, blue, and red dashed lines represent the reference potential, Dirac point, and Fermi level, respectively, across the length of the channel.

which dissipate their excess energy to the channel via different mechanisms. The consequent local heating of the lattice due to these mechanisms, marked by the onset of diffusion of heat from the source to sink and the beginning of a state of electrothermal nonequilibrium, is referred to as intrinsic heating of the channel. During prolonged operation of a device, the self-heating manifests as a consequence of accumulation of intrinsic heating over time and dimensions of the device, which conceals the dependence of breakdown on gate and drain voltages. The intrinsic heating results in a substantial population of hot electrons without causing early damage and provides a window to study the true effects of gate and drain voltages on breakdown. The thermal diffusion time (t_{diff}) of a typical graphene transistor is approximately few tens of nanoseconds [10]. Hence, the intrinsic heating can be explored by probing the high-field transport for $t < t_{\text{diff}}$ ($\sim$10 ns).

We capture the effects of intrinsic heating on high-field transport in Fig. 3(a). It highlights two striking features: 1) linear increase in current with drain voltage for operation of the device near the Dirac point ($V_g = 60$ V) and 2) quasi-saturation in current at high drain voltages for operations away from the Dirac point. In order to explain this behavior, we invoke the band structure of graphene and consider the possibility of occupancy of various energy states [see Fig. 4]. The hot carriers thermalize among themselves by carrier–carrier scattering and relax to Fermi level by dissipating the excess thermal energy to the lattice via phonons. The scattering rate is proportional to density of states available at the final state and quantified by Fermi's golden rule (FGR). The operation of transistor away from the Dirac point permits such transitions due to the presence of a large number of states. The eventual electron-optical phonon scattering results in current saturation. The density of states in graphene decreases near the Dirac point, which reduces the probability of transition of hot electrons from higher energy state to a lower energy state in the vicinity of the Dirac point. The absence of transitions due to Pauli blocking [28] of final states causes a substantial reduction in electron–phonon scattering, which results in a linear increase in current with the drain voltage. In pump and probe-based experiments, it has been observed that such a restriction on scattering can contribute to attainment of near-Fermi velocity by hot electrons [29] and cause delayed cooling of hot carriers [30].

Having investigated the field dependence of intrinsic heating, we shift our attention to the consequences of intrinsic heating on the device breakdown. Fig. 3(a) highlights a substantial decrease in the breakdown current and noticeable increase in the breakdown voltage as Fermi level approaches the Dirac point. The decrease in current is attributed to the reduction in density of states near the Dirac point. In order to explain the effect of electrostatic doping on the breakdown voltage, we consider the relaxation of hot electrons at different Fermi levels. As discussed earlier, the emission of optical phonons is the primary mechanism behind the relaxation of hot electrons. The scattering of electrons to the states near the Dirac point is suppressed due to Pauli blocking of the electronic-state deficit region. In the absence of substantial rate of scattering, the relaxation of hot electrons happens slowly through a meager population of optical phonons. Consequently, the breakdown happens at higher voltages.

It is instructive to discuss the roles of various phonon modes in energy relaxation during intrinsic heating. The graphene optical phonon, SiO_2 surface polar phonon, and HfO_2 surface polar phonon modes are located at 200 meV [31], 58.9 meV [32], and 21.6 meV [32], respectively. The large difference in energies of surface polar phonons and

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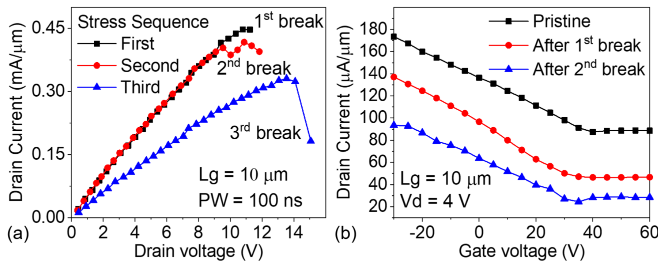

Fig. 5. (a) Controlled breakdown of a long-channel device. The ramping of voltage pulses (V_{ds}) is stopped after a reduction in current is observed. The voltage is again ramped from 0 V, resulting in a series of discrete breakdowns. (b) DC I_d–V_g performed after every breakdown. The Dirac point stays invariant, while the drain current shows a reduction after every breakdown.

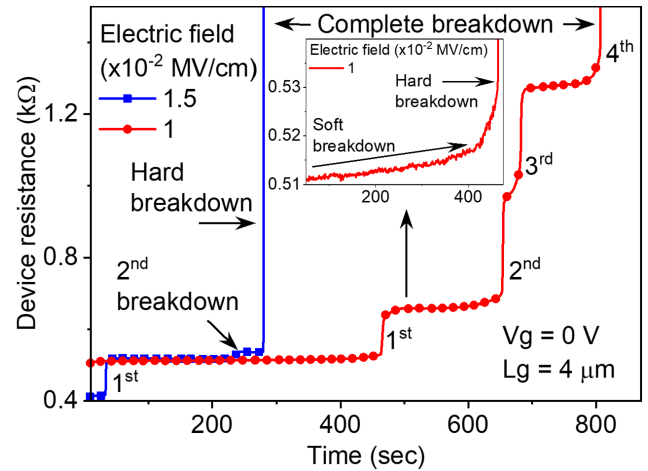

Fig. 6. Signatures of time-mediated breakdown captured as discrete increments in the device resistance at different time instants. The devices show a series of partial breakdowns before undergoing a complete breakdown. Two different modes of breakdown, soft and hard, are shown in the inset.

graphene optical phonons indicates significant scattering of hot carriers through the top and bottom oxides. The surface polar phonons provide an indirect path for relaxation of hot electrons, playing a dominant role in current saturation [31]. While scattering through surface polar phonons transfers the energy of a major fraction of hot electrons to the substrate, a relatively less dominant scattering through graphene optical phonons increases the lattice temperature. The increase in temperature of graphene phonons has earlier been observed through changes in intensities of Stokes and anti-Stokes peaks in Raman spectrum of a biased graphene [15]. Excessive scattering at high electric fields increases the contribution of both surface polar phonons and graphene optical phonons toward current saturation and lattice temperature. A scrutiny of low-bias resistance in Fig. 3(b) shows few notable changes. The device operated near the Dirac point ($V_g = 60$ V) shows the reduction in low-bias resistance after every injection of nanosecond charge burst. The operations in the p-doped region ($V_g = 0$ and -50 V) show a slight increase in resistance in the prebreakdown region. The former reduction could be due to the dissipation of excess heat near the metal–graphene interface and consequent current annealing of the interface. The increase in resistance is attributed to gradual breakdown of the channel.

The graphene–dielectric interface generally contains trapped water molecules, impurities, and fixed charges, which results in its p-type doping and shifts in the Dirac point. In order to preclude their role in changing the low-bias dc resistance, we perform a series of controlled breakdown measurements on a long-channel device [see Fig. 5(a)] and monitor the changes in I_d–V_g characteristics after every breakdown. As shown in Fig. 5(b), the device does not show any substantial shifts in the Dirac point. A large reduction in the drain current has been observed after every breakdown. Such a reduction suggests an increase in the channel resistance, possibly due to the creation of defects. A large change in the Dirac point would indicate field-induced trapping/detrapping at graphene–dielectric interface, which has not been observed here.

IV. Isothermal Heating of Graphene

The oxidative nature of breakdown imparts it a kinetic behavior, with exponential dependence on $-E_a/T$, where E_a is the activation energy for oxidation and T is the lattice temperature. Arguably, the breakdown of graphene, and 2-D materials in general, demands investigations at different isothermal conditions. As discussed previously, intrinsic heating due to different electrostatic conditions contributes to lattice heating. In this section, we utilize intrinsic heating to maintain an isothermal condition during far-equilibrium state of operation and explore the breakdown behaviors. The isothermal conditions correspond to a local temperature of the lattice, while electrons undergo temperature swing due to recursive processes of thermalization and phonon emissions. The state of far-equilibrium is selected so as to have a steady rate of collisions and temperature gradient across the device, while low electric fields are applied to avoid early breakdown due to self-heating.

The breakdown behaviors due to isothermal heating of two different devices are captured in Fig. 6. The devices are stressed with a constant electric field until a complete breakdown is achieved. Interestingly, the devices show a series of time-dependent step-by-step increase in resistance before undergoing a complete breakdown. The device stressed with 1.5×10^{-2} MV/cm shows early breakdown, whereas the device stressed with 1×10^{-2} MV/cm shows delayed breakdown. A scrutiny of the breakdown characteristics reveals two different modes of breakdown—soft and hard breakdowns. The soft breakdown is characterized by a gradual increase in the resistance, whereas the hard breakdown shows an abrupt increase in the resistance. These two modes of breakdown are shown in inset of Fig. 6. Moreover, the number of soft and hard breakdowns increases with decrease in the electric field. In order to understand these observations, we invoke the mechanism of oxidative breakdown of graphene. The Arrhenius nature of oxidation predicts an increase in rate of oxidation with temperature, which explains the field dependence of breakdown. The oxidation of graphene is a multistage process, involving dissociation of oxygen on graphene, formation of intermediate species, and evolution of CO_2 [33]. The dissociation of oxygen is a site-specific process. The dissociation over the basal plane happens via an endothermic process, making it a high-temperature process. On the contrary, vacancies provide

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a favorable site for dissociation of oxygen via an exothermic process. After dissociation, the vacancies get saturated with ether or carbonyl groups, which provides additional sites for dissociation of oxygen. The intermediate oxygen-containing species are desorbed as CO_2 or CO, eventually exposing more vacancies for dissociation of oxygen. The gradual rise in rate of degradation, captured as soft breakdown in inset of Fig. 6, could be attributed to increase in a number of active sites for dissociation with every desorption of CO_2. An increase in number of active sites, in turn, initiates a chain reaction, resulting in hard breakdown. More details on vacancy-assisted oxidation can be found in [33] and [34]. Although we have discussed the case of preferential oxidation at vacancies, other defect structures (grain boundaries, triple junctions, wrinkles, and folds) can also provide sites for dissociation of oxygen. The constant voltage stressing [Fig. 6] also shows multiple jumps or multiple hard/soft breakdowns. These jumps could be attributed to creation of multiple defect sites. Such time-dependent successive breakdown events have also been observed during constant voltage stressing of oxides [35] and hexagonal boron nitride (hBN) [36].

We substantiate the mechanism behind defect-dependent oxidation of graphene through Raman mapping after every occurrence of abrupt increase in resistance during constant voltage stressing of two different devices. It has earlier been observed that prolonged irradiation of graphene results in an increase in the intensity of D-peak (I_D) due to the creation of more defects [37]. However, the increase in the intensity saturates after a particular defect density, after which all the characteristic peaks of graphene (D, G, and 2-D) show a decrease in intensity due to ablation of carbon or formation of amorphous carbon [37]. Here, we monitor the ablation of carbon and defect density through the changes in intensities of G-peak (I_G) and D-peak (I_D), respectively. It should be noted that the defect density in graphene is generally quantified using the ratio I_D/I_G [38]. The value of the ratio becomes indiscernible for regions with low defect densities. Therefore, the ratio (I_D/I_G) has not been used to investigate the defect evolution during constant voltage stressing. The investigation of Raman map shows a localized increase in the intensity of D-peak in Fig. 7(a) and (b) and reduction in the intensity of G-peak in Fig. 7(c)–(e). The increase in D-peak represents the creation of more defects [37], whereas the decrease in the intensity of G-peak indicates ablation or oxidation of graphene [37], [39]. The observation corroborates with the proposed mechanism, which involves site-specific oxidation followed by creation of more defects. Hence, electrical breakdown of graphene involves recursive occurrences of two processes: 1) defect-specific dissociation of oxygen and 2) oxidative removal of carbon, resulting in defect-by-defect unzipping. The defect-dependent oxidative breakdown of graphene suggests that devices with relatively low defect density would sustain higher electric fields for longer durations in vacuum. In an interesting work by Kim *et al.* [40], it was demonstrated that the devices based on exfoliated graphene can sustain high electric fields ($\sim 4.2 \times 10^{-2}$ MV/cm) in vacuum while emitting light for >200 h. The reported values of electric field and duration of operation exceed the corresponding values shown

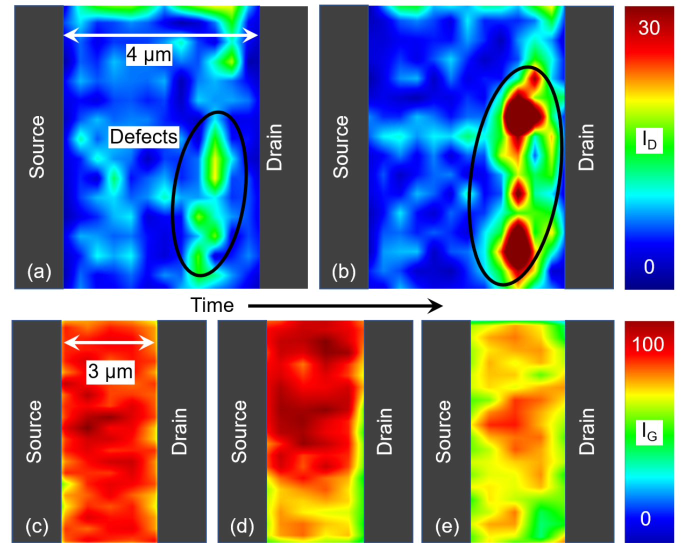

Fig. 7. Signatures of defect-by-defect breakdown captured through Raman mapping of the damaged channel of two different devices. (a) and (b) Increase in intensity of D-peak due to constant voltage stressing of the device. (c)–(e) Decrease in the intensity of G-peak due to constant voltage stressing of the device. The damage occurs primarily around the defect site, indicating the site selectivity of oxidation.

in Fig. 6, highlighting the vital roles of defects and ambient oxygen in the breakdown of graphene-based devices.

V. Pathways to Heat Dissipation

The rate of oxidative breakdown increases with temperature due to its Arrhenius-like dependence on temperature. Hence, various breakdown mechanisms discussed previously are expected to depend on cumulative effects of various thermal resistances across the pathways to the heat sinks. The electrothermal network of graphene FET, shown in Fig. 8(a), highlights two distinct paths to dissipate excess heat. The lateral spread (Path 2) of relaxation of hot electrons is governed by thermal healing length $L_H = (\kappa W h/g)^{1/2}$, where κ is the thermal conductivity of graphene, W is the width of the device, and g is the thermal conductance to the substrate per unit length [41]. For a typical graphene transistor ($L, W > 1\ \mu$m and $T_{ox} \sim 100$ nm), the healing length corresponds to $\sim$100 nm [41]. Hence, for the devices considered here, a substantial fraction of heat dissipates through the substrate. In this section, we study the effect of vertical thermal resistance on the breakdown behavior. Assuming back-Si thickness (t_{Si}) $\gg L, W \gg$ oxide thickness (t_{Ox}), the vertical thermal resistance R_{th} is given by $1/(\text{hLW}) + t_{Ox}/(k_{Ox}\text{LW}) + 1/(2k_{Si}(\text{LW})^{1/2})$, where h is the thermal interface conductance between graphene and the oxide ($\sim 10^8$ Wm^{2}K^{-1}) and k_{ox} and k_{Si} are thermal conductivities of the oxide and silicon, respectively [42], [43]. The dependence of breakdown on thermal resistance of the substrate is shown in Fig. 8(b). The breakdown behavior shows a reduction in breakdown field with increase in R_{th}. The devices show saturation in drain current due to intraband heating in the p-doped region and the extent of saturation increases with R_{th}. Moreover, the devices with the highest R_{th} fails at the lowest field and drain current and vice versa. During high-field transport, the emission of

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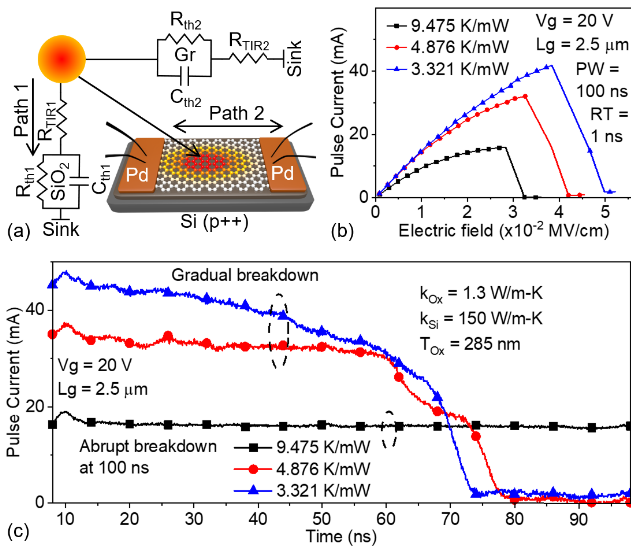

Fig. 8. (a) Electrothermal network of a graphene FET. (b) Devices show an increase in breakdown field and reduction in current saturation with decrease in thermal resistance of path 1. (c) Breakdown behavior changes from abrupt to gradual with reduction in thermal resistance of path 1. Characteristics shown in (b) correspond to three different devices having different channel widths. Their current transients during breakdown are shown in (c).

phonons in the devices with high R_{th} causes relatively more temperature drop across the device, which in turn increases the possibility of phonon bottleneck and current saturation. The rise in lattice temperature also results in increase in rate of degradation, as shown in Fig. 8(c). The dependence of rate of degradation on the R_{th} highlights the impact of electrothermal transport on kinetics of degradation.

The R_{th} also depends on thermal resistance of the Si/SiO_2 stack and thermal interface resistance between graphene and the dielectric. They have not been considered here due to the unavailability of measurement systems and devices suitable for specific measurements. Earlier, IR imaging [12] and electrothermal simulations [10] have shown a proportional scaling of channel temperature with oxide thickness. A reduction in channel temperature due to insertion of hBN between graphene and dielectric has been observed using the Raman thermometry [44].

VI. Unified Mechanism for Breakdown and SOA

Thus far, we discussed the breakdowns during nonequilibrium and far-equilibrium states, which are two extreme cases of operation of a device. In this section, we explore a unified mechanism behind breakdown. A rapid rate of oxidation due to high-field and temperature during nonequilibrium state (few nanoseconds) can mask the occurrence of defect-by-defect breakdown. Similarly, relatively low-field and temperature in far-equilibrium state (seconds) can conceal the role of intrinsic heating. Therefore, we use a time scale of microseconds to capture the discernible signatures of intrinsic heating and defect-by-defect breakdown. Fig. 9 shows the breakdown behavior captured during near-equilibrium operation and highlights the following behaviors: 1) current saturation during operation in the p-doped region; 2) linear behavior during operation near the Dirac point; 3) increase in breakdown voltage with decrease in electrostatic doping; and 4) series of discrete increments in low-bias resistance of the devices operated in the doped region for voltages in excess of 1.5 V. Behaviors 1, 2, and 3 corroborate the breakdown due to intrinsic heating, whereas behavior 4 indicates defect-by-defect breakdown. Hence, the breakdown behaviors correspond to both intrinsic heating and defect-by-defect breakdown. Presumably, the breakdown is expected to proceed in defect-by-defect fashion due to intrinsic heating during all transient states and electric fields.

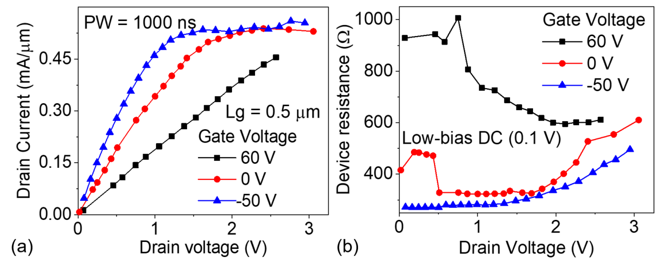

Fig. 9. Signatures of intrinsic heating and defect-by-defect breakdown during operations in near-equilibrium state. (a) Linear rise in current for operation near the Dirac point ($V_g = 60$ V) and saturation for operation in the doped regions. (b) Low-bias dc resistance shows a gradual reduction for the transistor operated near the Dirac point. A gradual pulse-by-pulse increase in resistance is distinctively visible for operations in the doped regions. All the devices showed abrupt permanent damage (channel open) for the voltages higher than the maximum drain voltages shown here.

Having discussed the breakdown mechanism of graphene-based transistors, we demarcate a SOA and underscore the factors limiting the operation. The SOAs for two sets of devices discussed in this work are shown in Fig. 10. The figure highlights that the devices operated in nonequilibrium state feature relatively longer boundary than those operated in far-equilibrium state. The maximum values of drain voltages and drain currents are bounded by oxidation due to Pauli-blocked delayed heating and excessive heating due to intraband heating, respectively. The SOA boundaries shrink as the device operation is moved towards near or far-equilibrium regions while increasing the duration of operation and decreasing the electric field across the channel. As discussed earlier, this happens due to slow oxidation of carbon at relatively low temperatures but longer duration of operation. Hence, during EOS/ESD events, the channel is expected to undergo rapid oxidation due to intraband heating or Pauli-blocked delayed heating. A relatively longer operation of graphene (e.g., interconnect, gate electrode, or sensors) is expected to show slow time-mediated defect-by-defect breakdown. As a corollary to the discussion presented in Section V, the thermal resistance of the substrate is expected to contribute to the overall spread of the SOA. The shrinking of SOA due to defects and thermal resistance necessitates the use of suitable defect engineering techniques [45] and 2-D heat spreaders [44], respectively, to increase the robustness of graphene-based devices.

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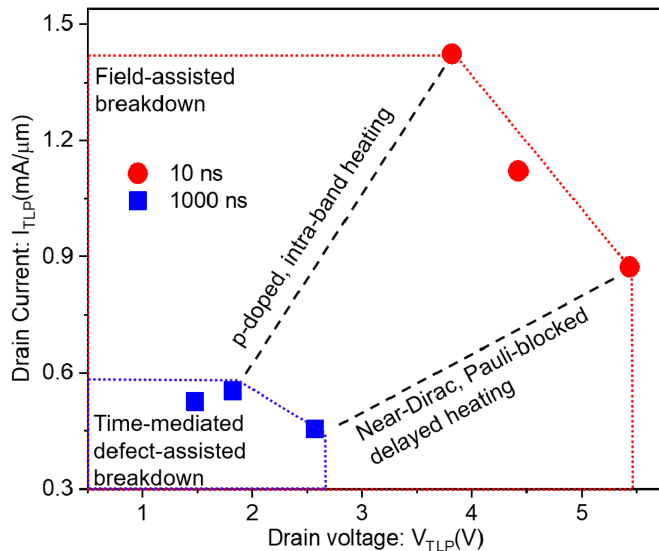

Fig. 10. SOA of graphene-based transistors operated in nonequilibrium state (circle) and near-equilibrium state (square). The allowed values of drain voltages and drain currents at different gate voltages form an irregular pentagon. The SOA shrinks considerably for longer pulse widths due to time-mediated defect-by-defect breakdown.

VII. Conclusion

In summary, we discussed the breakdown of graphene FETs under various operating conditions and transient states. A unique mechanism involving delayed phonon emission due to Pauli blocking of states was found to dictate the breakdown near the Dirac point, while intraband heating was found to cause early breakdown during operations in doped states. A time-mediated and defect-dependent breakdown mechanism was revealed by isothermal heating of graphene. Interestingly, these three mechanisms define the SOA of graphene-based devices. The suppression of electron-phonon scattering due to Pauli-blocked states near the Dirac point is expected to cause excessive contact heating in downscaled RF transistors, which calls for design of robust metal–graphene interface. Moreover, the applications requiring prolonged operation of graphene are expected to undergo degradation or aging due to kinetic nature of oxidation, necessitating their periodic destressing. In a nutshell, the reliability of a 2-D material-based device is governed by electro-thermo-chemical transport, which leads to a time-mediated and defect-by-defect unzipping behavior, eventually causing its breakdown.

Acknowledgment

The authors would like to thank Prof. Srinivasan Raghavan (CeNSE, IISc) for fruitful discussions.

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