On the Channel Hot-Electron's Interaction With C-Doped GaN Buffer and Resultant Gate Degradation in AlGaN/GaN HEMTs

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***Abstract*— In this work, we report a critical semi-ON-state drain stress voltage above which the gate current increases significantly and degrades permanently in AlGaN/GaN high electron mobility transistors (HEMTs). The observed critical voltage was found to be channel field-dependent by analyzing devices with different field plate lengths and passivation thicknesses, along with different gate–drain distances. Besides field dependence, the critical voltage was found to be carrier energy dependent by comparing the performance of devices subjected to semi-ON-state stress with devices under OFF-state stress. Experimentation on HEMTs with different buffer carbon doping variations revealed the degradation phenomenon to be a function of carbon doping in the GaN buffer. Furthermore, detailed electric field and electron temperature analysis revealed the drain edge to be a hot spot in accelerating interaction of hot electrons with traps in the GaN buffer leading to gate current degradation. A mechanism based on hot electron–buffer trap interaction-induced thermoelastic stress buildup and subsequent defect formation in the GaN buffer is proposed to explain the observed performance degradations. Observations such as a significant rise in channel temperature and accumulation of mechanical stress in the GaN buffer validate the proposed mechanism. Finally, the processes responsible for degradation lead to catastrophic failure of the device for longer stress times by the formation of cracks and pits in the GaN buffer, as validated by the postfailure field emission scanning electron microscopy (FESEM) analysis.**

***Index Terms*— AlGaN/GaN high electron mobility transistors (HEMTs), buffer traps, critical voltage, device design, electroluminescence (EL), gate leakage, hot electron, reliability.**

I. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are extensively being used in high-power and high-frequency applications [1]. These applications expose the device to semi-ON condition, where high electric field and high carrier density exist simultaneously [2]. These operating conditions provide suitable environment for hot-electron generation, which are known to be a major source of degradation in GaN HEMTs [2]–[8]. Moreover, interaction of hot electrons with trap states results in several reliability issues, such as drain current (I_D) and transconductance (g_m) degradation [4], threshold voltage (V_{Th}) shift [5], dynamic ON-resistance (R_{ON}) [6], generation of electrically active defects [7], and impact ionization-induced time-dependent dielectric breakdown (TDDB) of gate-stack [8]. HEMTs having intentional carbon [9]/iron [10] doping are more prone to hot-electron-induced degradation because of doping-induced traps in the GaN buffer [11]. Several reliability issues affecting drain current, channel, and buffer properties due to interaction of hot electrons with GaN buffer have been reported in the past, such as kinks in the output characteristics [12], current collapse [2], and premature vertical stack breakdown due to increased leakage [13]. However, any impact of such an interaction on gate stability is yet to be explored. The impact of hot electrons on gate degradation has only been considered due to changes happening near the gate electrode [5], [8]. Our recent study [14] highlighted that interaction of hot electrons with the carbon-doped GaN buffer significantly affects the channel electric field profile. Moreover, such interactions were found to be dependent on device parameters, such as the gate–drain distance (L_{GD}), the gate-connected field plate length (L_{FP}), and the SiN_x passivation thickness (t_{Passi}). While the study did show gate leakage degradation resulting from such interactions, the mechanism governing the phenomenon was not explored. A similar interdependence of electric field distribution and hot-electron dynamics, along with its impact on trapping related device reliability, was observed in recent studies conducted on p-GaN HEMTs [15], gate injection transistors (GITs), and hybrid-drain-embedded GITs (HD-GITs) on the C-doped GaN buffer [16], [17].

Gate degradation not only influences the transistor performance by affecting critical parameters, such as subthreshold swing and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio [18], but also adversely affects the device reliability [19], [20]. Therefore, it becomes essential to understand the underlying physical mechanism in order to optimize device design for improved device performance and reliability. In this work, we report a semi-ON-state stress-induced gate leakage degradation and the existence of

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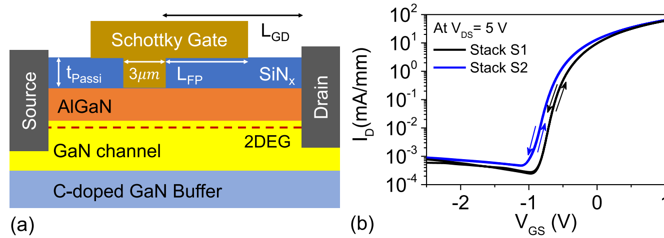

Fig. 1. (a) Schematic of the AlGaN/GaN HEMTs used for the investigation. The device parameters that were varied have been labeled. (b) Typical dual-sweep transfer characteristics of the HEMTs fabricated on stacks S1 and S2 having C-doping variation in the GaN buffer. Device dimensions are $L_{GD} = 9$ μm, $L_{FP} = 4$ μm, and $t_{Passi} = 20$ nm.

an associated critical voltage for its onset in AlGaN/GaN HEMTs. Electroluminescence (EL)/photoluminescence (PL), Raman spectroscopy, and thermal measurements have been employed to understand the underlying mechanism responsible for hot-electron generation and interaction with traps in the GaN buffer. The impact of carbon doping (C-doping) in the GaN buffer on the observed degradation is discussed. Besides, the factors governing the degradation have been identified by analyzing devices with different physical dimensions, such as L_{GD}, L_{FP}, and t_{Passi}. This article is organized as follows. In Section II, the device structure and experimental setup are described. Gate leakage degradation under the semi-ON stress condition is discussed in Section III. The source of observed performance degradation is discussed in Section IV, by studying its dependence on lateral device design parameters, namely, L_{GD}, L_{FP}, t_{Passi}, and on buffer C-doping. Furthermore, a physical model describing the observed device behavior is proposed and experimentally validated in Section V. Finally, the work is concluded in Section VI.

II. Experimental Setup

Schottky-gated AlGaN/GaN HEMTs, as shown in Fig. 1(a), were fabricated on GaN on Si epistack using a well-optimized process [21]. For monitoring the impact of device design parameters on device performance, design variables, namely, L_{GD}, L_{FP}, and t_{Passi}, were varied in each process lot. Moreover, to analyze the impact of buffer traps on device performance, the fabrication was carried out on two different GaN buffer stacks (labeled as S1 and S2). Both the stacks had similar epilayer arrangement with an 18-nm $Al_{0.25}Ga_{0.75}N$ barrier, a 175-nm undoped GaN channel, and a thick (>5 μm) GaN buffer. However, the two stacks had different C-doping concentration in the GaN buffer, resulting in different 2-dimensional electron gas (2DEG) densities. While S1 had a 2DEG density of $\sim 8.5 \times 10^{12}$ cm^{-2}, the same for S2 was 9×10^{12} cm^{-2}, indicating a higher C-doping concentration in S1. Fig. 1(b) shows the typical dual-sweep transfer characteristics of the HEMTs under test with superior ON-state performance, low OFF-state leakage, and negligible V_{Th} hysteresis.

The devices were subjected to a *measure–stress–measure* cycle with the device being stressed in the semi-ON-state by applying $V_{GS\text{-}Stress} = V_{Th} + 0.5$ V and varying the drain stress voltage ($V_{DS\text{-}Stress}$) from 80 to 220 V. Different parameters of the device were monitored on-the-fly to analyze impact on electrical characteristics, electric field, stress profile, and temperature profile of the device. A Parameter Analyzer (4200A-SCS) was used for on-the-fly monitoring of the temporal response of the transistor currents during the stressing period and the transfer characteristics (I_D–V_{GS} for $V_{DS} = 1$ V) of the HEMTs in prestress and poststress conditions. Electric field profile estimation was done with the help of EL microscopy by using the Andor iXON Ultra EMCCD camera. Moreover, EL spectrum and stress profile estimation were done with the help of Horiba micro-Raman spectroscopy setup. The stress profile was extracted using 532-nm laser-based Raman mapping. The EL spectra were captured over the wavelength range of 350–850 nm from evenly spaced points ($\sim$1 μm spot size) between the gate field plate edge (GFPE) and the drain edge (DE). The peak EL intensity from these captured spectra along the lateral dimension, from GFPE to DE, allowed extraction of EL line scans. While the EMCCD camera provides a 2-D field distribution profile, EL line scans provide further insight into the electric field distribution in the gate–drain (G-D) access region. In addition, the GaN channel temperature was monitored during the stress cycle with the help of an NT-220C Thermoreflectance thermal imaging system by employing a 365-nm noncoherent UV LED.

III. Device Performance Under Semi-ON Stress

A. Impact on Gate Stability

GaN HEMTs fabricated on stack S1 were stressed in the semi-ON-state, and the device characteristics, including gate leakage current (I_G) transients, were monitored. Fig. 2(a) shows the $I_G(t)$ monitored for multiple $V_{DS-Stress}$. Following observations can be made from the transients: 1) for $V_{DS-Stress} \leq 120$ V, I_G degradation is minimal even for stress time (t_{Stress}) of $\sim$1000 s; 2) as $V_{DS-Stress}$ is increased beyond 120 V, I_G starts increasing with t_{Stress}; 3) the fast rate of increase in I_G is accompanied by fluctuations for $t_{Stress} > 100$ s; and 4) for the subsequent stress cycles ($V_{DS-Stress} = 150$ V), I_G starts increasing from a higher value at $t_{Stress} = 0$ s [corresponds to $t = 3060$ s in Fig. 2(a)], suggesting a permanent degradation in the gate leakage. These observations point toward the existence of a critical drain-stress voltage (V_{Cr}) governing the onset of I_G degradation in semi-ON-state, which, in this case, is $\sim$140 V.

B. Permanence of Gate Leakage Degradation

Fig. 2(a) suggested the observed degradation in I_G to be permanent. In order to further investigate this aspect, the step-stress approach was adopted, as shown in Fig. 2(b). The initial I_G measurements were done at a $V_{DS-Stress} < V_{Cr}$. This was followed by stressing the device at $V_{DS-Stress} \geq V_{Cr}$, before repeating the measurement for $V_{DS-Stress} < V_{Cr}$. Such a measurement cycle allowed us to measure the change in I_G for $V_{DS-Stress} < V_{Cr}$ induced by exposing the device to $V_{DS-Stress} > V_{Cr}$. Following observations can be made from Fig. 2(b): 1) I_G reduces with t_{Stress} for $V_{DS-Stress} < V_{Cr}$; 2) I_G drastically increases for $V_{DS-Stress} \geq V_{Cr}$, which further

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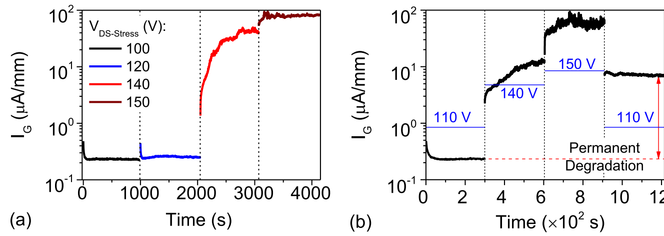

Fig. 2. Gate leakage transients recorded at multiple $V_{\text{DS-Stress}}$'s showing (a) existence of a critical voltage (V_{Cr}) beyond which I_G increases significantly and (b) permanent ~2 order rise in I_G for $V_{\text{DS-Stress}} = 110$ V ($< V_{\text{Cr}}$) when stressed beyond V_{Cr}. Device dimensions are $L_{\text{GD}} = 9$ μm, $L_{\text{FP}} = 4$ μm, and $t_{\text{Passi}} = 40$ nm.

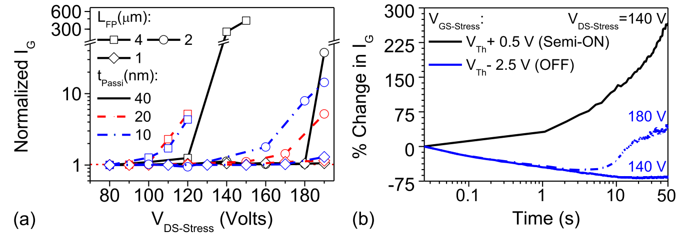

Fig. 3. (a) Normalized I_G (Normalized w.r.t. steady state I_G for 80 V stress) as a function of $V_{\text{DS-Stress}}$. L_{FP} and t_{Passi} varied keeping fixed $L_{\text{GD}} = 9$ μm. (b) Gate leakage transient under OFF- and semi-ON-state stresses showing higher $V_{\text{DS-Stress}}$ (180 V) required for degradation in the OFF-state. HEMT dimension: $L_{\text{GD}} = 9$ μm, $L_{\text{FP}} = 4$ μm, and $t_{\text{Passi}} = 40$ nm.

increases with t_{Stress}; 3) increasing $V_{\text{DS-Stress}}$ further adds to the I_G, indicating accumulative nature of degradation; and 4) I_G does not reduce to pristine level even on reducing $V_{\text{DS-Stress}}$ below V_{Cr}, establishing the observed phenomenon to induce permanent degradation in the gate leakage.

IV. Sources of Degradation

The presence of V_{Cr}, as noticed in Fig. 2(a), indicates the presence of a critical electric field governing I_G degradation phenomenon. Motivated by this field dependence, different device design parameters are examined in this section to determine the source of observed I_G degradation.

A. Impact of Channel Electric Field

The channel electric field can be modulated by changing L_{FP} and t_{Passi} [22]. To gain further insight into the field dependence of V_{Cr}, devices with different L_{FP}'s and t_{Passi}'s were analyzed, as shown in Fig. 3(a). The figure shows V_{Cr} to be dependent on both the parameters, with an increase in L_{FP} or a reduction in t_{Passi} leading to a lower V_{Cr}. Both increase in L_{FP} and reduction in t_{Passi} are expected to increase field magnitude near the GFPE [22]. This indicates field plate design to be an important parameter affecting semi-ON-state reliability of the device. Further, this establishes the observed I_G degradation to be field-dependent. However, the semi-ON-state stress is known to have high carrier density besides high electric field. This makes it necessary to consider carrier energy besides electric field to evaluate performance in the semi-ON-state. To isolate the impact of electric field and carrier energy, a comparison between I_G degradation in OFF-state and semi-ON-state is carried out. As shown in Fig. 3(b), I_G degradation in OFF-state happens at much higher voltage ($V_{\text{Cr}} \sim 180$ V) compared to that in the semi-ON-state stress ($V_{\text{Cr}} \sim 140$ V). Moreover, the degradation is lower in OFF-state compared to that in semi-ON-state. This establishes that the presence of high electric field along with a higher carrier density in semi-ON-state accelerates the I_G degradation phenomenon.

B. Correlation Between Electric Field, Carrier Energy Hotspots, and I_G Degradation

In order to determine the electric field and carrier energy hot spots, further analysis was done using EL, which is a commonly used technique to study electric fields [23]. Fig. 4(a)–(c) depicts EL intensity (I_{EL}) maps extracted in the G-D access region for multiple $V_{\text{DS-Stress}}$'s. The figure indicates a shift in lateral electric field from GFPE to DE and an increase in I_{EL} as $V_{\text{DS-Stress}}$ is increased. The significant increase in I_{EL} is attributed to an increase in the electric field and generation of high energy electrons [2]. The EL intensity line scans (obtained by averaging the intensity along the device width), as shown in Fig. 4(d), reveal the I_{EL} peak to be confined near the GFPE for lower $V_{\text{DS-Stress}}$. However, as $V_{\text{DS-Stress}}$ is increased beyond V_{Cr}, EL distribution becomes increasingly confined near the DE leading to creation of a hot spot with relatively higher I_{EL}. To determine the carrier energy hotspots, the average energy of the electrons measured in terms of electron temperature (T_e) [24] is extracted and shown in Fig. 4(d). T_e is found to be higher near the DE and increases from ~2200 to ~5000 K as $V_{\text{DS-Stress}}$ is increased from 80 to 120 V. This suggests DE to be a carrier energy hotspot.

The increase in peak I_{EL} near the DE shows that the lateral electric field peak in the channel shifts from GFPE toward the DE. On the other hand, the significant rise in T_e near the DE shows that a large fraction of channel electrons possesses high kinetic energy, which are known as hot electrons. Moreover, an increase in I_{EL} near the DE (as shown in Fig. 4) accompanied by the onset of I_G degradation [as shown in Fig. 3(a)], for $V_{\text{DS-Stress}} > V_{\text{Cr}}$, suggests that hot electrons near the DE play a critical role in determining semi-ON-state performance of the device.

C. Determining Possible Trap Interactions of Hot Electrons

Preceding discussions highlight hot electrons and channel electric field to play an important role in determining I_G degradation under semi-ON stress. To further investigate the possibilities of interaction of hot electrons with traps in the device, the EL spectrum was analyzed. The EL spectrum was extracted near the DE due to the strong correlation between I_{EL} at DE and I_G degradation. Fig. 5(a) shows EL spectra as a function of $V_{\text{DS-Stress}}$ extracted at the DE. For $V_{\text{DS-Stress}} < V_{\text{Cr}}$, the EL spectrum has a long Maxwellian tail-like feature [23], with $I_{\text{EL}} \propto e^{-E_{\text{Photon}}/k_B T}$. As $V_{\text{DS-Stress}}$ increases beyond V_{Cr}, the EL spectrum shows distinct trends: 1) the spectral bandwidth increases, indicative of the rise in the energy of the channel electrons [shown in Fig. 5(b)];

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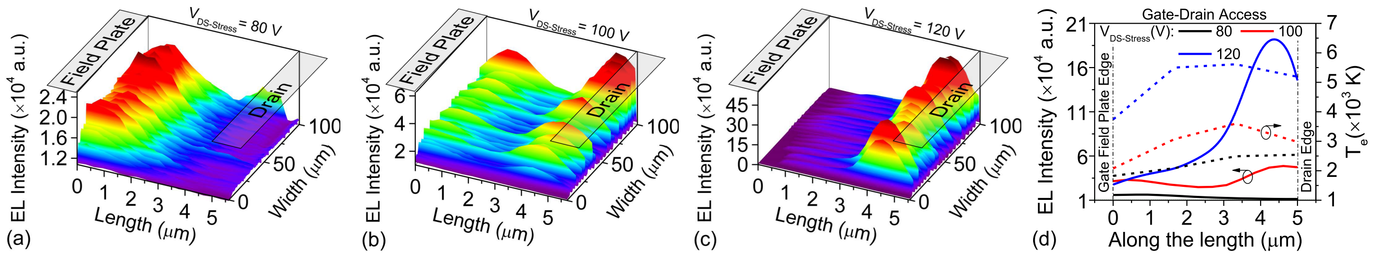

Fig. 4. EL microscopy images (3-D intensity plot) in the gate–drain access region obtained in semi-ON-state for $V_{DS-Stress}$ = (a) 80 V, (b) 100 V, and (c) 120 V. (d) EL intensity (width averaged) line scan and electron temperature (T_e) distribution in the access region as a function of $V_{DS-Stress}$. T_e has been extracted from the slope of the high-energy tail of the EL spectra. The HEMT had L_{GD} = 9 μm, L_{FP} = 4 μm, t_{Passi} = 20 nm, and V_{Cr} = 100 V.

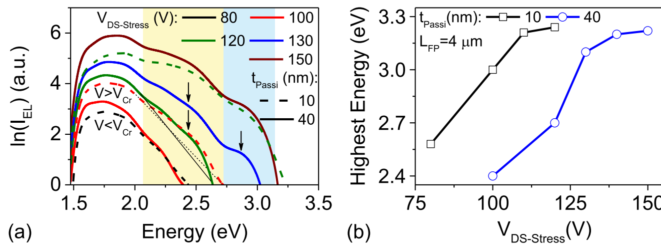

Fig. 5. (a) EL spectra extracted at DE for multiple $V_{DS-Stress}$'s, in semi-ON-state, showing two regimes separated by the critical voltage (V_{Cr}). The bias-dependent spectral evolution is compared for different passivation thickness of 10 and 40 nm, having L_{GD}= 9 μm and L_{FP} = 4 μm. (b) Plot of highest energy (high energy x-intercept of EL spectra) versus $V_{DS-Stress}$.

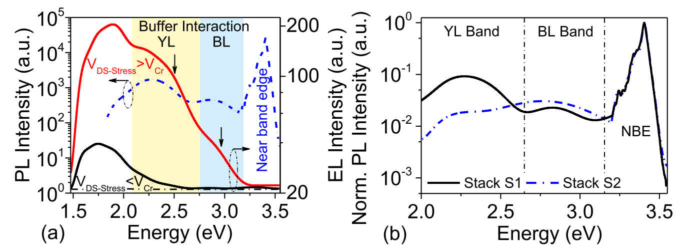

Fig. 6. (a) Comparison of UV PL spectra with EL spectra for $V_{DS-Stress} > V_{Cr}$ and $< V_{Cr}$ from HEMTs on stack S1. (b) Comparison of PL spectra from GaN buffer stacks S1 and S2 having variation in C-doping concentration.

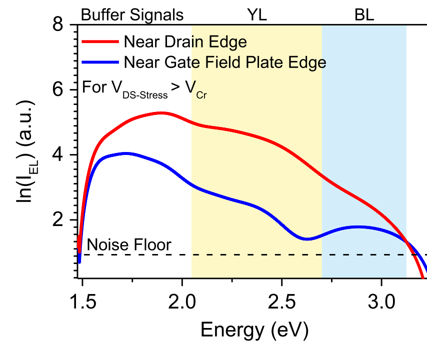

Fig. 7. EL spectra collected at two different locations show the presence of buffer signals in both the spectra. The HEMT had L_{GD} = 9 μm, L_{FP} = 4 μm, t_{Passi} = 20 nm, and V_{Cr} = 100 V.

2) I_{EL} increases with $V_{DS-Stress}$ indicating an increase in the concentration of hot electrons; and 3) for $V_{DS-Stress} \geq V_{Cr}$, strong deviation from the Maxwellian tail-like feature is observed due to appearance of prominent signals with distinct peaks in EL intensity [shown by arrows in Fig. 5(a)].

A comparative study between PL and EL spectra, as shown in Fig. 6(a), reveals the observed distinct peaks in the EL spectra to correspond to the well-known yellow luminescence (YL) and blue luminescence (BL) bands attributed to defects in the C-doped GaN buffer [25]. The presence of distinct peaks in the EL spectra within YL and BL bands can then be attributed to the interaction of hot electrons with defect states in the C-doped GaN buffer. Moreover, EL spectrum near the GFPE extracted for a $V_{DS-Stress} > V_{Cr}$ (as depicted in Fig. 7) suggests buffer interaction of hot electrons near the GFPE as well. The above analysis suggests the interaction of hot electrons with defects in the C-doped GaN buffer to be a possible source of the observed I_G degradation. In addition, the following observations suggest the process to be initiated near the DE, which then extends laterally up to the GFPE: 1) I_G degradation is seen only after the carrier energy hot-spot shifts to DE [Fig. 4(d)] and 2) relatively higher EL intensity and stronger buffer interaction signal is observed near the DE (see Fig. 7).

D. Hot-Electron's Interaction With Buffer Traps and I_G Degradation

To establish that the interaction of hot electrons with the carbon-induced buffer traps plays a central role in governing the I_G degradation, a comparative study was carried out on HEMTs fabricated on GaN stacks with the difference in C-doping concentration. A comparison of PL spectra for stacks S1 and S2, as shown in Fig. 6(b), shows a prominent YL band in S1, which is absent in S2. Moreover, the ratio of the PL intensity of the BL peak to that of the YL peak (I_{BL}/I_{YL}) is lower for S1, which shows higher carbon doping in S1, compared to S2 [26]. Moreover, HEMTs fabricated on stacks S1 and S2 had similar device dimensions and surface conditions for a fair comparison of semi-ON-state performance. As shown in Fig. 8(a), I_G shows a drastic increase (180% increase) for stresses beyond V_{Cr} for devices fabricated on S1. However, for similar stress duration, much lower change (∼30% increase) was observed for devices fabricated on S2. Fig. 8(b) shows a comparison of the EL spectra extracted at the DE of devices based on stacks S1 and S2. It reveals that the devices fabricated on S2 lack features of

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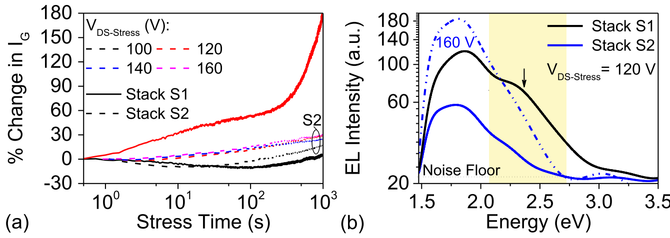

Fig. 8. (a) Stress-induced change in gate leakage current transient for multiple $V_{DS-Stress}$'s compared among HEMTs on stacks S1 (high C-doping) and S2 (low C-doping). The device based on S1 was not stressed beyond 120 V to avoid catastrophic failure. (b) EL spectra from HEMT on stack S1 show buffer interaction signals at a 120 V stress. Buffer signals are missing in EL spectra for HEMTs on S2 even during a 160 V stress. The devices had similar surface conditions, with $L_{GD} = 9$ μm and $L_{FP} = 4$ μm.

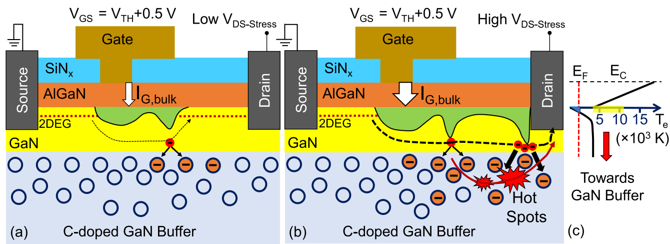

Fig. 9. Schematic showing gate leakage, depletion region, and hot-electron path in GaN HEMTs at (a) low $V_{DS-Stress}$ and (b) $V_{DS-Stress}$ ($>V_{Cr}$). Higher $V_{DS-Stress}$ increases hot-electron injection into the GaN buffer, creating parasitic conduction paths for gate leakage via hotspot formation. This is denoted by increasing thickness of the arrow depicting bulk component of gate leakage ($I_{G,bulk}$). (c) Schematic showing preferential injection of hot electrons with average electron temperature (T_e) ~5000–7000 K (yellow window) into buffer.

hot-electron–buffer trap interaction in the EL spectrum, which contrasts with that seen for a device fabricated on S1. Therefore, large degradation in I_G accompanied by the appearance of strong YL and BL signals in EL spectra is the characteristic feature of the interaction of hot electrons with C-doping-induced traps in the GaN buffer. This validates the role of hot electron–buffer trap interaction in semi-ON stress-induced I_G degradation.

V. Physical Mechanism Governing Hot-Electron-Induced Gate Leakage Degradation

A. Proposed Mechanism

Based on the observations of the shift in electric field peak from GFPE to DE and subsequent interaction of hot electrons with the buffer traps, the following mechanism is proposed to explain the observed I_G degradation. It is well known that GaN HEMTs exhibit an electric field peak at the gate edge (GE)/GFPE during semi-ON-/OFF-state stress [3]. Taking this into consideration, the 2DEG electrons are exposed to a high electric field at the GE and the GFPE. By acquiring kinetic energy from the field, the channel electrons are scattered out of the AlGaN/GaN quantum well, as shown in Fig. 9(a). Subsequently, the scattered electrons are trapped in the deep acceptor states that are plentiful in the C-doped GaN buffer [as seen from the PL spectra of stack S1 in Fig. 6(b)] [27].

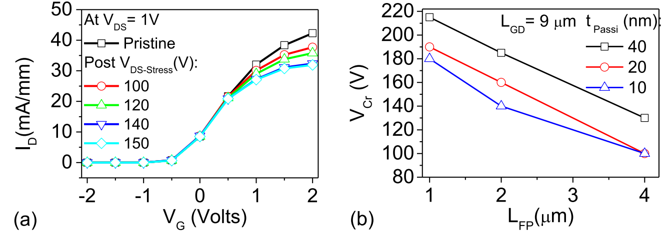

Fig. 10. (a) DC transfer characteristics of a pristine HEMT and post semi-ON-state stress. Dimensions: $L_{GD} = 9$ μm, $L_{FP} = 4$ μm, and $t_{Passi} = 40$ nm. (b) Dependence of critical voltage on field plate length and passivation thickness.

Trapping in GaN buffer leads to the lateral extension of the depletion region and subsequent field redistribution in the access region [28]. As $V_{DS-Stress}$ approaches V_{Cr}, the depletion region extends laterally up to the DE and results in an electric field peak near the DE. Given the larger depletion width and carrier availability due to the semi-ON-state, electrons gain significantly higher energy at the DE [seen in Fig. 9(b)]. These hot electrons have a high probability of being injected into the GaN buffer, as shown in Fig. 9(c). Subsequently, hot electrons exchange energy with the GaN lattice and lead to mechanical stress accumulation and significant rise in thermal stress in the buffer, as shown in Fig. 9(b). The thermoelastic stresses accumulate and trigger crack/pit formation from point defects and dislocations in the GaN buffer, which, being significantly doped by carbon, is a host to a large number of defects [11]. As a result, a low-resistance conduction path is formed between the gate/field plate and the drain contact through GaN buffer. This leads to a significant increase in I_G, as shown in Fig. 9(b).

B. Model Validation

1) Evidence of Electron Trapping in GaN Buffer: Based on the proposed mechanism, trapping of hot electrons in the GaN buffer should take place on applying $V_{DS-Stress}$ in the semi-ON-state. To validate this, the HEMT transfer characteristics were monitored before and after subjecting the device to semi-ON-state stress, as shown in Fig. 10(a). A significant drop is noticed in I_D after the stress without any shift in V_{Th} of the device. This establishes significant trapping in the G-D access region. Moreover, the shift in the peak EL intensity from GFPE to DE, as shown in Fig. 4(a)–(c), further establishes trapping in the GaN buffer [28].

2) Modulating Channel Depletion to Control V_{Cr}: As discussed in the proposed mechanism, V_{Cr} is the $V_{DS-Stress}$ required for extending the depletion region to DE. Consequently, any variation in device parameters controlling channel depletion should affect V_{Cr}. To evaluate this aspect, L_{GD}, L_{FP}, and t_{Passi} were considered as design variables to modulate channel depletion, and its impact on V_{Cr} of the device was monitored. Fig. 10(b) and inset of Fig. 11(c) show V_{Cr} to be dependent on L_{FP}/t_{Passi} and L_{GD}, respectively. It is observed that V_{Cr} decreases as L_{FP} is increased or t_{Passi} is decreased. Dependence of V_{Cr} on L_{FP} can be explained by comparing EL line scans for devices with different L_{FP}'s, as shown in Fig. 11(a). It reveals the EL intensity to be uniformly

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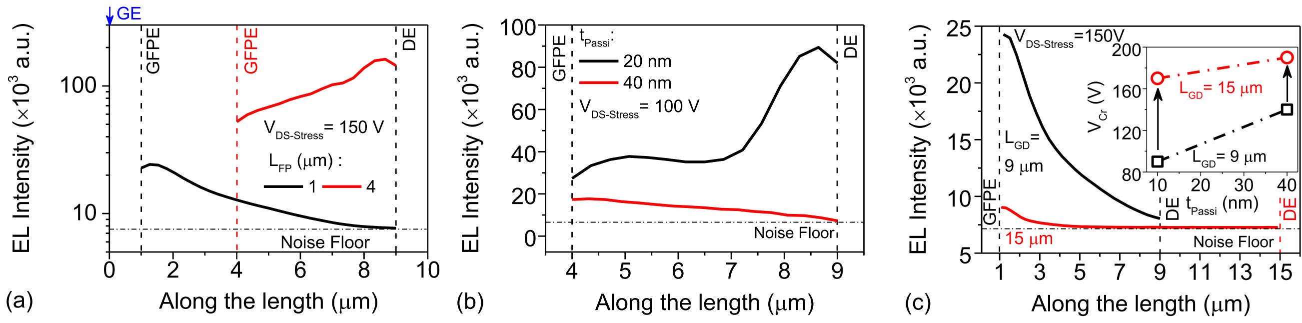

Fig. 11. Comparison of EL intensity (width averaged) line scans among devices having (a) variation in L_{FP} for a fixed $V_{DS-Stress}$ of 150 V, (b) variation in t_{Passi} for a fixed $V_{DS-Stress}$ of 100 V, and (c) variation in L_{GD} for a fixed $V_{DS-Stress}$ of 150 V (inset depicts effect of t_{Passi} on V_{Cr} with L_{GD} as a parameter, showing that V_{Cr} significantly increases as L_{GD} increases). Here, the origin for the x-axis is the GE.

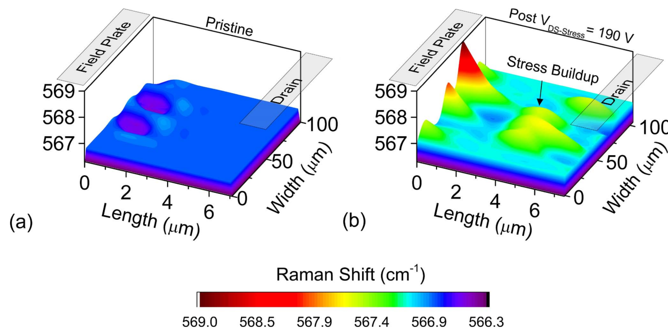

Fig. 12. Distribution of the Raman shift of $E_{2(High)}$ phonon mode in (a) Pristine condition and (b) post 190 V ($V_{DS-Stress} > V_{Cr}$) semi-ON stress. Mechanical stress buildup in the access region is indicated. The device had $L_{GD} = 9$ μm, $L_{FP} = 2$ μm, and $t_{Passi} = 20$ nm with $V_{Cr} = 185$ V.

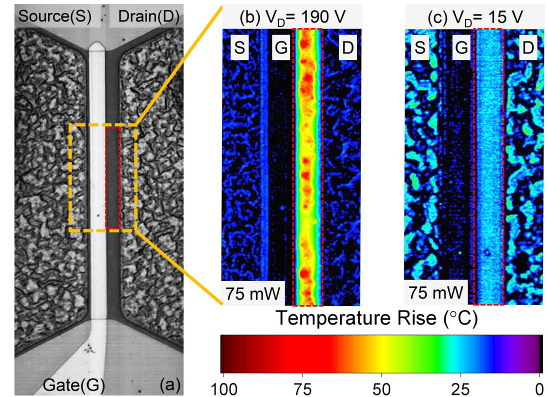

Fig. 13. (a) CCD image of the HEMT used for steady-state UV thermal imaging. Thermal images captured at (b) $V_{DS-Stress} = 190$ V ($>V_{Cr}$) in the semi-ON condition and (c) $V_{DS-Stress} = 15$ V in the ON-state. The output power is constant at 75 mW. The device had $L_{GD} = 9$ μm, $L_{FP} = 2$ μm, and $t_{Passi} = 20$ nm with $V_{Cr} = 185$ V.

distributed in the access region for a larger L_{FP} device and confined near the GFPE for a device with smaller L_{FP}. This establishes that, for devices with larger L_{FP}, a lower $V_{DS-Stress}$ is required to extend the depletion region up to the DE. Therefore, V_{Cr} has a lower value for devices with larger L_{FP}. Furthermore, the EL line scan for devices with 20-nm passivation shows significant EL signal at DE, whereas no such signal was visible for a device with thicker passivation (40 nm) for a similar $V_{DS-Stress}$, as shown in Fig. 11(b). This explains the reduction in V_{Cr} as t_{Passi} is reduced. Moreover, EL line scans for devices with different L_{GD}, as shown in Fig. 11(c), depict the EL signal to be absent at the DE for larger L_{GD} devices, unlike that for smaller L_{GD} devices. Therefore, the voltage required to extend the depletion region to DE and, hence, V_{Cr} would be higher for larger L_{GD} device [see the inset of Fig. 11(c)].

3) Hot-Electron-Induced Thermoelastic Stress Buildup: Electron trapping in the GaN buffer and the importance of field magnitude at DE in determining I_G degradation has been established. The proposed mechanism further suggests thermoelastic stress buildup due to the interaction of hot electrons with the buffer traps. Raman spectroscopy allowed us to evaluate stress conditions in the device. Fig. 12 depicts an overall positive shift in the $E_{2(High)}$ phonon mode frequency in the G-D access region and localized shifts near the GFPE and the DE after stressing the device in semi-ON-state stress with $V_{DS-Stress} > V_{Cr}$. This indicates elastic stress buildup

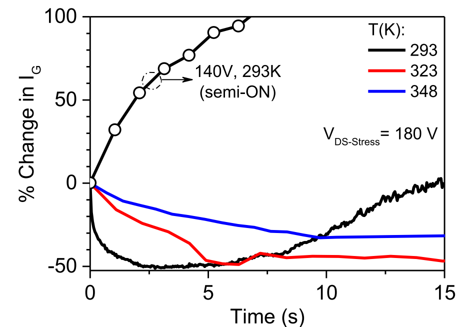

Fig. 14. Gate leakage evolution during OFF-state stress of $V_{DS-Stress} = 180$ V with $V_{GS-Stress} = V_{Th}$—2.5 V, as the device is heated to different temperatures, indicates I_G degradation to be absent at higher temperatures. The I_G transient during semi-ON stress ($>V_{Cr}$) is shown as a reference. The device had $L_{GD} = 9$ μm, $L_{FP} = 4$ μm, and $t_{Passi} = 40$ nm.

in the GaN buffer [29]. Lattice temperature measurements in the G-D access region [marked in the charge-coupled device (CCD) image shown in Fig. 13(a)] to estimate the thermal contribution of hot electron–buffer trap interaction reveal a significant rise in lattice temperature with the presence of localized hotspots, as shown in Fig. 13(b). On the other hand, stressing the device in ON-state while keeping the supplied electric power unchanged, results in a much lower temperature

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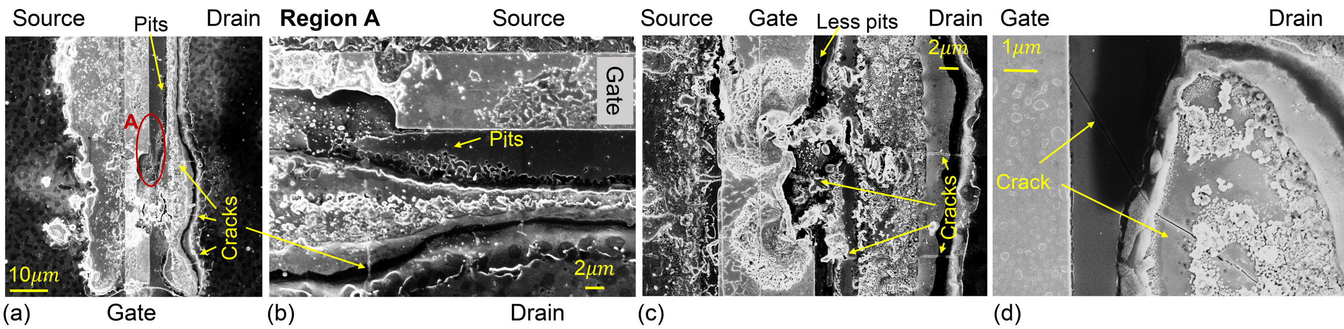

Fig. 15. FESEM images showing catastrophic failure in devices having (a) $t_{\text{Passi}} = 20$ nm and (c) $t_{\text{Passi}} = 40$ nm. Existence of cracks and pits is marked. (b) Magnified image of region A [marked with red circle in (a)]. (d) Magnified view of the damaged access region [for device depicted in (c)] showing crack traveling from GFPE to DE and further extending below the drain contact (seen due to drain pad peel off).

rise [$\Delta T \approx 25$ °C, as shown in Fig. 13(c)] compared to that in semi-ON-state stress [$\Delta T_{\max} \approx 85$ °C, as shown in Fig. 13(b)]. Furthermore, the temperature is uniformly spread in the G-D access region as opposed to localized hotspots observed during the semi-ON-state stress. This suggests hot electrons to play a significant role in increasing the lattice temperature, which can be attributed to three factors: 1) thermalization of the injected hot electrons by losing excess kinetic energy to the lattice; 2) phonon generation during recombination of the injected hot electrons with the trap states; and 3) significant increase in channel resistance due to the extension of depletion region toward DE induced by trapping of hot electrons in the GaN buffer.

Moreover, the absence of I_G degradation even at elevated temperatures on stressing the device in OFF-state, as shown in Fig. 14, further establishes the thermoelastic stress buildup due to interaction of hot electrons with buffer traps to be responsible for the observed I_G degradation.

4) Catastrophic Failure of the Device: On exposing the devices to longer semi-ON-state stress times with $V_{\text{DS-Stress}} \geq V_{\text{Cr}}$, devices exhibited catastrophic failure. Moreover, the catastrophic failure was preceded by a significant rise in I_G accompanied by the appearance of strong buffer signals in the EL spectrum. The intensity of such buffer signals increases with an increase in the density of point defects (e.g., Ga vacancy), extended defects (e.g., edge dislocations), and other structural imperfections (e.g., cracks and pits) [25], [30]. Therefore, the observed strong buffer signals, just before the device failure, indicate the formation of defects and cracks/pits in the buffer due to accumulation of thermoelastic stress beyond a critical value [31], which can lead to the observed device failure. Fig. 15 (a)–(d) shows the field emission scanning electron microscopy (FESEM) images of the devices that failed during prolonged semi-ON-state stress. Fig. 15(a) shows the FESEM of a device with $t_{\text{Passi}} = 20$ nm. Extensive damage to the source pad, gate/field plate edge facing the drain, and the drain pad is noticed. As shown in Fig. 15(b), multiple cracks (along the G-D length) are present in the G-D access region, accompanied by pit formation near the DE. This corroborates the mechanism explaining I_G degradation and subsequent failure triggered by hot electrons in the G-D access region. Furthermore, the FESEM of a device with thicker t_{Passi} of 40 nm, as shown in Fig. 15(c) and (d), shows hot-electron-induced failure signatures in the G-D access region similar to that for devices with $t_{\text{Passi}} = 20$ nm. However, the failure is with a lower density of cracks and pits. This is attributed to the reduced interaction of hot electrons with buffer as t_{Passi} is increased.

VI. Conclusion

Detailed semi-ON-state stress investigation on AlGaN/GaN HEMTs fabricated on carbon-doped GaN buffer revealed the presence of a critical drain stress voltage above which a drastic increase in gate leakage was observed. This observed degradation was found to be permanent and was prominent for devices having significant C-doping in the GaN buffer. Moreover, the critical voltage was found to be a function of L_{GD}, L_{FP}, and t_{Passi}, suggesting electric field distribution to be of prime importance. The onset of I_G degradation was preceded by shifting of peak electric field from GFPE to DE. This was accompanied by an increased EL intensity, a rise in electron temperature, and the appearance of YL and BL signals (in the EL spectra) near the DE. This reveals hot-electron generation and interaction with the buffer traps at the DE to determine the degradation process. Furthermore, the appearance of YL and BL signals in the EL spectra was attributed to the creation of defect states, due to the formation of cracks and pits, in the C-doped buffer, which explained the permanence of the observed degradation. A mechanism based on hot-electron-assisted defect formation and propagation, accompanied by increased trap assisted gate–drain leakage current conduction through the GaN buffer, is proposed. Defect formation was attributed to hot-electron interaction-induced thermoelastic stress buildup in the GaN buffer. The proposed mechanism was able to explain the field dependence of the observed I_G degradation, besides explaining the observation of catastrophic device failure on subjecting the device to a prolonged stress cycle. The catastrophic failure was found to be driven by crack and pit formation, which further establishes hot electrons and I_G degradation as serious reliability concerns in HEMTs.

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