# A NEW PHYSICAL INSIGHT AND 3D DEVICE MODELING OF STI TYPE DENMOS DEVICE FAILURE UNDER ESD CONDITIONS

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***Abstract***

*We present experimental and simulation studies of STI type DeNMOS devices under ESD conditions. The impact of base-push-out, power dissipation because of space charge build-up and, regenerative NPN action, on the various phases of filamentation and the final thermal runaway is discussed. A modification of the device layout is proposed to achieve an improvement (~2X) in failure threshold ($I_{T2}$).*

## I. INTRODUCTION

Aggressive scaling has resulted CMOS devices operating below 1 volt in sub 100nm node technologies. To communicate with external world, high voltage (HV) I/O devices are required, which can be integrated in the same CMOS process flow. To protect these devices from an ESD event, dedicated ESD protection devices are used [1]. An accurate modeling of ESD behavior, in these ESD protection and I/O devices, is a critical need for designing robust ESD protection circuits in sub 100 nm node technologies [1] [2]. With growing cost of scaled technologies and increased competition in the market, it is also mandatory to reduce the development cycle. One way to do so is to develop accurate pre-silicon concepts by using TCAD simulations in order to understand the failure mechanism and to get a proper insight of failure levels [3]. The failure of a device under ESD condition has been traditionally linked to rise of temperature because of self heating, which causes intrinsic carrier concentration higher than background doping [4] and takes the device into negative differential resistance (NDR) mode [5]. This eventually leads to onset of filamentation and device failure because of thermal runaway.

The drain extended NMOS (DeNMOS) is a HV device, which can be easily integrated with standard CMOS process in sub 100 nm node technologies. Attributed to shrinking ESD window it is very important to design self protecting I/O devices, since the I/O devices may themselves be prone to failure because of an ESD event. Reliability of DeNMOS device under ESD condition is very critical for its use as an ESD protection device for some HV I/O circuit applications and its use as an I/O device applications. However these devices have been found to be extremely vulnerable to ESD events and till now, several mechanisms have been proposed for DeNMOS failure [6]-[9]. It has been proposed that carrier heating in high field region influences saturation drift velocity and impact ionization, which starts regenerative NPN action and causes second breakdown [6]. Results discussed here were only through 2D simulation, and the 3D filament behavior was not clear. Also the proposed regenerative NPN action in the device was discussed for CDM time domain (1-2ns), whereas the device does not get heated within this short interval of time. These simulation studies also show influence in saturation drift velocity at temperatures higher than 1000 $^{o}$K, which itself is sufficient for the onset of filamentation because of NDR and further thermal runaway. The study does not also discuss about base-push-out behavior. Other studies show that because of space charge limited current, peak electric field shifts at drain contact which causes regenerative avalanche injection. This again leads to filamentation and device failure [7][8]. A more detailed 3D modeling of filamentation has shown that regenerative turn on of parasitic NPN causes short circuit power dissipation and leads to an enhanced heating and filamentation [9]. However, a complete picture of the transient device behavior during base pushout and the various phases of filamentation based on 3D simulation studies is still missing.

Works till now do not also give a proper understanding of various phases of filament and a clear and correlated understanding of device failure during ESD event. For the first time, we present a critical study of STI type DeNMOS device under ESD conditions. In this work, a clear and correlated picture on impact of base-push-out, space charge buildup, regenerative NPN action, various phases of filamentation and thermal runaway is presented. Further, we presented a modification in the device layout to achieve improvement (~2.5X) in failure threshold ($I_{T2}$).

## II. EXPERIMENTAL AND SIMULATION RESULTS

A thin gate oxide, drain extended NMOS (DeNMOS) device with STI under gate-drain overlap, as shown in Fig. 1, is processed in state-of-art sub 100 nm node CMOS technology. Figure 2 shows that the device exhibits a failure at very low current ( 1 mA/ µm – 1.7 mA/µm) even in the presence of gate bias or source resistance unlike in [7] [9]. Oscillations in moderate current branch of TLP characteristics show two different stable states for the device (fig. 2), in which one state tries for deep snapback and the other state tries to move into the high resistance branch. No change in leakage occurs in this regime. Finally these two states are getting balanced into high resistance branch causing the device failure. The IV characteristic has been checked to be reversible for stress current values up to 90% of It2.

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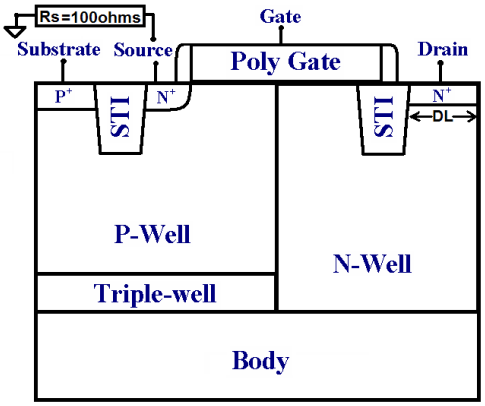



**Figure 1:** DeNMOS device under study. Figure shows the one sided structure (simulated). Actual structure on silicon has folded geometry where drain (N-Well) region is shared between two fingers.

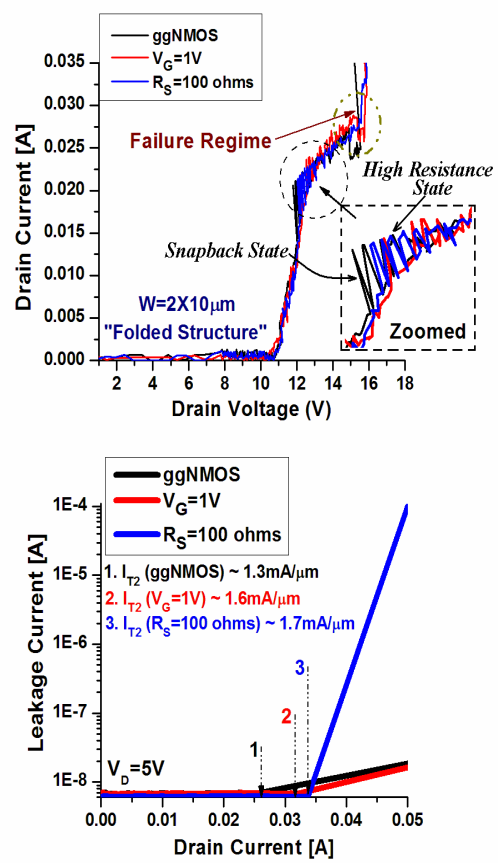



**Figure 2:** Various Experimental TLP (Left) and leakage (right) characteristics of DENMOS device, failing at early current. Only small improvement in $I_{T2}$ was observed by using gate bias or source resistance.

The failed device (width=50 μm) was physically characterized using SEM, which is shown in figure 3. The failure analysis result (SEM image) proves catastrophic failure of device because of filamentation and self heating. It also validates the location of filament and hot spot, which is modeled further through 3D device simulations.

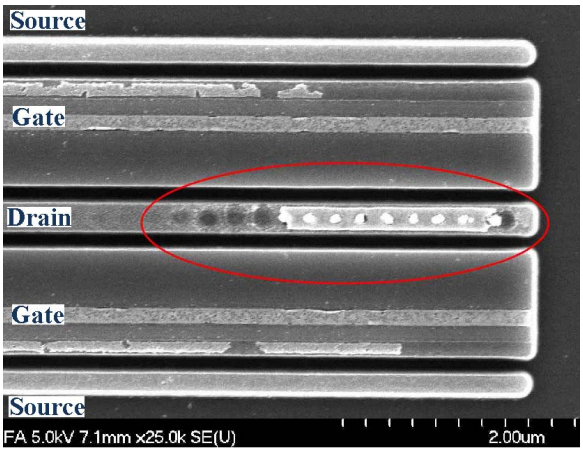



**Figure 3**: SEM image of failed device. Figure shows failure analysis results, which proves catastrophic fail of device because of filamentation and self heating. Figure also validates the location of filament and hot spot, which is modeled further through 3D device simulations.

Figure 4 shows simulated TLP characteristics for devices having different drain diffusion length (DL). The device having lower DL (high current density in N-Well) leads to an early base pushout and device failure with a deep snapback where as the device having longer DL (low current density in N-Well) has no base pushout (follows high resistive branch) and survives higher currents.

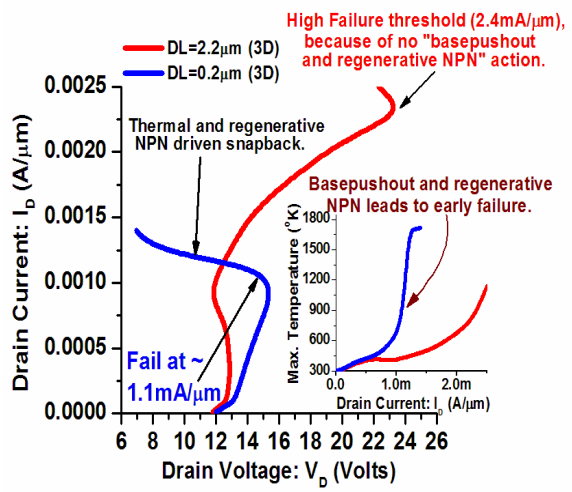



**Figure 4**: Simulated TLP (3D) characteristics of DENMOS device having different drain diffusion length (DL). We find that the devices having higher DL survives up to higher currents.

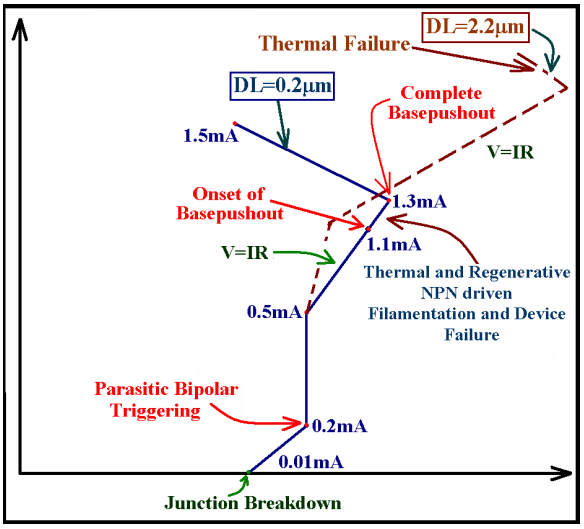
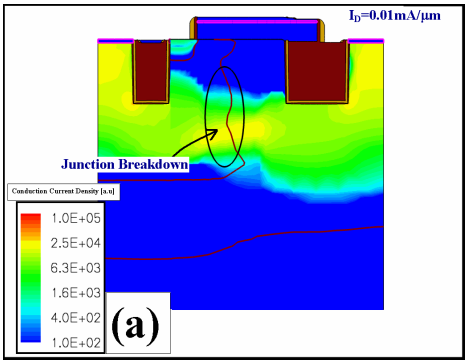



**Figure 5**: Approximated TLP characteristics of DENMOS devices having DL=0.2µm and DL=2.2µm, shows device behavior at different current (per µm) regime.

Figure 5 gives an explanation for the behavior of the two different devices types:

**1.** ***Junction Breakdown*****:** The initial current flow through the device is because of junction breakdown. Figure 6 shows current density contours at low current (< 0.1mA/µm). Maximum fraction of forced current at drain (collector of NPN) terminal moves out through substrate (base of NPN) contact, which proves the dominance of junction breakdown in conduction at low TLP currents. Absence of source (emitter of NPN) current in the contours show that the parasitic bipolar is yet not triggered.

**2.** ***Bipolar Triggering*****:** Figure 7 shows the triggering nature of parasitic bipolar in the DeNMOS device considered for this work. Onset of current flow through source (fig. 7a) shows that parasitic bipolar is turned on at moderate currents. At higher currents (fig. 7b) most of current flows through emitter (source) of parasitic bipolar, whereas base (substrate) current is defined by β of NPN. The slope of TLP characteristics increases at moderate current (defined as region V=IR) because of rise in snapback (bipolar) resistance at high temperature.



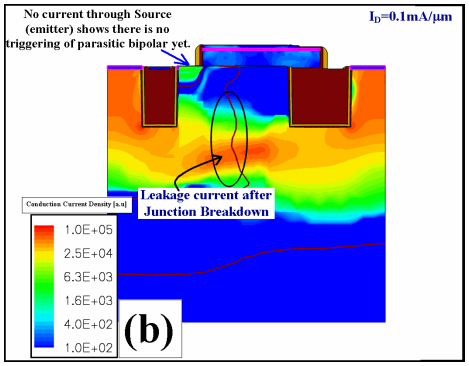




**Figure 6:** Conduction current density (a) At $I_D$=0.01mA/µm (b) At $I_D$=0.1mA/µm. Initial current flow through device is dominated by junction breakdown, whereas the parasitic bipolar is yet not triggered at 0.1mA/µm.

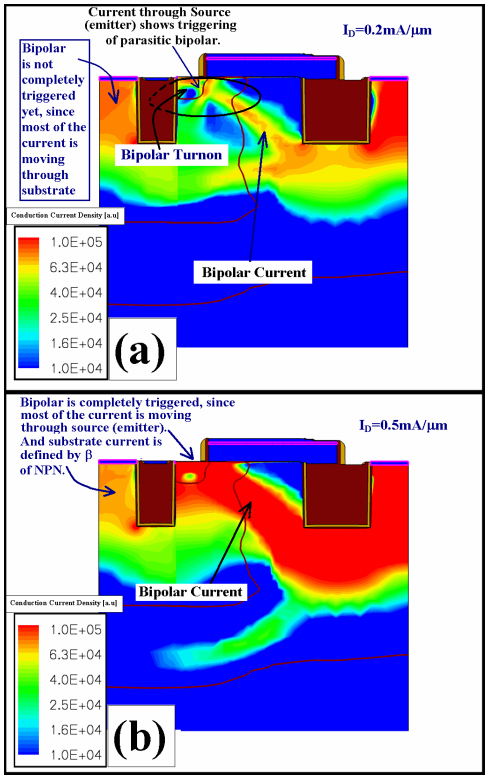



**Figure 7**: Conduction current density (a) At $I_D$=0.2mA/µm (b) At $I_D$=0.5mA/µm. The parasitic bipolar is triggered at 0.2mA/µm. At higher currents base (substrate) current is defined by β of NPN.

**3.** At the ***onset of base pushout*** driven snapback, devices having lower and higher diffusion length (DL) behave differently. The devices with smaller DL suffer from high current densities which drives them into early base pushout causing a thermal failure. The devices with a larger DL assume a high ohmic state until they fail at higher current density without showing a base push-out. Figure 8 shows the onset and complete base pushout of DeNMOS device for the case of lower DL. At a forced TLP current of 1mA/µm there are high fields at N-well-to-P-well junction as well as high fields under the drain diffusion ($N^+$) region. This shows the onset of base pushout. The high field at

the junction was washed and further shifted (at 1.3mA/µm) under drain diffusion, which shows a complete base pushout. Figure 8 shows the current dependence of base pushout behavior, while transient nature of this interesting behavior is also studied in the later part of this work.

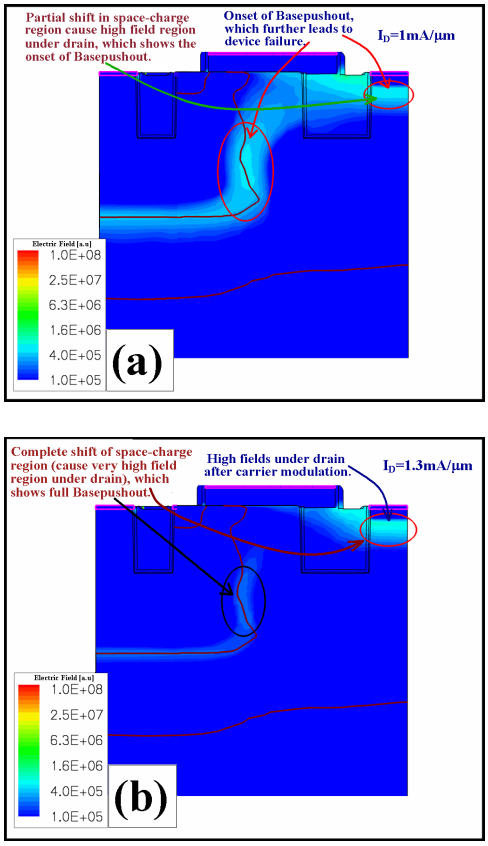



**Figure 8:** Electric Field (a) At $I_D$=1mA/µm (b) At $I_D$=1.3mA/µm. Shows the onset of basepushout at 1mA/µm. After basepushout, there is a significantly high electric field under drain ($n^+$) contact.

The observed TLP behavior (fig. 2a) of the investigated folded double-finger structure (as clear from SEM image) can be explained as follows. The drain diffusion is shared between two fingers. Initially only one finger is turned on. At moderate current this finger moves into the base pushout regime which causes regenerative NPN action. In this voltage regime, the second finger might trigger as well, which reduces the overall current density. In this case both fingers are operating in a state without base pushout exhibiting lower absolute resistance but higher differential resistance (similar to the case of larger DL). This is seen as a bi-stable state in the IV-characteristics. At higher currents, the device stabilizes into a high resistance state because of lower current density.

## II. FAILURE MECHENISM AND 3D DEVICE MODELING

Before we start discussing about failure mechanism, it is important to understand the definition of failure threshold and thermal boundary conditions in this work. Failure threshold ($I_{T2}$) is the forced TLP current at which the maximum temperature inside the device goes above 1500 K. We choose 1500 K since it is very close to melting point of Si and the used electrothermal model (UniBo2) is not modeled beyond this temperature. To achieve proper thermal boundary conditions, we extended the device boundaries by 5 µm and defined 300 $^oK$ of thermal boundary condition at the surroundings of the device. The extension was done in such a way that it does not affect the electrical behavior of the device. We choose 5 µm since thermal diffusion (in Si) length for 100ns (HBM) is 3.3 µm [3].

Figure 9 shows the carrier velocity and the corresponding temperature with respect to forced TLP current. The carrier velocity in the high field region was extracted from 2D device simulations. As claimed in [6], carrier velocity significantly drops down at failure levels. In other words, the device has failed because of drop in saturation drift velocity, which eventually leads to a regenerative NPN action. We found that there is no significant fall in carrier velocity at higher currents at which device fails. This means that carrier velocity plays no role in the filamentation and device failure.

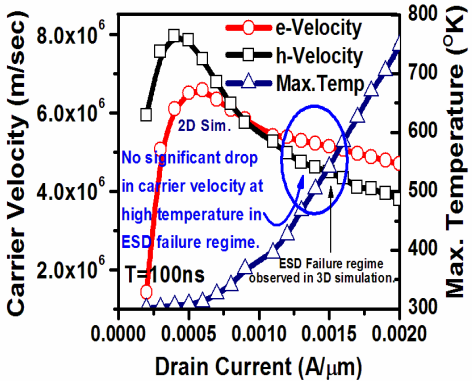



**Figure 9:** Variation of carrier velocity and maximum temperature with respect to drain current. No significant drop in carrier velocity was observed from 2D simulations for higher current at which device fails.

The studies done in previous DeNMOS works had not modeled the transient behavior of device during 100nsecs of HBM event. Proposed model in [9] says device failure at the onset of bipolar triggering (bipolar snapback). It was proposed that bipolar snapback (because of regenerative NPN action) leads to a dissipation of energy stored in junction capacitor, which eventually leads to a filament formation. We calculated that the energy stored in junction capacitor is in the range of pico-Joules, which is not sufficient for device failure. All these contradictions point to a need for understanding transient behavior of the device at failure current.

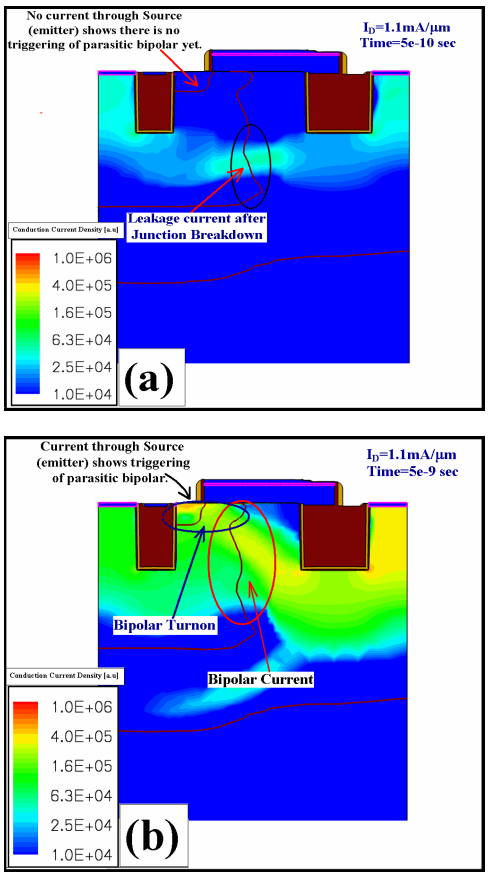



**Figure 10:** Conduction current density (a) at time=0.5ns (b) at time=5 ns for failure current. The junction breakdown happens at 0.5 ns whereas the parasitic bipolar is triggered at 5ns.

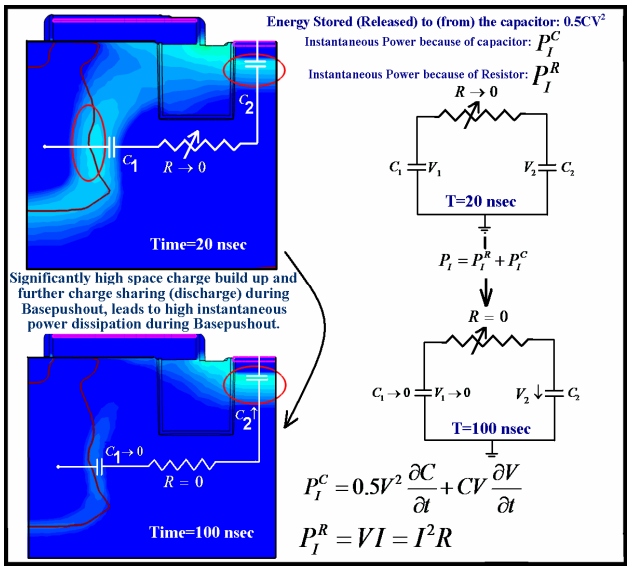



**Figure 11**: Figure shows model for space charge buildup and further discharge, which cause high instantaneous power dissipation during Base pushout. It also shows the transient nature of Basepushout behavior.

Figures 10 (a) and (b) show the device behavior at the failure current having a junction breakdown at 0.5ns and bipolar triggering at 5ns respectively. Further after 20 ns, as shown in figure 11, at higher currents the onset of base pushout causes a significantly higher space charge buildup in the device. It was found that the buildup of a space charge region leads to a formation of very high capacitance during the first 40ns, which stores very high amount of energy (unlike the energy stored across junction capacitance presented in [9]). The stored energy was dissipated in silicon, which significantly exceeds the V·I component as shown in figure 12. This phenomenon was not observed at lower currents i.e. before base pushout.

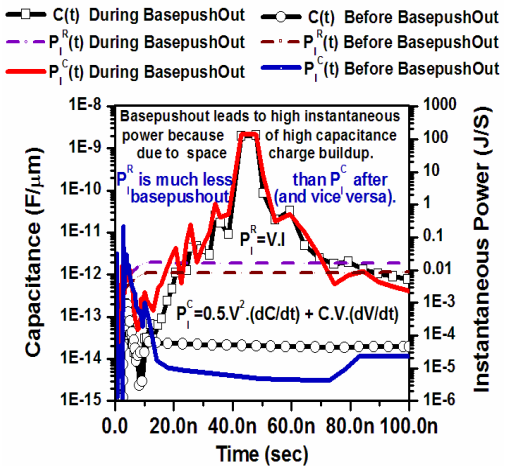



**Figure 12**: Figure shows Capacitance (t) and instantaneous power dissipated (stored) by various parasitic (electrical) components before and after Base pushout.

Figure 13 shows 3D distribution of current density inside the device (i.e. along the device width at source and drain separately), which shows a unique filament behavior at drain and source side for different times.

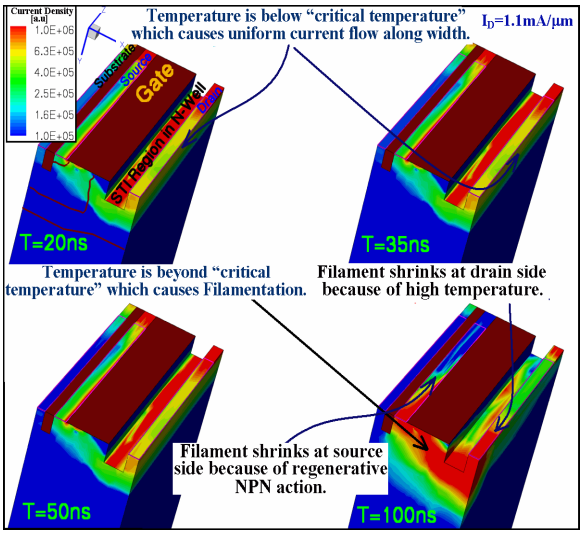



**Figure 13**: Current density at different times extracted from 3D simulations (DL=0.2μm). First filament starts shrinking at drain side because of temperature rise, which leads to regenerative NPN action (due to the high fields after basepushout) and further causes filament shrink at source side.

Figure 14 shows an exponential increase in the drain hole current at higher times for failure current, which shows the presence of regenerative NPN action. This regenerative NPN behavior was not significant in 2D simulations and was not observed before base pushout in 3D simulations. The regenerative NPN action results from high electrical field and consequently a high avalanche generation along the filament at drain diffusion. A large hole current is generated which turns on the NPN. We find that the regenerative NPN action starts at a lattice temperature higher than 1000 K, which itself is a sufficient temperature for formation of a current filament at drain. The regenerative NPN action leads to shrinking of the current filament at source side (Fig. 13).

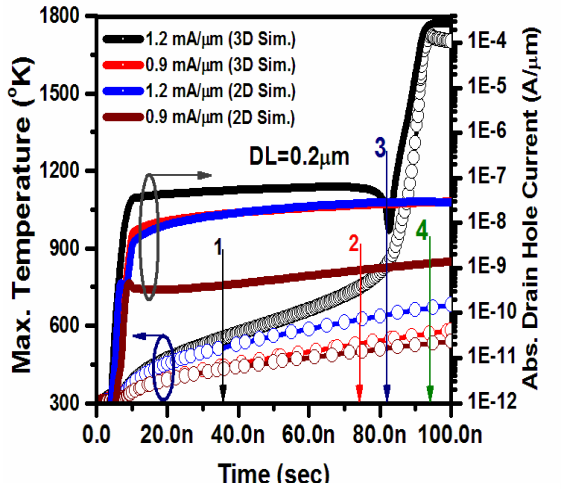



**Figure 14**: Hole current and max temperature at different current levels, extracted from 2D and 3D simulations. 3D simulations for lower currents and 2D simulations show absence of regenerative NPN action, whereas regenerative NPN action is clear for higher current (beyond onset of base pushout-3D) because of an exponential rise in the hole current. *Figure also describes various phases of filament formation.1: Onset of Base pushout and space charge buildup,2: Onset of filamentation because of high temperature, 3: Filamentation caused temperature rise that starts regenerative NPN action and 4: Device failure because of thermal & regenerative NPN*

In summary we find following unique filament behavior at drain and source side during 20-100ns, considering a current sufficient to cause base pushout, which finally leads to device failure:

1. ***Onset of base pushout***, which leads to high space charge buildup.
2. ***High energy storage*** *in space charge region and its* ***dissipation into silicon.***
3. ***Heating,*** *because of high fields after basepushout,* ***leading to a onset of filamentation at drain side.***
4. *Filamentation leading to a* ***further temperature rise***.
5. Onset of ***regenerative NPN action*** *due to high electrical fields and high current density in filament.*
6. *Heating at drain diffusion because of filament shrink at drain side that causes regenerative NPN action. Furthe, the regenerative NPN action* ***shrinks the filament at source side.*** *These two mechanisms work together and act like a positive feedback to each other. This leads to a fast temperature rise within a short time (fig. 14).*
7. ***Device failure*** *because of thermal and regenerative NPN based filamentation.*

Even though the regenerative NPN action was observed, the dominant mechanism for device failure is exceeding the melting temperature. The regenerative NPN action only acts as an extra positive feedback after onset of filamentation, which causes shrinking of current filament also at the source side leading to rapid confinement of the current filament during short time scales. Figure 15 validates location of hot spot and failure because of excessive melting temperature, as observed in SEM images (fig. 3).

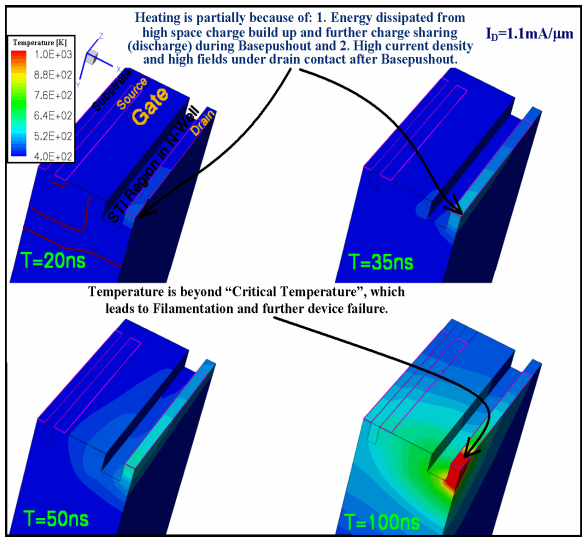



**Figure 15:** Lattice Temperature at different times extracted from 3D simulations (DL=0.2μm).

## IV. FURTHER IMPROVEMENT IN FAILURE THRESHOLD

Figure 4 also shows improvement in failure threshold by extending $n^+$ drain diffusion (DL=2.2 μm) and drain contact (no change in ballast resistance) all over the drain diffusion. Increasing the diffusion area (increasing DL) leads to lower carrier density in the N-well region underneath the drain diffusion (Fig. 16). Reduction of carrier density in N-Well shifts the onset of base pushout to higher currents. Since there is no base pushout before device failure, the high field is located at the well junction, which is much lower than the peak electrical field under the drain contact ($n^+$) of a device showing base pushout (for DL=0.2μm). Figure 16 depicts the filament behavior of the device having larger DL. Figure 17 shows that initially the heating takes place at the well junction, which was quite relaxed as compared to the case of DL=0.2 μm (i.e. device having base pushout) because of less electric fields and less current density. Figure 18 compares the maximum temperature and hole current

in both the devices at failure current. Because of the absence of base pushout and regenerative NPN action, the device with larger DL exhibits a smoother increase in temperature until fail. At high temperatures, only an extended filament is formed at the drain side (fig. 16) because of lack of regenerative NPN action. At source a uniform current distribution is found for the simulated device. Due to reduced current confinement in the filament a higher It2 was achieved.

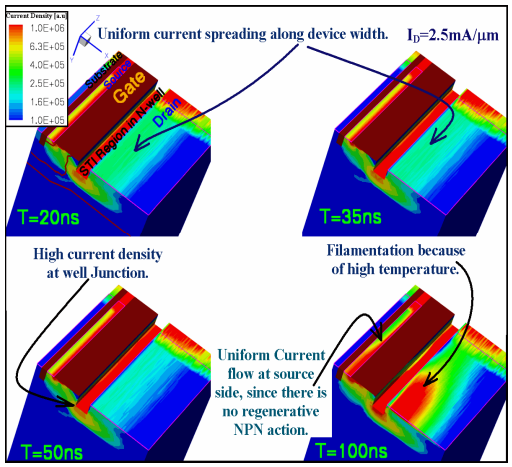



**Figure 16:** Current density at different times extracted from 3D simulations (DL=2.2μm). Filament shrink at drain side is because of temperature rise, whereas absence of regenerative NPN action (due to the lower fields in the absence of base pushout) causes uniform current density at source side.

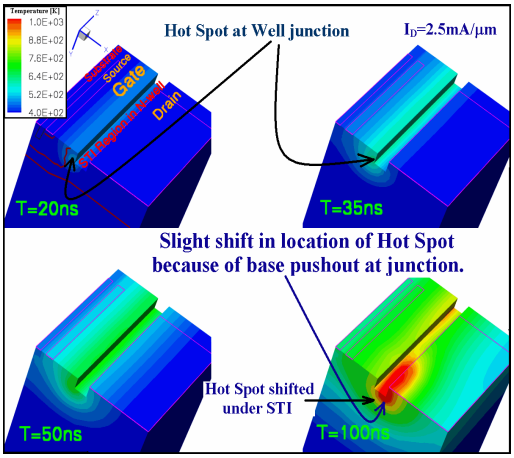



**Figure 17:** Lattice Temperature at different times extracted from 3D simulations (DL=2.2μm).

The device intrinsic performance i.e. $R_{ON}$ (On resistance), $V_{BD}$ (Breakdown voltage), $C_{GG}$ (Gate capacitance) and $C_{DD}$ (Drain capacitance) was found unchanged for DL=2.2μm case, so no loss of mixed signal/RF performance of the device is observed when used in I/O circuits. Further we found that DL=0.6μm is sufficient enough to shift the onset of base pushout to higher currents in order to achieve high It2 values.

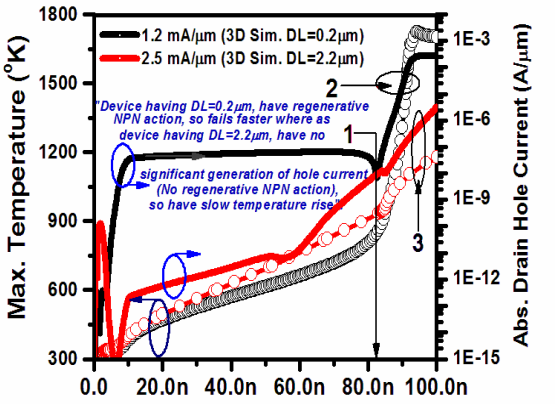



**Figure 18:** Hole current and maximum temperature at failure current level of device having basepushout (DL=0.2μm) and no basepushout (DL=2.2μm) before filamentation. *1: Time at which maximum temperature and hole current are same for both the devices, 2: Regenerative NPN action leads to fast formation of filament and 3: Absence of Base pushout causes lower electric fields, which leads to a lower impact ionization generated holes. Since hole current is negligible, there is no regenerative NPN action*

## V. CONCLUSION

We found that the onset of filamentation is caused by elevated temperatures at drain side. The degree of confinement of the filament is strongly dependent on the existence of a regenerative NPN action. In a drain extended MOS a strong regenerative NPN is found to occur along with a base pushout, which results in a low It2. Additionally, a high space charge buildup during base pushout contributes to an early failure. Avoiding the base pushout by decreasing the current density under the drain diffusion increases the failure current significantly. This can be achieved by choosing a sufficient length of the drain diffusion area.

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