Highly Resistive Body STI NDeMOS: An Optimized DeMOS Device To Achieve Moving Current Filaments For Robust ESD Protection

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Abstract: *A novel DeMOS device with modified body and source region in grounded gate (gg) NMOS configuration for ESD protection is proposed. Detailed 3D simulations indicate a high failure threshold because of moving current filaments and self-protection from gate oxide breakdown, even for fast transients. A detailed physics of second basepushout and moving filaments is discussed.*

I. INTRODUCTION

For Integrated Circuit technology, as the technology advances towards sub 100 nm node, the Electro-Static Discharge (ESD) protection design is becoming more and more critical. In sub 100 nm node technology various devices compatible with high IO voltages have been proposed for ESD protection, but they all have some drawbacks, e.g. ggNMOS has relatively low second breakdown current (I_{T2}), SCR devices does not switch fast to protect against charged device model (CDM) stress and diode protection does not allow local clamping [1]. The trigger voltage of ggNMOS can be reduced below breakdown voltage of I/O device by using gate biasing [2], but this cause higher heating and eventually lower failure thresholds. Recently it was shown that moving current filaments improves DMOS performance under high current stress and hence excellent ESD robustness can be achieved [3]. Drain extended MOS devices (DeMOS) have very low failure threshold because of early filamentation, which was attributed to regenerative NPN action [4]. Still the optimization issues of DeMOS devices for robust ESD protection and detailed physics of filament motion is missing. In especially non-moving, localized filaments lead to early fail.

We present an optimized DeMOS device for robust ESD protection. Extensive 2D and 3D simulations show that device gives very high failure threshold (>10mA/µm) along with other improvements. The device is self protected from gate oxide breakdown, even in the presence of fast switching. It does not show any degradation of the failure threshold in the presence of gate biasing. Moving current filament found in the proposed structure improves the ESD robustness. Physical behavior of device in different regions of snapback curve is discussed. A new phenomenon of soft snapback in high current regime is observed and its physics is discussed. The behavior and the various necessary conditions in the device for filament motion are studied from extensive 3D simulations.

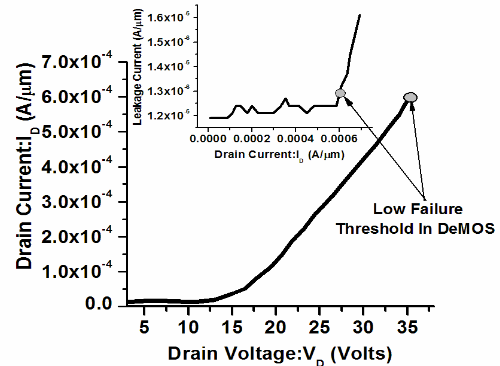
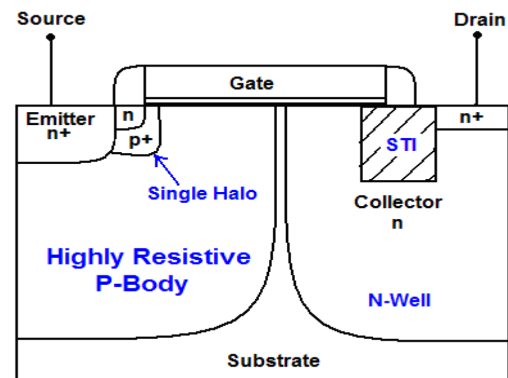


Figure 1: Experimental TLP characteristics and leakage analysis of a non-optimized reference grounded gate DeMOS device.

II. DEVICES & EXPERIMENTAL RESULTS

A thin gate oxide drain extended MOS (DeMOS) device with STI under gate-drain overlap is processed in state-of-art 130nm node CMOS technology. STI under gate-drain overlap helps in achieving improved gate oxide reliability. The TLP characteristic of gg-DeMOS is shown in Fig 1, which exhibits a device failure at very low current right at the onset of snapback (~0.5 mA/µm). This fail was attributed to very high heating and regenerative NPN action [4]. To improve the ESD performance a modified structure was analyzed by 2D/3D device simulation (Fig.2). Based on a well calibrated process and device input deck. The IV characteristics of the original device was matched and the optimization of the modified device compatible to IO voltages up to 6 V be proven (Fig 3). The leakage at 6 V is 1 nA/µm.



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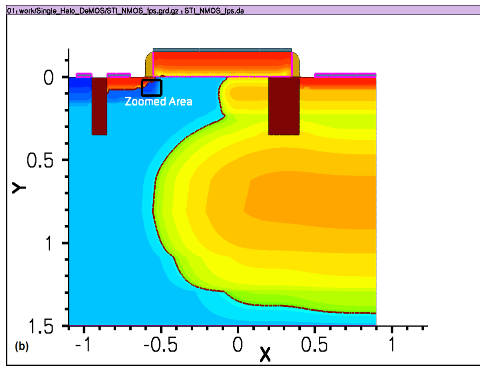

Figure 2: (a) Highly resistive P-Body (HRB) DeMOS, gate and source are grounded. (b) Device after process simulation

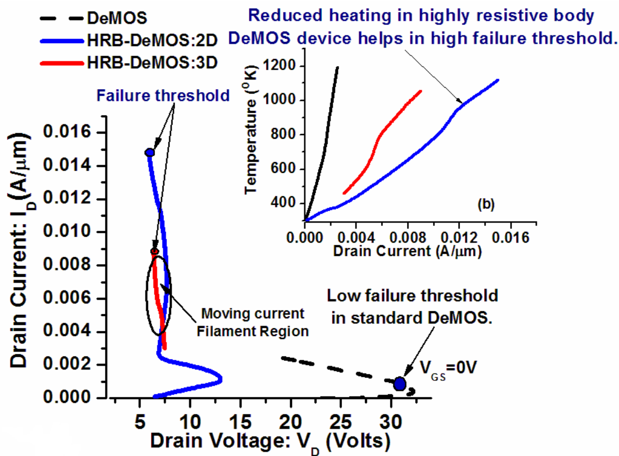

Figure 3: Simulated TLP characteristics of HRB DeMOS and standard DeMOS device in grounded gate configuration.

III. IMPACT OF MODIFIED SOURCE/BODY PROFILE

In proposed device a highly resistive body has been realized using standard process steps (Fig. 2). Triggering speed of NPN device is proportional to β (beta) of transistor, which depends on the emitter-to-base electric field (defines the drift nature of excess carriers from emitter to collector) and base doping (defines the recombination in base). Incorporating a single halo implant forms graded base in NPN device, which causes a high electric field at the emitter-base junction. This improves the drift of carriers from emitter to base, which in turns improves the bipolar gain. Similarly a highly resistive body or very low body (base) doping helps in reducing the excess carrier recombination in base improving the bipolar gain. Also, since the NPN triggering occurs by impact ionization (II) generated holes, highly resistive body helps in raising the body potential even in the presence of very less no of II generated holes. These all eventually lead to an improved parasitic bipolar effect before charge modulation occurs, which further helps in achieving moving current filaments (as discussed in chapter V). At higher current the more compact dimension of this device proves to be an advantage.

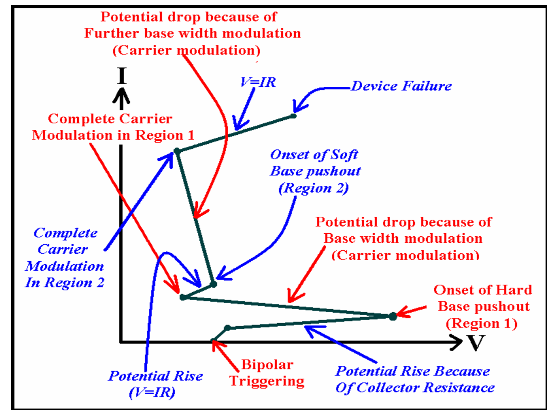

Figure 4: Physical behavior of device at different current regions of I-V curve.

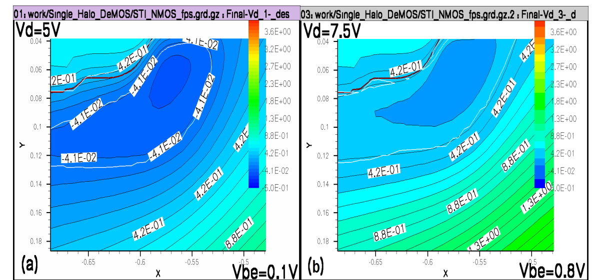

Figure 5: Electrostatic potential contour at different drain bias. Figure shows triggering of parasitic bipolar below at V_D=7.5V (Zoom in of Fig 2b).

IV. SIMULATION RESULTS

Fig 4 summarizes the various operational states seen for this device when current is forced in a TLP set-up.

A. Parasitic Bipolar Triggering: Figure 5 shows the potential contours (for the zoomed area shown in fig. 2a). The plot proves that a V_{BE} > 0.7 V, and therefore triggering of parasitic bi-polar, was achieved at V_D ~ 7.5V (Fig 5b). In the IV characteristic no snapback is seen at this point due to the high resistive drain. In contrast the drain voltage continues to increase significantly.

B. Hard Base Pushout: Figure 6 shows the electron density at different current levels and background doping, in the direction of current flow, below STI. At lower currents the electron density is less than the background doping concentration, which becomes higher beyond 1mA. This shows the onset of base push out at 1mA/μm and further carrier modulation of N-well region at 3mA/μm. This leads to a deep snapback from 13 V to about 7 V (Fig. 3). Both the bipolar triggering and base pushout can be found in the transient waveform (Fig. 7). Because of high β the bipolar triggering is very fast (10-20 picoseconds). At later times (depending on TLP current) the parasitic bipolar gets into base pushout. Figure 8 shows the electric field in the direction of current flow, at different time and at different currents which verifies the basepushout w.r.t time and current as discussed above.

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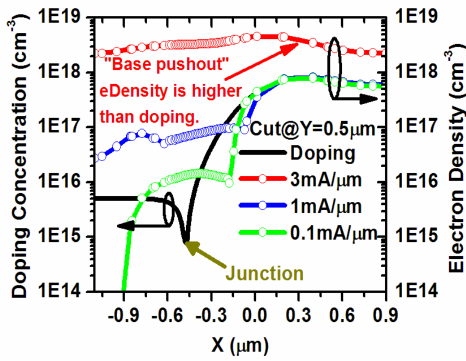

Figure 6: Electron density at different drain currents. Onset of base pushout was observed at 1mA/um. But in the graph 3 mA/µm is indicated as base pushout. Add the depth of the cut. In the caption as well.

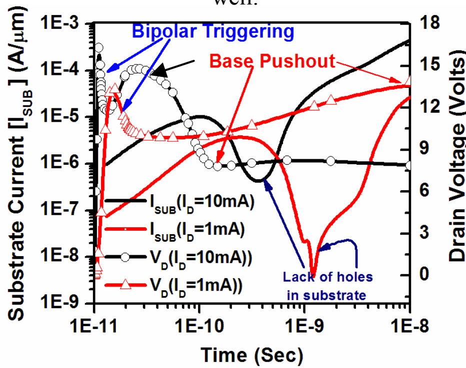

Figure 7: Drain voltage and substrate current at low and high current levels for trapezoidal TLP with 10 ns rise time. Base push arrow for 1 mA/µm should point more towards the peak.

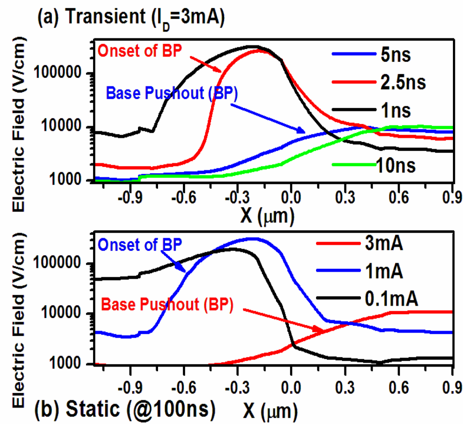

Figure 8: 1D lateral electric field distribution showing base pushout behavior (a) At different times during TLP at I= 3mA /µm (b) At different currents in steady state after 100 ns.

C. Soft Base Pushout: An unusual second snapback at higher currents is observed. This is attributed to the base pushout (in the vertical direction along the flow of carriers) in deep highly doped part of the retrograde N-well and underneath drain (n^+) region. Figure 9 gives a clear picture of carrier modulation in vertical direction. At medium current density, where the lowly doped region of the nwell directly underneath the STI has already gone through the base pushout, the electron density is still lower than the background doping in deep N-Well region and below n^+ region. At higher currents, more carriers are forced into deep N-Well, which leads to carrier modulation and eventually a second base pushout. This leads to soft snapback in the IV characteristics (fig.10). Figure 11 shows the I-V (TLP) plot for three different STI depths (underneath gate-to-drain overlap). It indicates that for devices without STI under the gate drain edge, the onset of soft snapback is at much higher currents as compared to device having deep STI (350nm) and short STI depths (100nm).This shows that STI enforces flow of carriers towards deep N-Well region. Figure 12 depicts the electron current density contour at 6mA/µm. A flow of carriers towards deep N-Well because of STI (underneath the gate drain edge) can be seen. To model this behavior by analytical means an approximated N-well doping profile in the direction of carrier flow was considered (Fig.13).

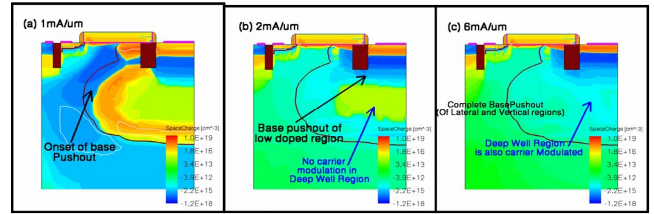

Figure 9: Space charge density contours at different current levels. It shows that first lowly doped region of the nwell gets carrier modulated followed by highly doped region of the deep nwell region. This causes a double snapback in the IV characteristics (fig.11).

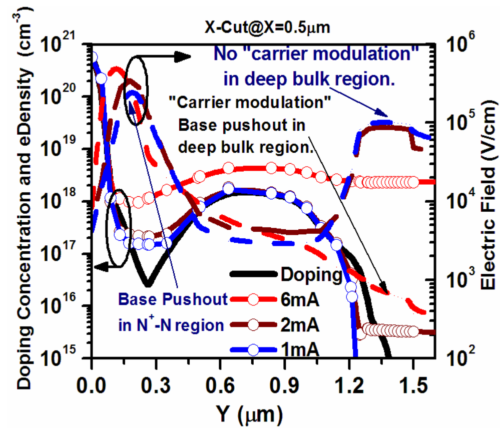

Figure 10: Electron density and 1D electric field distribution along vertical direction, underneath drain (n^+) region.

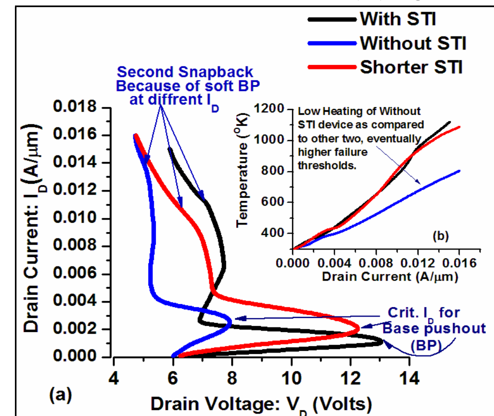

Figure 11: TLP characteristics of HRB DeMOS with STI, without STI and with short STI.

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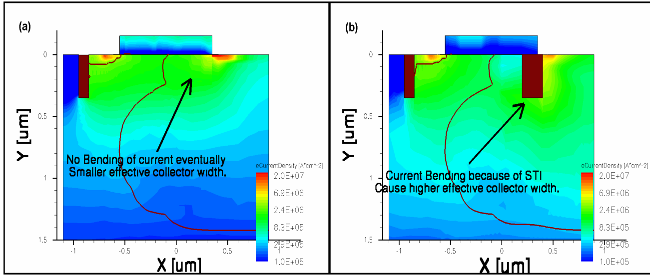

Figure 12: Electron current density contour (a) Without STI (b) With STI. It shows that STI pushes carriers towards deep well region.

The collector voltage at the onset of base pushout was modeled as equation (1) [5]. From a first order approximation, the change in collector voltage during hard and soft base pushout (δV1 and δV2) can be modeled as equation 2 and 3, respectively. Since W_{C2} is less than W_{C1} (Fig. 13), the potential drop because of second snapback is less as compared to the first snapback.

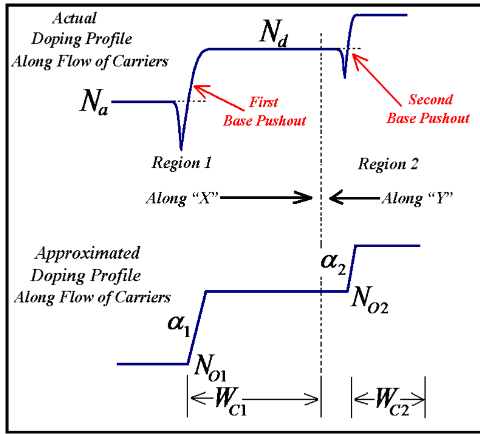

Figure 13: Actual and approximated doping profile in the direction of flow of carriers.

$$V = \frac{qW_c^2\{3(N_O - n) + \alpha W_C\}}{6\varepsilon} \quad \text{......... (1)}$$

$$\partial V_1 = \frac{2qW_{C1}[\partial W_{C1}\{3(N_{O1} - n) + \alpha_1\}]}{6\varepsilon} \quad \text{....... (2)}$$

$$\partial V_2 = \frac{2qW_{C2}[\partial W_{C2}\{3(N_{O2} - n) + \alpha_2\}]}{6\varepsilon} \quad \text{........ (3)}$$

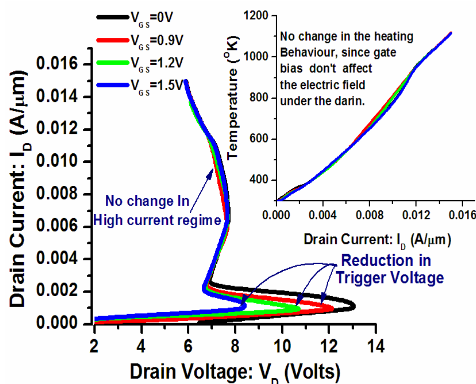

Figure 14: Impact of gate biasing on TLP characteristics.

D. Impact of Gate Bias: To further improve the turn–on behavior and voltage clamping the impact of gate bias was investigated (Fig.14). The trigger voltages could significantly be reduced without increase of peak temperature or change in failure threshold.

V. MOVING CURRENT FILAMENTS

The device forms current filaments after base pushout. Filaments either move along the device width or are localized, which leads to fails at low current levels [4]. In the proposed device moving filaments occur. Figure 16 and 17 shows the motion of peak current density and peak lattice temperature along the device width at different times respectively. The beneficial filament motion in the device is attributed to fast bipolar switching of the device. *In addition to a temperature gradient [3], filament motion requires the following conditions:*

*1. **Ultra fast bipolar switching behavior.***
*2. **Base pushout.***
*3. **Filament shrinking at source side.***

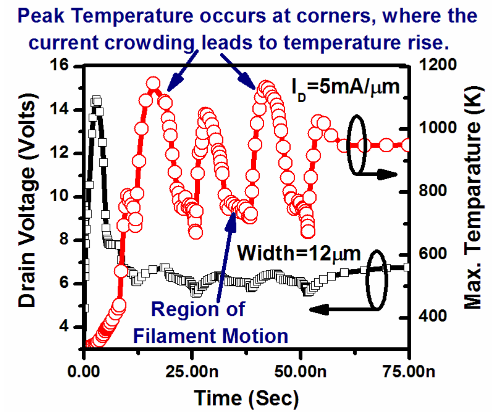

Figure 15: Drain voltage and maximum temperature during 3D TLP simulation. Oscillations in drain voltage are an indication of moving current filaments.

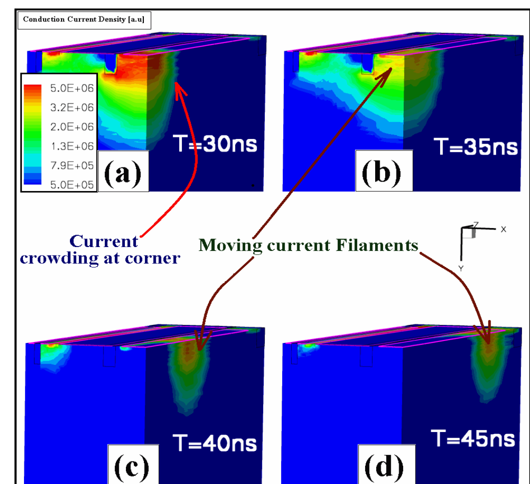

Figure 16: Conduction current density (A/cm^{-2}). Moving current filament along device width at high currents.

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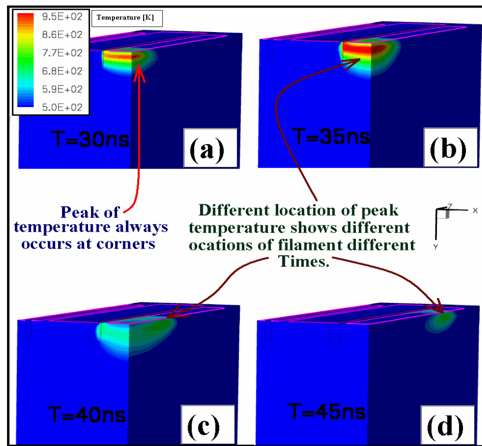

Figure 17: Different location of peak temperature (^{o}K) along device width at high currents because of moving filaments.

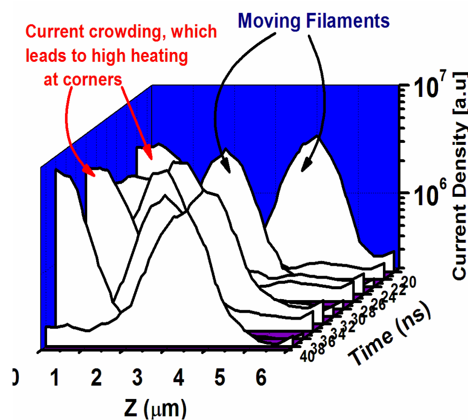

Figure 18: Current density (A/cm^{-2}) profile along device width at high current at different times shows moving filaments.

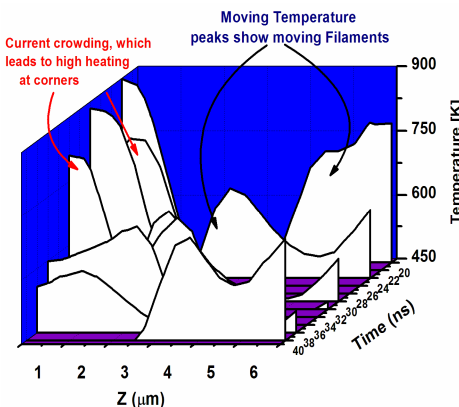

Figure 19: Temperature (^{o}K) profile along device width at high current at different times.

A filament motion starts when speed of bipolar switching is higher than rate of heating in the device. Figure 18-20 shows that filament motion occurs in following manner:

1. ***Onset of Filamentation after base pushout*** because of high heating along one of the corner of device.

2. Rise of temperature leads to filament shrink at drain side. This starts the regenerative NPN process, which further leads to ***filament shrink at source side.***

3. ***High temperature reduces impact ionization*** inside the filament.

4. This causes slightly higher impact ionization generated carriers in the adjacent bipolar. ***Because of highly resistive P-Body, the device needs a very small number of carriers to trigger the parasitic bipolar. This eventually helps in achieving ultra fast triggering of the adjacent parasitic bipolar and the filament shift to adjacent location before the device failure.***

5. While the filament moves along the device width the device is heated uniformly. Only at the corners a transient temperature peak occurs because of current crowding before the filament is reflected.

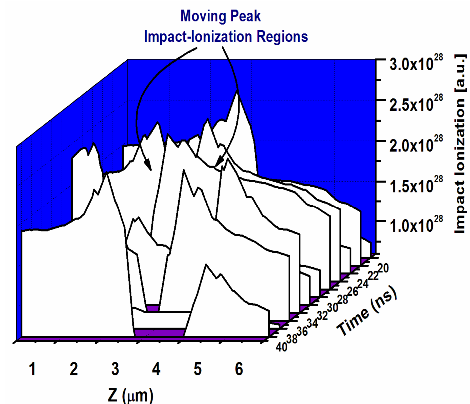

Figure 20: Impact Ionization (cm^{-3}sec^{-1}) profile along device width at high current at different times shows signature of moving filaments.

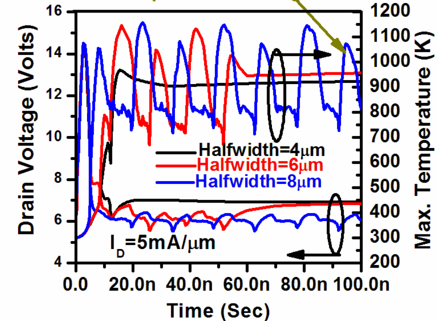

Figure 21: Impact of device width on filament motion shows increase in device width improves its robustness.

Figure 15 shows the transient characteristics during filament motion. The maximum temperature and drain terminal voltage oscillates with respect to time, which is a signature of filament motion. The high temperature peaks are because of current crowding at corners. Temperature rise tends to degrade the impact ionization rate To maintain avalanche generated holes in the substrate electrical field or eventually voltage has to increase, which leads to an experimentally observable oscillation in the voltage waveform [3].

Figure 21 shows transient characteristics of devices having different device widths. For lower device width the peak temperature (and drain voltage) saturates at lower times whereas for higher widths there is a continuous oscillation of peak temperature (and drain voltage) up to 100ns. ***It was found that the filament in the device having smaller width saturates at***

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corner and stops moving at shorter times whereas current filament, in the device having higher width, was continuously moving up to longer times. This behavior is attributed to fast rise in average temperature of the device having lower width as compared to device having higher width. In a device having low width, the filament moves from one corner to the other and come back in less time as compared to time required in a device having higher width. This causes lower rate of cooling. This shows that the ***ESD robustness of the devices showing filament motion increases by increasing device width up to a certain limit where it saturates***. Figure 22 shows transient characteristics for various simulated layouts of HRB-DeMOS device to understand the impact of layout on moving filament behavior. Increasing contact hole density or ***variation of the corner region do not have significant impact on filament motion***.

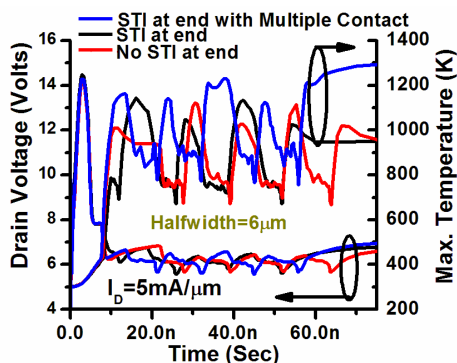
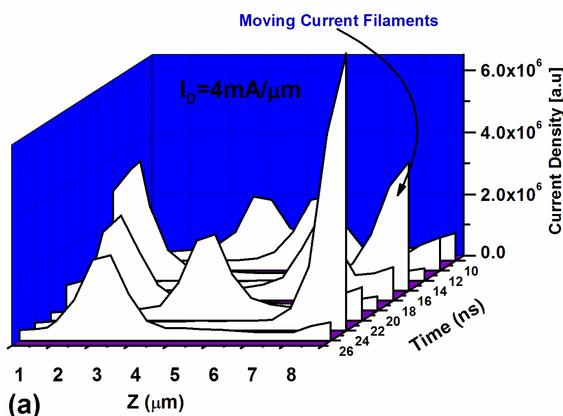


Figure 22: Impact of different layouts on filament motion shows filament motion is independent of device layout.

Figure 23 shows the ***presence of filament motion even in the case of tight thermal boundary conditions (worst cooling).*** Tight thermal boundary conditions were achieved by increasing thermal resistance parameter in the TCAD simulation**.** The filament motion is not influenced for the considered device width . However, the failure threshold is reduced because of faster temperature rise.



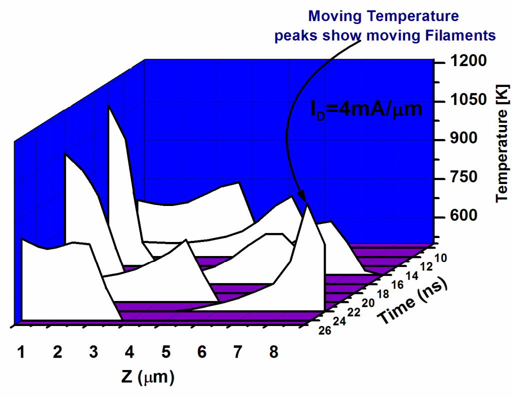


Figure 23: (a) Current density (A/cm^{-2}) and (b) Temperature (^{o}K). Figure shows the impact of tight thermal boundary conditions on filament motion shows filament motion is independent of cooling. Rate of cooling only affect the failure threshold because of high rate of temperature rise. (Tight boundary conditions were achieved by increasing thermal resistance.)

VI. CONCLUSION

Standard drain extended MOS (DeMOS) devices fail at the onset of snapback caused by base pushout . Regenerative NPN action and high heating lead to formation of localized filaments. This failure mechanism is a danger intrinsic to any device with lowly doped drain (collector). To optimize the robustness of DeMOS devices a highly resistive body is introduced. This leads to a significant improvement in parasitic bipolar triggering, which causes the filaments to start moving. An insight into physics of filament motion and second base pushout is has been presented. By achieving moving filaments instead of localized ones it is predicted that the device can sustain the snapback and the current density at fail increase by one order of magnitude (> 15 mA/μm). Introducing gate bias allows to tune the trigger voltages without degrading the failure threshold. Highly resistive body DeMOS can be used as efficient ESD protection elements for high voltage interfaces in advanced CMOS technologies.

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