FILAMENT STUDY OF STI TYPE DRAIN EXTENDED NMOS DEVICE USING TRANSIENT INTERFEROMETRIC MAPPING

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Abstract: We present filament behavior of STI type DeNMOS devices using detailed Transient Interferometric Mapping experiments and 3D TCAD simulations. Device behavior at different TLP currents is discussed. The impact of localized base-push-out, power dissipation because of space charge build-up, regenerative NPN action and various events during the current filamentation are explored. By uniform turn-on of the device during base push-out the failure current could be improved by more than 2X.

I. INTRODUCTION

Drain extended MOS (DeNMOS) devices used for high voltage I/O applications have been found to be extremely vulnerable to ESD events. Several mechanisms have been proposed for DeNMOS failure [1-4]. Recently we presented a more complete picture of STI type device behavior during the base pushout and the various phases of filamentation based on 3D simulation studies [5]. In order to validate our filament model developed using the TCAD simulations and to get a better insight into the filament behavior, we present the Transient Interferometric Mapping (TIM) [6] data in this work. This paper provides a clear insight into the 3D filament behavior of STI type DeNMOS devices along with a new physical phenomenon observed in these devices, which has not been reported before.

II. DEVICE AND EXPERIMENTAL SETUP

A thin gate oxide, double finger, drain extended NMOS (DeNMOS) device with STI under the gate-drain overlap, as shown in Fig. 1a, is processed in state-of-art 65 nm node CMOS technology. The electrical scheme for device stressing is given in Fig. 1b. TIM method monitors the temperature and free-carrier concentration induced changes in the silicon refractive index with a 1.5µm areal resolution and 3ns time resolution [6]. During the scanning, 30 stress pulses are applied at every scan point.

III. DEVICE BEHAVIOR

The TLP characteristics (Fig. 2) shows that the device undergoes failure at a very low current (~ 1.7 mA/µm). The device behavior before failure can be explained as follows:

1. ***Junction Breakdown*****:** The initial current flow through the device is because of junction breakdown.

2. ***Bipolar Triggering*****:** The parasitic bipolar triggers inefficiently ($\beta < 1$) at lower currents (0.1mA/µm). At moderate currents (0.5mA/µm) a bimodal behavior is detected, which indicates competition in the current distribution between emitter (source) and base (substrate) current of the double finger structure. At even higher current the slope of TLP characteristics increases and the two modes get merge.

3. At the **onset of base push out** driven snapback, device suffers from high current densities which drives it into strong charge modulation and early thermal failure.

IV. RESULTS AND DISCUSSION

A. Pulse-to-pulse instability and bipolar triggering

Pulse-to-pulse instability in the lower current branch of the TLP characteristics shows two different stable states for the device, in which one state tries to cause a snapback (Mode-A) while the other state tries to move into a high voltage branch (Mode-B). Fig. 3 shows that the bipolar triggering is efficient ($\beta > 1$) in Mode-A, whereas it triggers inefficiently ($\beta < 1$) in Mode-B. This behavior can be attributed to a one finger or two finger triggering as shown in Fig. 4. One finger triggering leads to a higher current density at the well junction, causing a higher impact ionization (II), eventually leading to an efficient bipolar triggering. On the other hand, a two finger triggering leads to a relaxed current density at the well junction, which generates fewer II carriers leading to an inefficient bipolar triggering. At moderate currents, both the branches (Mode A & B) merge into a high voltage state (Fig 2), which is attributed to an efficient bipolar triggering (Fig. 5). At moderate TLP currents, higher current density at the well-junction (Fig. 6) leads to excess II carriers, which eventually triggers the parasitic bipolar efficiently.

B. Device behavior at lower currents

Fig. 7 shows that self heating at lower currents in both the modes is identical, whereas the small difference in phase shift is because of the higher current density at well junction in Mode-A. Further, nearly uniform phase distribution along Y axis (Mode-A) proves uniform current conduction (i.e.

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efficient bipolar triggering) whereas a non-uniform distribution (Mode-B) shows inefficiently triggered parasitic bipolar action. Nearly symmetric distribution of phase along the X axis (Fig. 8) regardless of one or two finger triggering is attributed to the location of peak hot spot (i.e. at drain diffusion [5]) which is in the center of two fingers. Uniform diffusion of thermal energy in all the directions (in silicon) leads to a symmetric phase distribution. Fig 7 and 8 also prove that bipolar driven snapback (Mode-A) does not lead to filamentation and device failure.

C. Device behavior at moderate currents

Fig. 9 shows an instant rise in phase shift (i.e. heating) during the initial 40ns (between 0-40ns), whereas it rises gradually during the next 60ns (i.e. 40-100ns). This behavior is attributed to power dissipation because of energy discharge from the space charge region during the initial times, which eventually leads to an excess heating. Further, Fig. 9 (a) shows a uniform conduction along the device width, which is attributed to an efficiently triggered bipolar and (b) a bell shaped characteristics along X axis unlike to triangular distribution found at lower current, which is because of the negative phase components due to excess carriers in the body/pedestal region.

D. Space charge build-up and discharge at higher currents.

According to estimations from the experimental setup (capacitance of external circuit/setup), not more than 10mA of current overshoot is expected during the parasitic capacitance discharge through the device in snapback. A higher current overshoot (i.e. 80-100mA, Fig. 10) during charge modulation driven snapback gives a signature of space charge build up and its discharge after the onset of base push out. The peak overshoot current and the time of snapback depends on the forced TLP current.

E. Localized base push out.

Fig. 11 shows (i) soft snapback and (ii) higher failure threshold (It2 ~ 4 mA/µm), at larger load values (i.e. R_L=3kΩ), unlike the behavior observed in Fig. 2 for low ohmic cases (i.e. deep/hard snapback and failure). Fig. 12 (a) shows the onset of base push out in 2D plane at lower times and (b) & (c) show the non-uniform charge modulation in 3D plane and finally (d) shows the strong filamentation because of localized base push out. Fig. 13 shows (i) deep snapback and early failure when it has a localized base push out (3D simulation) and (ii) soft snapback and higher failure threshold when charge modulation occurs only in the 2D plane (2D simulation). Fig 11-13 can be correlated as uniform charge modulation along the width at higher load line values, which survives the base push out driven "instability/deep-snapback" and leads to a high failure threshold because of relaxed heating. Further-on device behavior under *Pulse-to-Pulse instability* at currents between 0.4mA/µm and 0.8 mA/µm can be elaborated using Fig. 13. At lower currents, when bipolar triggers efficiently (one finger triggering: Mode-A), the triggered finger conducts uniformly along the device width (2D Simulation) and exhibits a slight snapback, whereas inefficient bipolar triggering (two finger triggering: Mode-B) leads to non-uniform conduction along the width (3D simulation) and causes a high voltage state. This qualitatively agrees with the observations in fig. 2 and 11.

F. Regenerative NPN action and its impact.

Negative phase near the drain contact (Fig. 14) proves the presence of excess carrier injection/generation at the drain diffusion, which leads to a regenerative NPN action. Excess carrier injection/generation starts at the onset of base push out and was not found as the dominant cause of device failure [5].

G. Impact of excess charge carriers on phase signal

The particular behavior in the pedestal region of Fig. 9b is explained by the impact of negative phase signal because of excess carrier, which counterbalances the positive phase shift due to heating. Resolving the distribution of the phase signal at higher current in the center of the device, a strong negative component of the phase signal can be detected as well (fig. 14). This is remarkable as it sustains during the full duration of the pulse and can be simulated by TCAD including models for TIM (Fig.15). At the end of the pulse the phase signal in the center of the device shows an overshoot which is explained by the vanishing negative contribution of the excess charge carriers while the positive heat signal decays much slower (fig.16). Besides there might be additional heating due to recombination of the excess carriers.

V. CONCLUSION

Transient interferometric mapping experiments of drain extended ULSI devices under TLP stress have been presented for the first time. They fully support the recently presented predictions based on TCAD simulations, which confirm the validity of the TCAD modeling approach. In addition, an initially unexpected strong impact of the free charge carriers is discovered in the superposed phase signal over the complete duration of the pulse at high current densities. A significantly improved failure current of 4 mA/µm of the drain extended NMOS was experimentally shown by achieving a uniform turn-on during base push-out. Using a combination of TCAD device simulations and TIM measurements, the detailed device physics behind the critical ESD phenomena under high transients could be explored. This understanding paves way for further device optimization and TCAD-based ESD robustness prediction.

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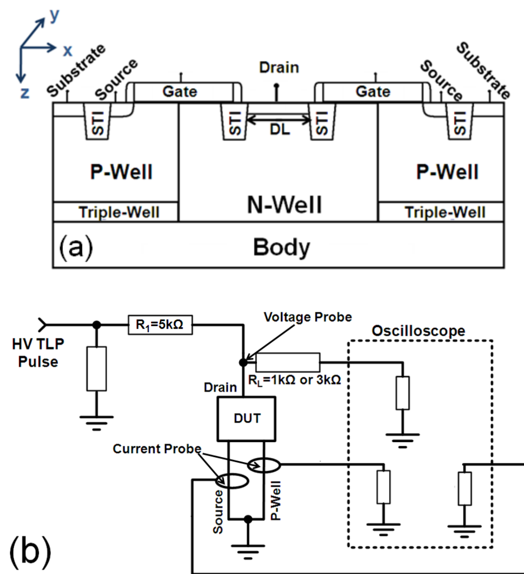

Fig. 1: (a) Schematic of DeNMOS device. Figure shows folded/two-finger structure (W= 2x 5 µm) which was fabricated on silicon using state of the art 65nm CMOS process. (b) Electrical scheme for device stressing and TIM.

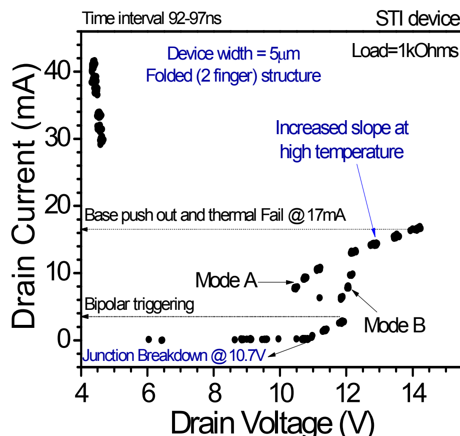

Fig. 2: TLP characteristics of DeNMOS device at lower load line (i.e. 1kΩ). Figure shows (i) junction breakdown, (ii) pulse-to-pulse instability, (iii) bipolar triggering and (iv) base push out followed by device failure. Figure shows two stable states at lower current branch, i.e. snapback state (Mode-A) and high resistance state (Mode-B) .

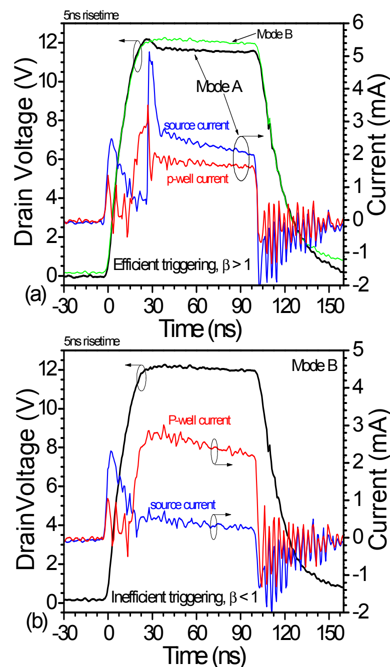

Fig. 3: At lower current levels the NPN depicts a bimodal triggering behavior in Mode-A (Fig.3a) and Mode-B (Fig.3b). Figure shows that bipolar triggering is inefficient (β < 1) in Mode-B, whereas it triggers efficiently (β > 1) with snapback in Mode-A.

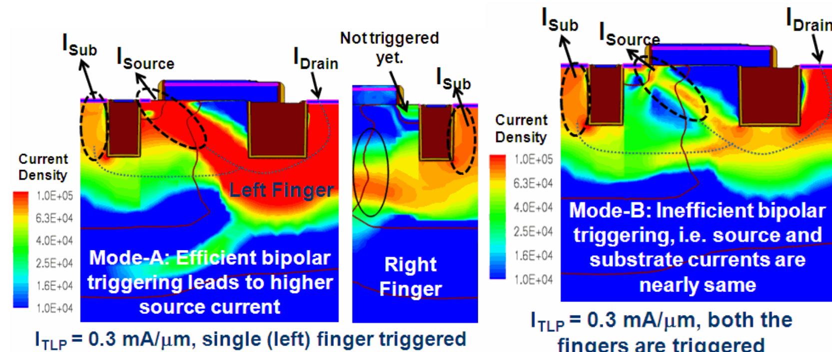

Fig. 4: TCAD simulation: At lower current levels nature of current flow in Mode-A (left) and Mode-B (right). Figure shows that β < 1 in Mode-B leads to high resistance state, whereas β > 1 in Mode-A, which leads to snapback.

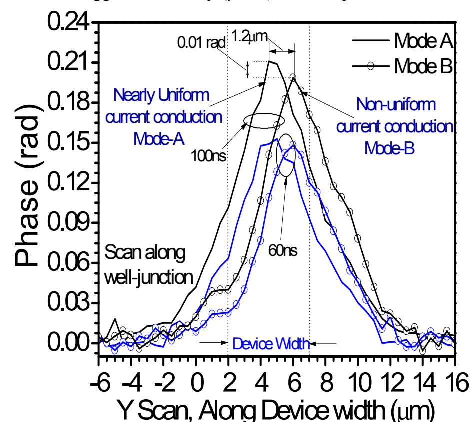

Fig. 7: TIM behavior (Y-Scan, along well-junction) in Mode-A and Mode-B after 60 ns and 100 ns. It shows an uniform conduction in Mode A as compared to Mode-B, which is slightly shifted to the right half of the device.

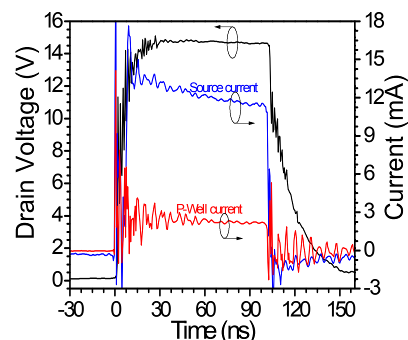

Fig. 5: At moderate/higher levels source current is dominant. This means that even though the device is in high resistance state at moderate/higher values of TLP pulse (Fig 2), the bipolar gets triggered efficiently

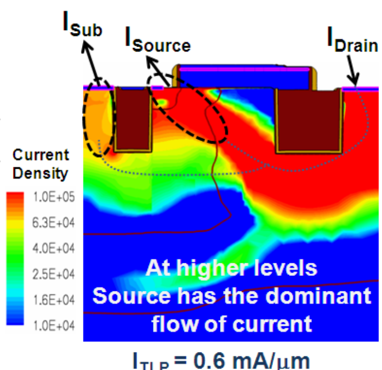

Fig. 6: At moderate/higher levels source current is dominant and the bipolar gets triggered efficiently since the current density at well junction is sufficient enough in order to produce II carriers for efficient bipolar triggering (b).

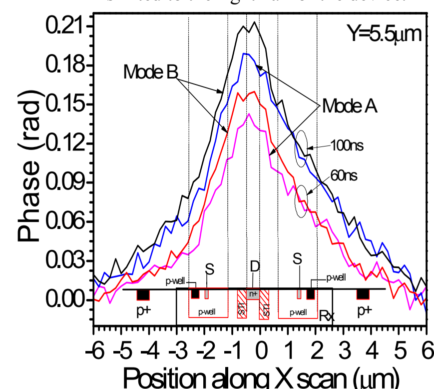

Fig. 8: TIM behavior (X-Scan) in Mode-A and Mode-B after 60 ns and 100 ns. It shows that the hot spot always sits at drain diffusion which was also proved by simulations [5]. Self heating behavior in both the modes are nearly identical.

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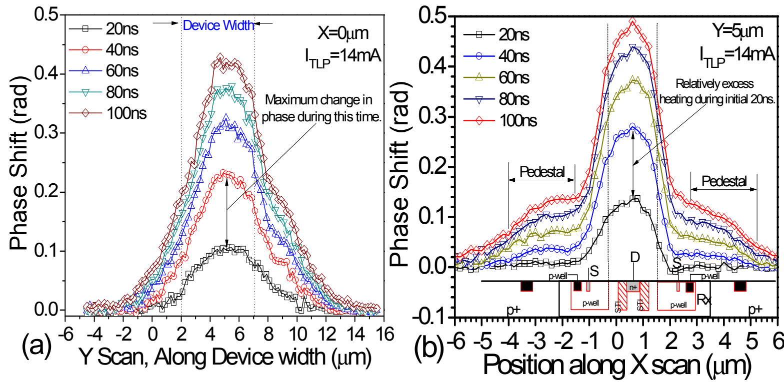

Fig. 9: Transient development of the TIM signal at moderate currents (a: Y-Scan and b: X-Scan). It shows that phase shift increase (i.e. heating) is faster during first 40ns (between 0-40ns) than in the next 60ns (i.e. 40-100ns). This supports excess heating during the initial time due to space charge [5] (a) Figure shows uniform conduction along the device width. (b) A bell shape characteristics along X axis unlike to triangular distribution found at lower current is because of excess carriers in the body/pedestal region, which leads to negative phase component. Fig. also shows identical phase distribution in both the fingers and gives a signature of heating in the pedestal region.

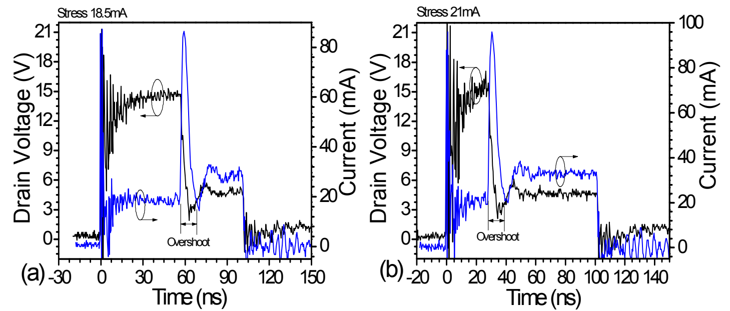

Fig. 10: A significant amount of current over shoot during charge modulation proves the space charge build up and its discharge after onset of base push out. The time at which the discharge takes place and the current overshoot during the discharge depends on forced TLP current. (a) I_{TLP}=18.5mA, Overshoot time=60ns and overshoot current=80mA. (b) I_{TLP}=21mA, Overshoot time=30ns and overshoot current=100mA.

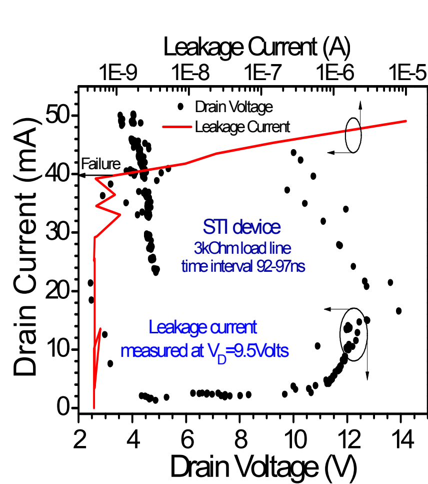

Fig. 11: TLP behavior of device at higher load line, i.e. 3kΩ. The figure shows soft snapback but no failure even up-to higher currents i.e. higher failure threshold. (leakage current measured at 9.5V).

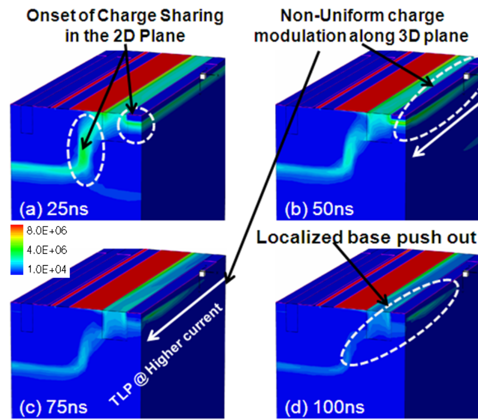

Fig. 12: 3D Electric field (V/cm) plot at different times. (a) Fig. shows the onset of base push out in 2D plane at shorter times, further (b & c) non-uniform charge modulation in 3D plane and finally (d) strong filamentation because of localized base push out.

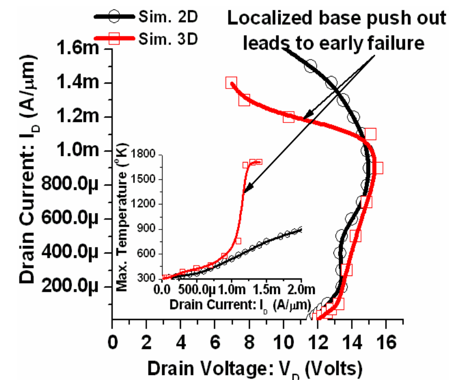

Fig. 13: Simulated 3D and 2D TLP curves which shows the snapback and self heating behavior in two cases: (i) 3D simulation provides the device behavior when it has localized base push out, whereas (ii) 2D simulation shows the device behavior when charge modulation occurs only in 2D plane.

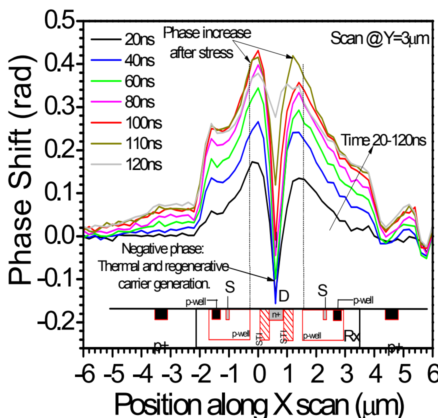

Fig. 14: TIM (X-Scan) behavior of device in base push out region, (i.e. at higher currents) shows negative phase shift at drain diffusion (N^+ drain contact). This is attributed to excess carrier injection/generation which leads to regenerative NPN action. This behavior was absent at moderate currents which validates that the regenerative NPN action starts at the onset of base push out [5].

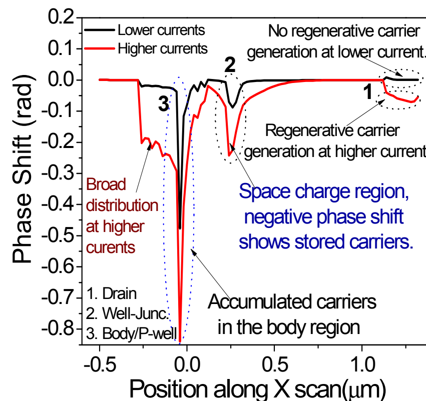

Fig. 15: Simulated phase shift due to excess carriers present in the device at lower and higher currents. Figure shows significant amount of carrier generation in the (1) drain region and accumulation/storage in the (2) well-junction and body region.

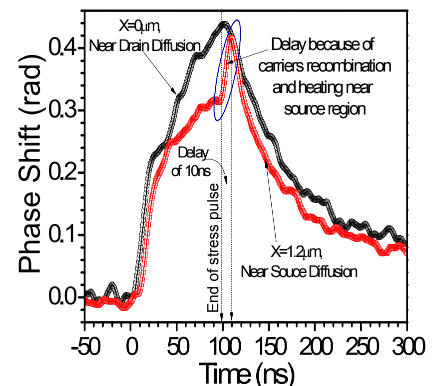

Fig. 16: Change in the phase at different location w.r.t. time. Fig. shows fall in phase at drain diffusion just at the end of stress pulse (i.e. 100ns) and delay of 10ns near source/body region, which is attributed to heating because of excess carriers in the body region. These excess carriers arise from regenerative carrier generation near drain diffusion after base push out (Fig. 16).

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