BENCHMARKING THE DEVICE PERFORMANCE AT SUB 22 NM NODE TECHNOLOGIES USING AN SoC FRAMEWORK

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Abstract: For the first time this paper makes an attempt at predicting the System-on-Chip (SoC) performance (i.e. logic, SRAM, ESD and I/O) of various sub 20 nm channel length planar and non-planar SOI devices using extensive & well calibrated 3D device and mixed-mode TCAD simulations. It has been shown that the non-planar devices such as FinFETs are not the ideal choice for SoC applications and perform poorly in comparison to the Ultra thin body (UTB) planar SOI MOSFETs. We further show different strategies to optimize the planar UTB MOSFETs for improved ESD robustness and I/O performance.

I. INTRODUCTION

A number of non-planar devices such as FinFETs and nano-wire FETs are proposed as technology options for sub 22 nm node gate lengths [1][2]. Further, underlap devices were found to have a better short channel performance and higher drive currents at gate lengths below 20nm compared to the overlap devices [3]. FinFET devices were also found to have a robust ESD performance [4]. While all these devices have shown an excellent performance, they suffer from issues such as width quantization and extra parasitics because of their 3D nature. The limitations with strain engineering in non-planar structures is also an issue currently [5][6]. Recently ultra thin body (UTB) SOI MOSFET was demonstrated as an option for sub 20nm gate lengths, with advantages like lower 3D parasitics, ease of incorporating strain effects, flexibility in width selection and suppressed random dopant fluctuation [7]. However, its ESD and I/O behavior still needs to be evaluated. During the technology development phase, one would normally optimize the technologies for their core circuit performance (i.e. logic and SRAM) and then look into the ESD and I/O issues. This poses a serious challenge to the ESD and I/O designers particularly in the sub 32nm technologies, where a co-development of core and I/O designs is desirable for a robust SoC performance. Keeping this objective in mind, a comprehensive evaluation of SoC performance (i.e. logic, SRAM, ESD and I/O) of various planar and non-planar devices is performed in this work, using well calibrated TCAD tools.

II. DEVICES AND SIMULATION SETUP

Fig. 1 shows the various devices used for 3D TCAD simulation studies. A well calibrated simulation deck is used here. TCAD mobility models for drift-diffusion transport considering quantum corrections are matched with experimental data for FinFETs (Fig. 2) [3][8]. Further the avalanche models and thermal boundary conditions are also calibrated with experiments [4] in order to capture the ESD and I/O behavior as shown in Fig. 3. The calibrated models provide an excellent fit (with a $\pm$5% error) with experimental I-V characteristics of Nano-wire FET [2] and mobility parameters for UTB-MOSFETs [9]. Fig. 4 shows the "Inverter driving Inverter" cell layout designed using the predictive technology model (PTM) in order to capture the delay overhead because of interconnect parasitics [10].

III. RESULTS AND DISCUSSION

A. Device optimization and short channel performance

Figures 5 and 6 compare the intrinsic and short channel performance of various devices. The thickness of the Fin, Nano-wire and the UTB silicon film thickness are optimized in order to achieve an equal I_{OFF} (50nA/μm) for all the devices. The devices are individually optimized at the same I_{OFF} for a maximum I_{ON}. We use equal I_{OFF} per unit electrical width as an optimization criterion for different planar/non-planar devices. FinFETs and Nano-wire devices have a better intrinsic and short channel performance for a given I_{OFF} per unit electrical width as compared to the UTB-MOSFETs.

B. Logic circuit and SRAM performance

Fig. 7 (a)-(c) shows that the inverter delay overhead because of device parasitics is much higher compared to the overhead because of interconnect parasitics for all devices under study. Further, Fig. 7 (d) shows that even though the ON current is maximum for the case of nano-wire device (Fig. 5b), the inverter delay is minimum for the case of UTB-MOSFET. This behavior is attributed to less 3D parasitics in UTB-MOSFETs, compared to the other non-planar devices, as demonstrated in Fig. 8 (a)-(c). Further, Fig. 8(d) illustrates that the interconnect parasitics are lower by an order of magnitude as compared to the device parasitics. Each device is realized with a minimum possible electrical width, which makes the FinFET device width equivalent to $2H_{FIN}+W_{FIN}$. Accordingly, Fig. 9 shows that the power performance of a UTB-MOSFET is better, compared to the FinFET and Nano-

wire devices, which is attributed to the width quantization effect in these non-planar devices. From the logic circuit performance results presented in Fig. 9, it can be seen that the Si-Nano-wire FET performs poorly at the scaled channel lengths because of its higher parasitics and quantized width as compared to the FinFET and UTB devices. This is primarily attributed to the gate-all-around nature of the silicon wire transistors.

SRAMS, which are designed using the minimum sized planar devices, interconnect capacitance [10] will cause a dominant loading on the bit-line as the technology is scaled down [3]. Fig. 8 gives an idea on the dominance of 3D device parasitics in non-planar devices. Considering this, Fig. 10 shows the calculated bit-line capacitance for a 1024 cell SRAM designed using the UTB-MOSFET and FinFET devices. Inset of Fig. 10 shows the various parasitic components contributing to the capacitive loading on bit-line. We found that the coupling capacitance between the bit-line and word-line (C_{WL}), which is the drain-to-gate coupling of access transistors, leads to a higher bit-line capacitance for FinFET SRAM compared to the UTB-MOSFET SRAM. This is attributed to the higher electrical width (because of width quantization) of access transistor in FinFET SRAMs. Fig. 11 shows that the read access time of UTB-MOSFET SRAM is 30% higher than the FinFET SRAM, which is due to the higher component of interconnect capacitance in UTB-MOSFET SRAMs (50%), compared to the FinFET SRAM (15%). Cell leakage power is improved by 10X in UTB-MOSFET SRAM, compared to the FinFET SRAM while the static noise margin is nearly the same.

C. ESD and I/O performance

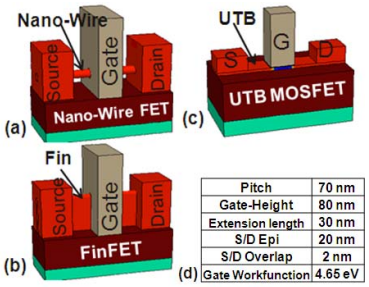
Figures 12 and 13 show that the device with a larger fin width exhibits a lower failure threshold (I_{T2}), which also validates the previously-reported experimental data [4]. This behavior also gives an indication that the fin width relaxation, which is followed in underlap FinFETs [3], cannot improve the I_{T2} of FinFET devices. Fig. 14 (a) shows that the hot spot occurs at the drain-to-gate edge and a major portion of the dissipated power gets absorbed by the metal gate. For the same fin width, we found that the underlap device has a lower failure threshold, which is attributed to the reduced cooling from the metal gate since the peak of the hot spot gets shifted under the spacer region (Fig. 14.b). Further Fig. 15a shows that the peak current flows through the center of the fin under the ESD stress. This is because of less depletion in the center of the fin as compared to the outer surface. Fig.15b shows a degraded I_{T2}/C performance while introducing a high-k & underlap. Fig. 16 shows that increasing the channel length reduces the I_{T2} of UTB-MOSFETs in contrast to FinFET devices. Figures 17 and 18 prove that the device fails because of a strong current filamentation at higher temperatures. Fig. 19 compares the I_{T2} of FinFET and UTB-MOSFET using different normalization schemes (inset). Since the FinFET has a higher volume for a given active width, it has a much higher I_{T2} per unit Si width, compared to the UTB-MOSFET. But I_{T2} values for both the devices are nearly same if compared for equal footprint. Fig. 20 shows that even though both the devices have an almost equal I_{T2} in a given footprint, UTB-MOSFET is better in terms of failure threshold per unit capacitive load (I_{T2}/C). This behavior is attributed to the 30% less parasitics in UTB-MOSFET. Fig. 21 shows that even though the UTB-MOSFET has been found to have less I_{ON}, it has a better V_{BD} v/s R_{ON} performance, compared to the FinFET devices.

D. Underlap (UND) High-K Spacer (HK) UTB-MOSFET

Until now we concluded that the UTB-MOSFET has a better SoC performance, compared to the conventional FinFET and Nano-wire devices. An underlap FinFET device may improve the logic and SRAM performance for the cases in which the interconnect capacitance is dominant [3], but will lead to a degraded ESD reliability. In order to further improve the ESD reliability of UTB-MOSFETs, without sacrificing on their logic performance, we propose a UND-HK-UTB-MOSFET, as shown in Fig. 22. Fig. 23 shows the performance improvement at an I_{OFF} of 50nA/μm, normalized with respect to a standard UTB-MOSFET. The effect of SOI thickness relaxation for different underlap lengths is also studied. It is clear that ESD and logic performance of the proposed UND-HK-UTB-MOSFET is improved by 40% and 15%, respectively, compared to a standard UTB-MOSFET device.

IV. CONCLUSION

We evaluated the SoC performance of various planar and non-planar SOI devices. Using logic and SRAM as a test vehicle, we have shown that the planar devices (UTB-MOSFETs) exhibit a superior circuit performance in terms of their speed and power dissipation when compared to their non-planar counterparts. This can be attributed to the lower 3D parasitics and flexible width selection possible with planar UTB-MOSFETs. Further, we show that the I_{T2} of a UTB-MOSFET is nearly identical to that of a FinFET when area is used for comparison, while the UTB-MOSFET exhibits a superior I_{T2}/C performance. Underlap FinFETs, though effective in improving the circuit performance, tend to degrade the ESD reliability. The proposed planar UND-HK-UTB-MOSFET device has a better ESD reliability, excellent logic performance, and is therefore a superior candidate for SoC designs for channel lengths below 20nm.



Pitch	70 nm
Gate-Height	80 nm
Extension length	30 nm
S/D Epi	20 nm
S/D Overlap	2 nm
(d) Gate Workfunction	4.65 eV

Fig. 1: (a-c) Various planar and non-planar devices realized for 3D simulation studies. Hollow region was filled with spacer and isolation oxide. Aspect ratio for FinFET was 5.(d) Common dimensional and electrical parameters of studied devices and their values.

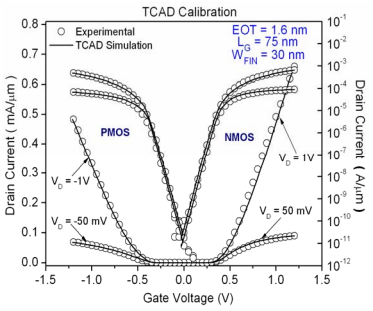


Fig. 2: Calibration of TCAD models for drift diffusion transport with experimental data [3][8].

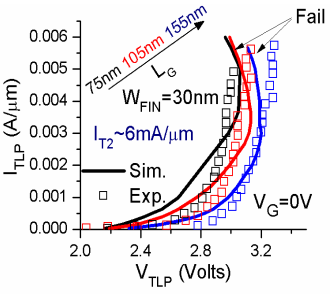


Fig. 3: Calibration of avalanche model and thermal boundary condition with experimental data [4].

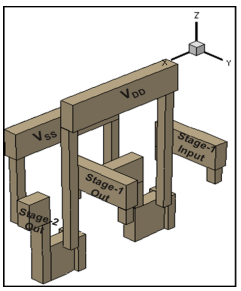
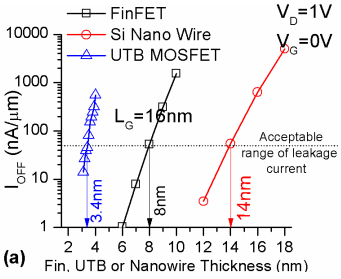
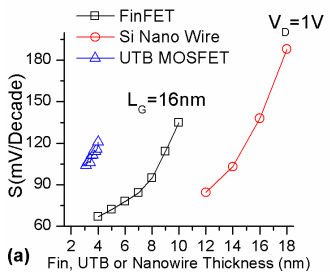
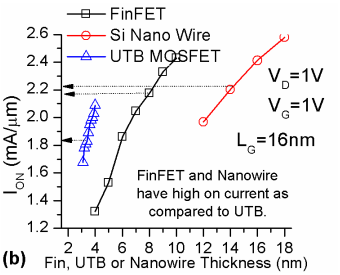
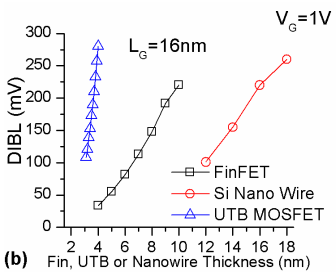


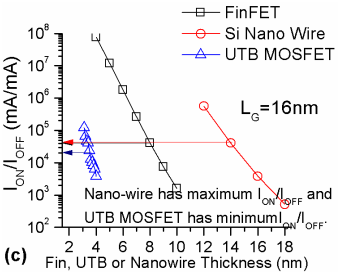
Fig. 4: 3D layout of Inverter cell with fan out =1 covering both device and interconnect parasitic capacitances











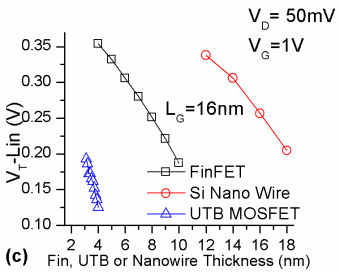
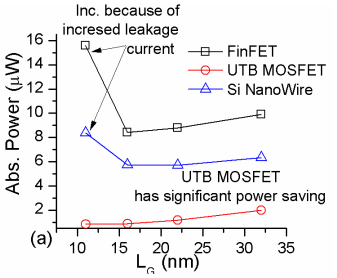


Fig. 5: Impact of Fin, Nanowire and SOI thickness on (a) I_{OFF} (b) I_{ON} and (c) I_{ON}/I_{OFF}. Fin/SOI thickness or Nanowire diameter is optimized in order to achieve equal I_{OFF} (50nA/μm) and maximum I_{ON}. (Nanowire thickness is mentioned everywhere in contrast to its diameter.

Fig. 6: Impact of Fin, Nanowire and SOI thickness on (a) Subthreshold slope (b) DIBL and (c) V_T Roll-off. UTB-MOSFET is quite sensitive to thickness in contrast to Nanowire.



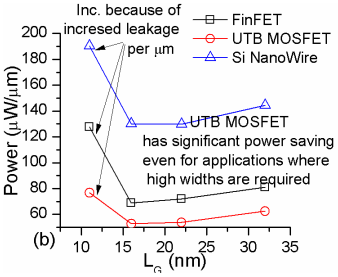


Fig.9: Performance of various devices in terms of (a) Absolute/total power dissipation and (b) Normalized (per electrical width of the device) power dissipation.

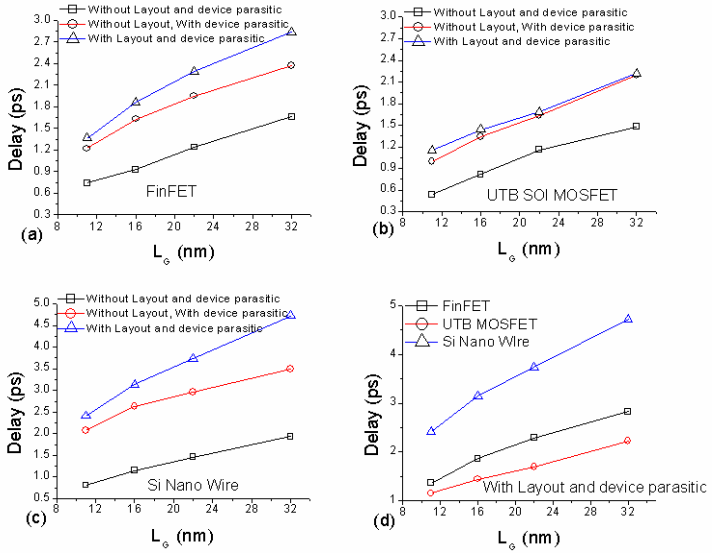


Fig. 7: (a-c) Impact of various parasitic components on the inverter delay at different channel lengths. (d) Inverter delay comparison of various studied devices at different channel lengths.

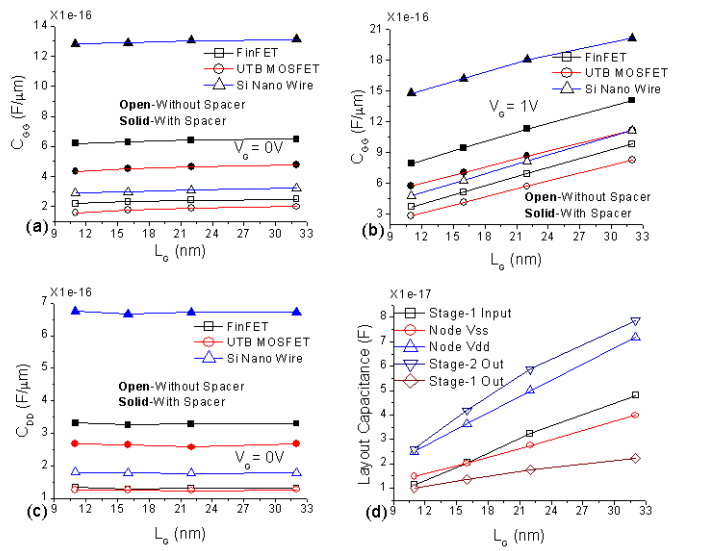


Fig. 8: (a-c) Various device parasitic components at different channel lengths (d) Various layout parasitic components at different channel lengths.

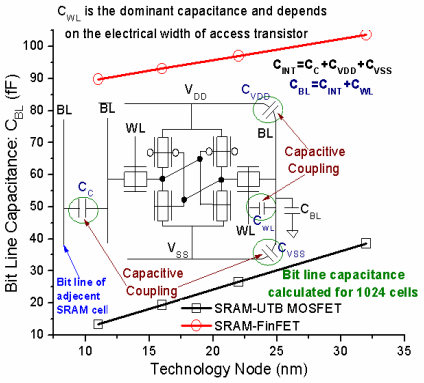


Fig. 10: Bit line capacitance of 1024 cell SRAM designed using UTB-MOSFET and FinFET. Inset shows a SRAM cell and various capacitive components which leads to loading over bit-line. SRAM cell size used to calculate bit line capacitance is referred from [11].

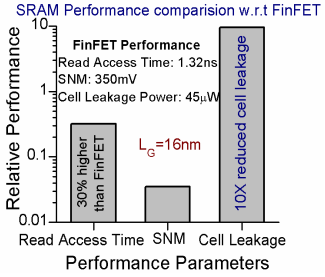


Fig. 11:Relative performance (Read access time, SNM & Cell leakage power) comparison of UTB-MOSFET SRAM w.r.t SRAM designed using FinFET device.

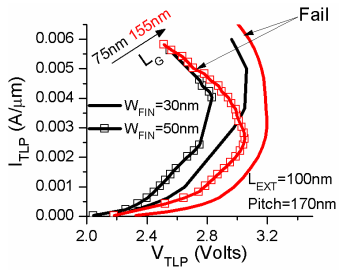


Fig. 12: TLP (100ns HBM) behavior of FinFET device for different fin thickness and channel lengths.

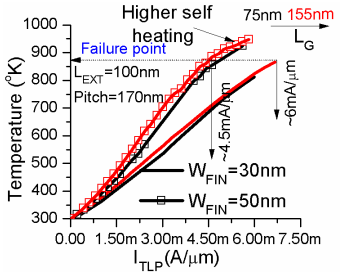


Fig. 13: Self heating nature of FinFET device for different fin thickness. Figure shows device with higher fin thickness has lower failure threshold.

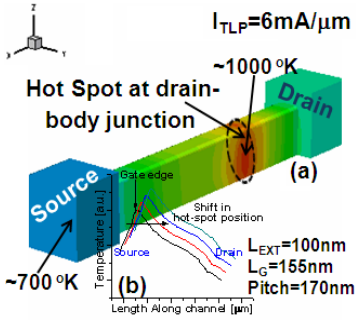


Fig. 14: (Lattice temperature plot) Self heating behavior of FinFET device under ESD stress conditions. The hot spot is at the drain-to-gate edge. Inset shows shift in hot spot location by introducing underlap.

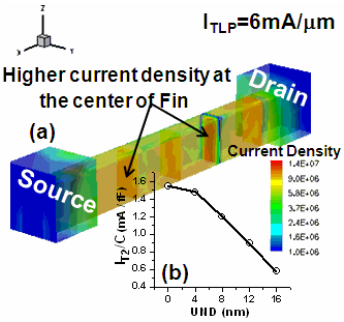


Fig. 15: (Current density plot) Figure shows that peak current flows through the center of the fin under ESD stress conditions. Inset shows degradation in I_{T2}/C performance by introducing underlap

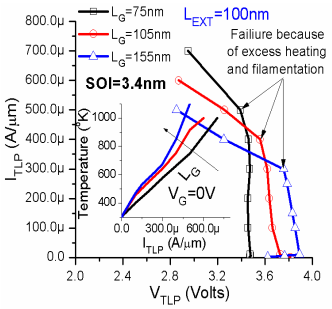


Fig. 16: TLP (100ns HBM) behavior of UTB-MOSFET device for different channel lengths. Inset shows self heating behavior at different channel lengths under ESD stress.

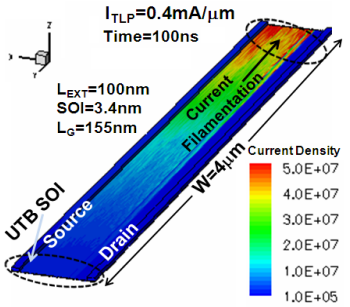


Fig. 17: Nature of current filamentation inside the UTB-MOSFET device under ESD stress conditions. Here the filament is static and not moving.

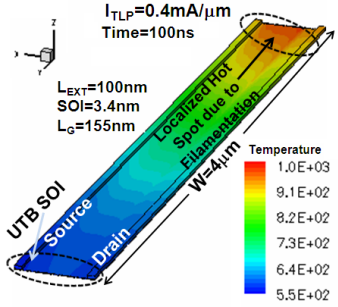


Fig. 18: Self heating behavior of UTB-MOSFET under ESD stress conditions. Localized hot spot can be seen because of filamentation.

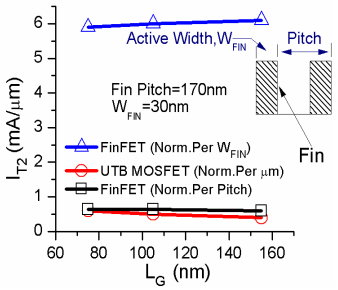


Fig. 19: Failure threshold (I_{T2}) comparison of FinFET and UTB-MOSFET at different channel lengths using different normalization schemes.

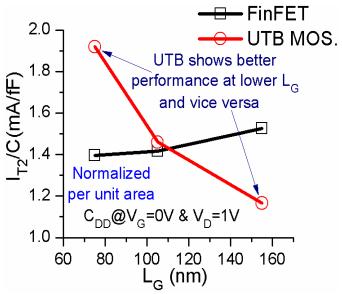


Fig. 20: Failure threshold per unit capacitive load (I_{T2}/C) for FinFET and UTB-MOSFET at different channel lengths.

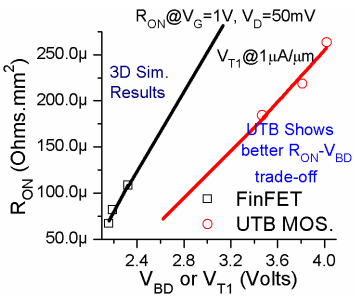


Fig. 21: V_{BD} v/s R_{ON} trade-off comparison for FinFET and UTB-MOSFET.

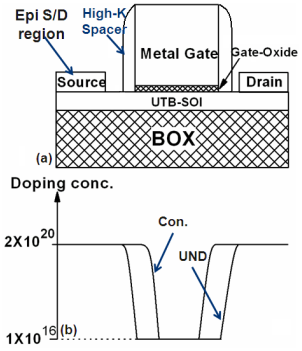


Fig. 22: (a) Underlap (UND) UTB-MOSFET. (b) Doping profiles of underlap and conventional UTB-MOSFET.

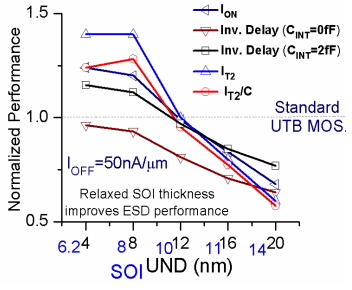


Fig. 23: Normalized SoC performance comparison of UND-UTB-MOSFET at different underlap lengths w.r.t con. UTB-MOSFET.

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