On the Differences Between 3D Filamentation and Failure of N & P Type Drain Extended MOS Devices Under ESD Condition

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***Abstract*- We present differences in the ESD failure mechanisms, intrinsic behavior and various phases of filamentation of STI type DeNMOS and DePMOS devices using detailed 3D TCAD simulations, TLP and TIM experiments. The impact of localized base-push-out, power dissipation because of space charge build-up, regenerative bipolar triggering and various events during the current filamentation are compared. Measurements show that the absence of base push out in DePMOS device leads to ~2.5X higher I_{T2} as compared to DeNMOS.**

***Index Terms*- DEMOS, ESD Failure, space charge build-up, Filamentation.**

I. Introduction

Low Voltage (LV) NMOS device is widely used as a ESD clamp because of its high failure current value (I_{T2}), whereas the Drain extended NMOS (DeNMOS) devices have been found to be extremely vulnerable towards the ESD event [1]-[4]. Recently we presented a complete picture of STI type DeNMOS device failure and current filamentation using Transient Interferometric Mapping (TIM) experiments and 3D TCAD simulations [5][6]. In the past, LV PMOS devices have shown lower I_{T2} as compared to LV NMOS. Intuitively, Drain extended PMOS (DePMOS) devices should perform even worse under the ESD conditions, whereas our measurement results show a ~2.5X higher I_{T2} for DePMOS device, as compared to DeNMOS. This gives an indication towards a different filamentation and failure mechanism involved in DePMOS devices. We observed that the drain extension region doping is slightly higher for DePMOS device (P-Well doping) as compared to DeNMOS (N-Well doping), which makes the DePMOS device less prone to base push out or charge modulation. This work compares the 3D filamentation and device failure mechanisms involved in STI type DeNMOS and DePMOS devices, which has not been reported before.

II. Device And Experimental Setup

Thin gate oxide, double finger DeNMOS and DePMOS device with STI under the gate-drain overlap, as shown in Fig. 1a & 1b, are processed in a state-of-the-art 65 nm node CMOS technology. The electrical scheme for device stressing is given in Fig. 1c. TIM method monitors the temperature and free-carrier concentration induced changes in the silicon refractive index with a 1.5µm areal resolution and 3ns time resolution [7]. During the scanning, 30 stress pulses are applied at every scan point. A well calibrated process and device simulation (for low currents) deck is used for 3D TCAD simulation, as described in our previous papers [5][6][8]. It is worth mentioning that simulations here underestimate (by 15%) the I_{T2} values, which is due to slight differences in the simulated P-Well profile with the actual SIMs profile. Nevertheless, TCAD setup can still capture the physical phenomena behind current filamentation and device failure accurately.

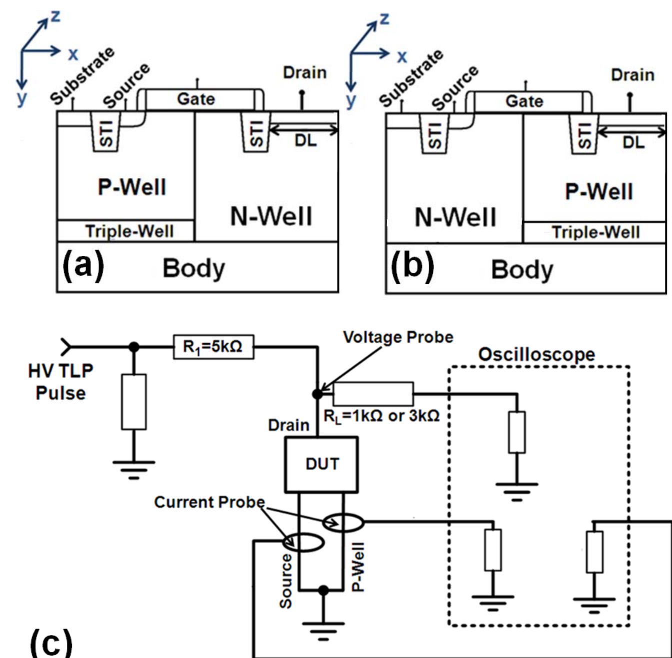

Fig. 1: Schematic of (a) DeNMOS and (b) DePMOS device. Figure show half structure only, whereas it was originally fabricated on silicon as in folded geometry/double finger (W= 2 x 5 µm) using state of the art 65nm CMOS process. (c) Electrical scheme for device stressing and TIM experiments.

III. On The Difference Of Device Intrinsic Behavior

The TLP characteristics (Fig. 2) show that the DeNMOS device undergoes failure at very low currents (~1.2mA/µm), whereas a DePMOS device survives up to ~2.5X higher currents (~2.9mA/µm). The higher I_{T2} is attributed to a

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slightly higher doping in the drain extension region of DePMOS as compared to DeNMOS (Inset, Fig. 2). Higher doping in the drain extension region survives the base push out driven filamentation [5][6], which eventually leads to higher failure threshold. It is worth mentioning that besides a lower hole mobility, both the devices have almost an equal on-resistance at lower currents, whereas DePMOS starts outperforming at higher currents.

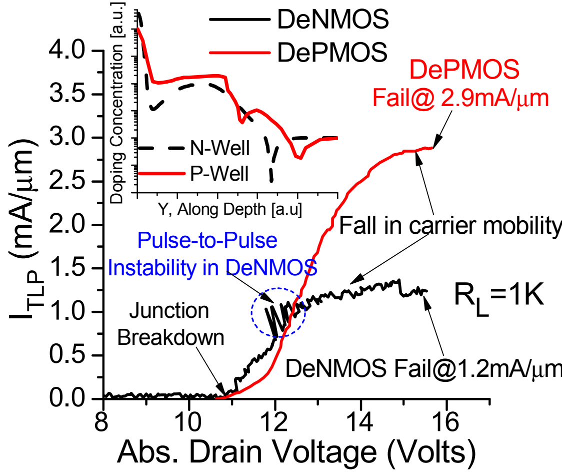

Fig. 2: Measured TLP characteristics of DeNMOS and DePMOS device at lower load line (i.e. R_L=1kΩ). Figure shows (i) junction breakdown at 10.7V, (ii) pulse-to-pulse instability and base pushout driven early failure in DeNMOS (iii) ~2.5X higher I_{T2} of DePMOS device as compared to DeNMOS (iv) Inset shows Drain extension region doping profile of DeNMOS and DePMOS (i.e. N-Well and P-Well respectively)

Differences in the device behavior before failure can be explained as follows-

(a) Junction Breakdown: Initially the current flow was dominated by junction breakdown, which occurs at 10.7V in both the devices (Fig. 2).

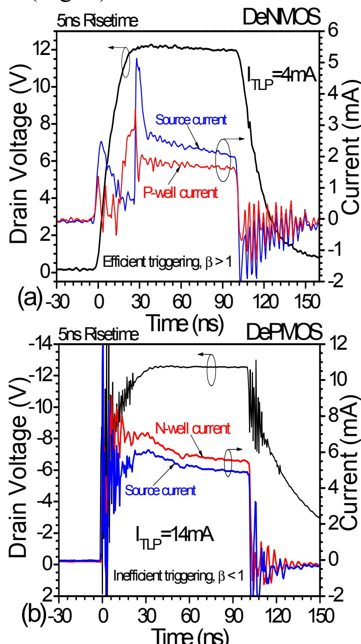

Fig. 3: Measured transient voltage/current plots during 100ns HBM event. (a) DeNMOS device triggers efficiently at lower TLP currents (4mA) whereas (b) DePMOS device show inefficient bipolar triggering even at higher TLP currents (14mA).

(b) Bipolar Triggering: Fig 3 shows that parasitic bipolar turns on efficiently (β > 1) at lower currents (4mA) in DeNMOS device, whereas DePMOS shows inefficient bipolar triggering (β < 1) even at higher TLP currents (14mA).

(c) Pulse-to-Pulse Instability: DeNMOS device has shown a pulse-to-pulse instability, whereas DePMOS device does not show a similar instability. Pulse-to-pulse instability was previously linked with bipolar turn-on and base push-out phenomena [5][6]. This difference is attributed to inefficient bipolar (PNP) turn on and absence of base push out.

(d) Base push out: Fig. 4 shows that DeNMOS device suffers from high electric fields underneath the drain diffusion [5], which is resulted from base push out and leading to early thermal failure. On the other hand, DePMOS device does not suffer from base push out and can withstand higher currents.

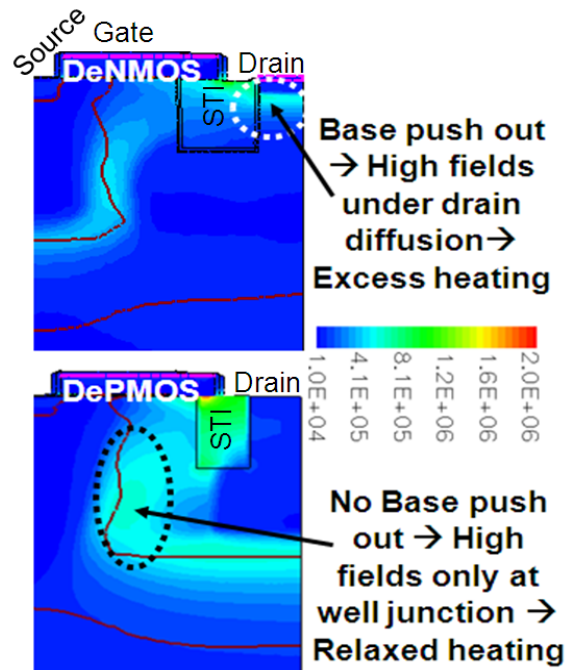

Fig. 4: Electric Field Plot (V/cm). DeNMOS device suffers from high electric field under drain diffusion because of base push out, which leads to early thermal failure. Whereas DePMOS device does not suffer from base push out and eventually survives up to higher currents.

IV. On The Difference Of 2D v/s 3D Behavior

Fig. 5 shows a distinct 2D and 3D behavior of DeNMOS device, which is attributed to localized charge modulation [6]. Onset of filamentation and thermal run away at very low temperature (600 K) signifies the leading role of base push out on the device failure (Inset Fig. 5) mechanism. Furthermore, Fig. 6 shows identical 2D and 3D behavior of DePMOS device, which is attributed to the absence of base push out. This eventually leads to a significantly higher value of critical temperature (1050 K) for the onset of filamentation and thermal run away (Inset Fig. 6) and provides higher value of failure currents.

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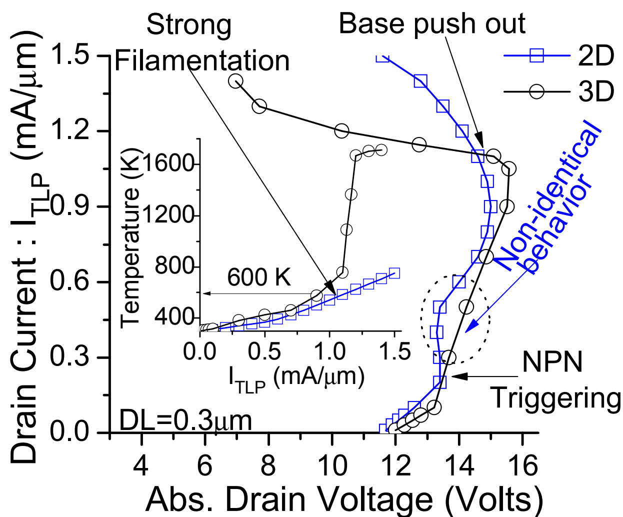

Fig. 5: TLP and self heating characteristics of DeNMOS device extracted from 2D and 3D simulations. Figure shows non-identical 2D v/s 3D behavior, whereas inset shows the onset of filamentation and thermal run away at very low temperature (600 K)

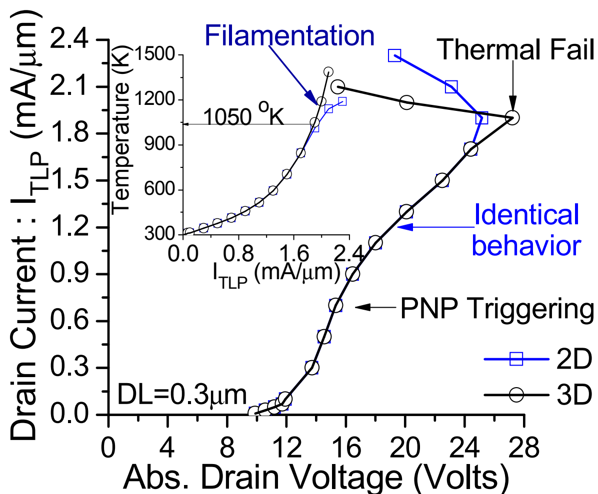

Fig. 6: TLP and self heating characteristics of DePMOS device extracted from 2D and 3D simulations. Figure shows identical 2D v/s 3D behavior, whereas inset shows the onset of filamentation and thermal run away at very high temperature (1050 K).

V. On The Differences Of Filamentation And Thermal Failure

Fig. 7a shows uniform current flow across the width of DePMOS device, even at higher TLP stress. Furthermore, uniform current flow at source side shows the absence of regenerative PNP action, which was found to be a cause of faster filamentation after base push-out. Fig. 7b shows that a strong filamentation exists in DeNMOS device, even at very low TLP stress values. Current shrink at drain side is because of elevated temperature, whereas shrink at source side is attributed to regenerative NPN action [5]. Figure 8 shows that DePMOS device has a hot spot at Nwell-to-Pwell junction, whereas it resulted underneath the drain diffusion in DeNMOS device. This is attributed to absence of base push-out in DePMOS device, which keeps the high electric field region near to the Well junction. (1) Lower current densities and (2) higher silicon area available for thermal diffusion at Nwell-to-Pwell junction is leading to relaxed self heating in DePMOS device as compared to DeNMOS, which eventually provides ~2.5X higher I_{T2}.

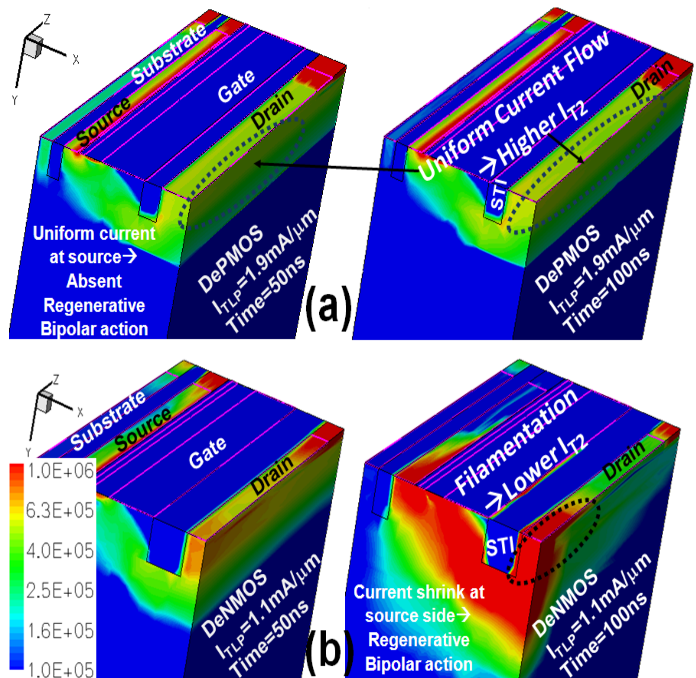

Fig. 7: Current Density Plot (A/cm^2) for (a) DePMOS and (b) DeNMOS devices at different time.

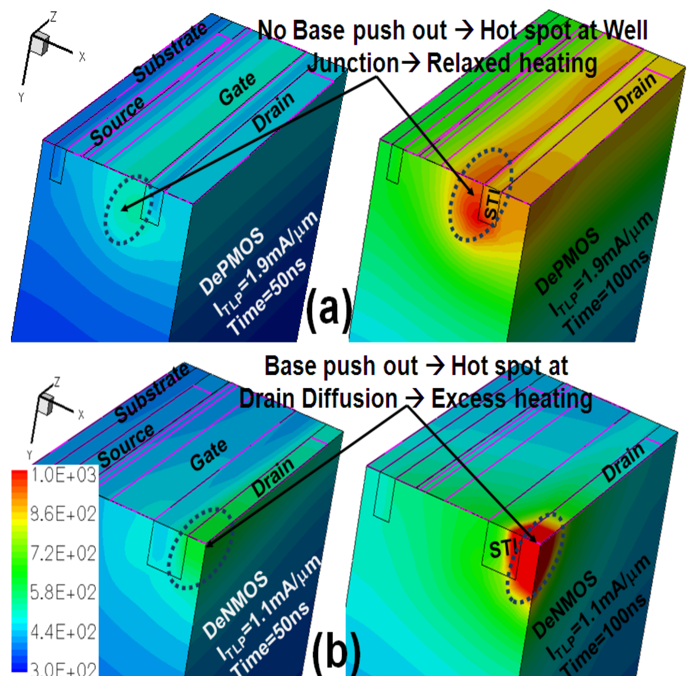

Fig. 8: Temperature Plot (K) for (a) DePMOS and (b) DeNMOS devices at different time. DePMOS device has hot spot at Nwell-to-Pwell junction, whereas it is underneath the drain diffusion in DeNMOS device.

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VI. On The Differences Of TIM Behavior

Fig 9 shows ~2X higher phase shift during the TLP stress (14mA), extracted from TIM measurements, in DeNMOS as compared to DePMOS device. This further validates the presence of excess heating in DeNMOS device, which leads to lower I_{T2}. Furthermore, DeNMOS device also shows significant heating (positive phase shift) during initial times (0-40ns), which is attributed to space charge build-up and current discharge after the onset of base push out [5][6]. Whereas, absence of base push out in DePMOS device leads to uniform phase shift with respect to time, i.e., a linear rise in temperature as a function of time.

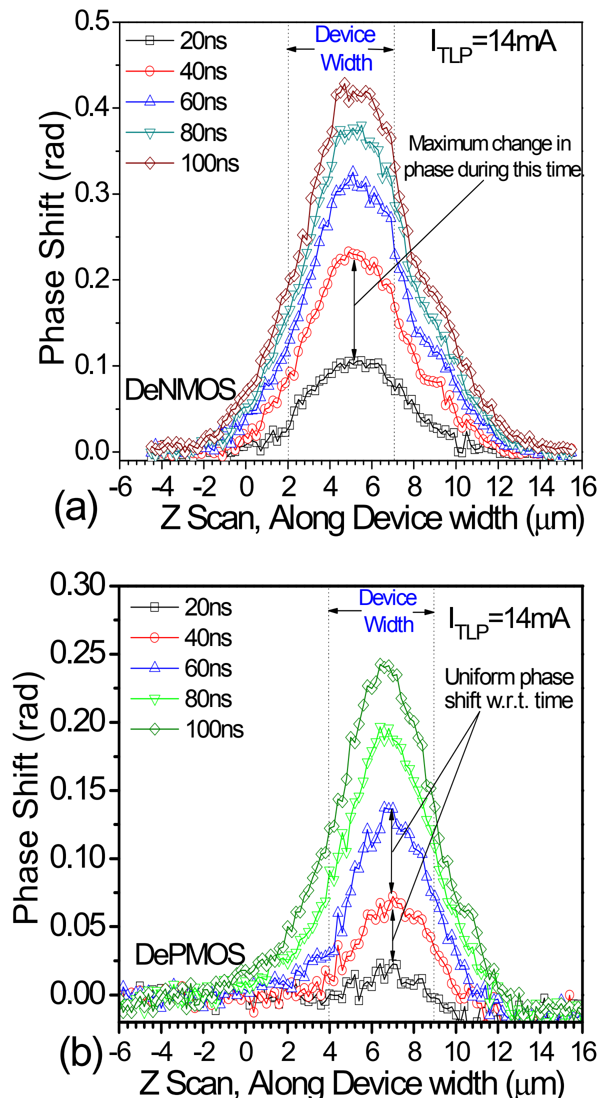

Fig. 9: Transient development of the TIM signal for (a) DeNMOS and (b) DePMOS devices (Z scan @ X': where X' is a point on X axis at which maximum phase shift occurs during X scan). DeNMOS device results ~2X higher phase shift as compared to DePMOS, which validates the presence of excess heating in DeNMOS device. Unlike to DePMOS, DeNMOS device also shows significant heating (positive phase shift) during initial times (0-40ns), which is attributed to space charge build-up and current

VII. Device Behavior At higher Load

Fig. 10 shows that both the devices fail at almost an equal TLP current when they are stressed at higher load (R_L=3KΩ). Relatively DeNMOS device shows a significant improvement (~3X) in I_{T2} as compared to DePMOS (30%). This behavior is attributed to the difference in failure mechanism of these devices. At higher load DeNMOS survives localized charge modulation, which increases the critical temperature for the onset of current filamentation. This eventually improves the failure threshold significantly. On the other hand, this critical temperature for DePMOS device is much higher, which therefore provides only a narrow window for improvement (30%) when the filamentation is survived using a higher load.

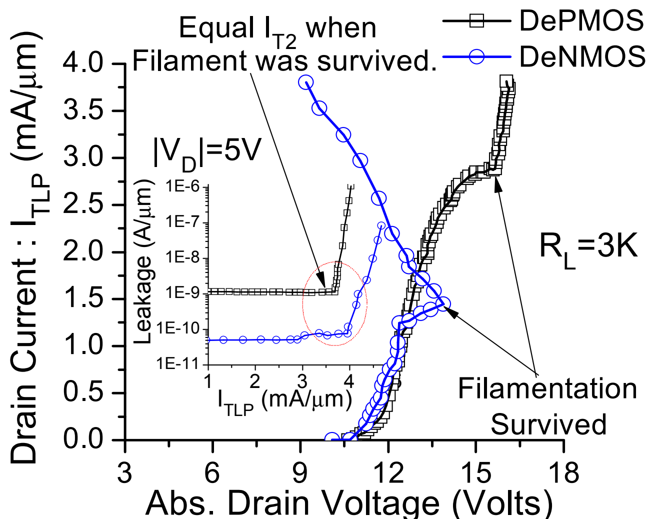

Fig. 10: Measured TLP characteristics of DeNMOS and DePMOS device at higher load line (i.e. R_L=3kΩ). Larger load survives the filamentation and leads to higher (almost equal) I_{T2} for both the devices.

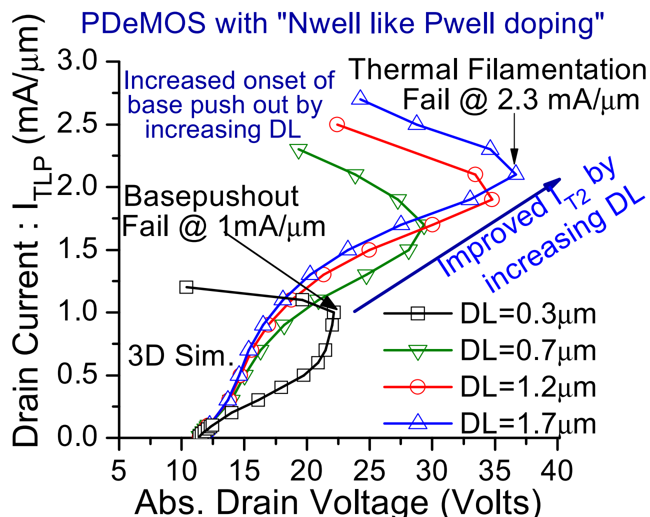

Fig. 11: TLP characteristics of DePMOS device *with N-Well like P-Well doping profile*, extracted from 3D simulations. DePMOS device (DL=0.3μm) with lower drain extension doping fails at 1mA/μm, which was further improved up-to 2mA/μm by increasing DL.

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VIII. DePMOS With N-Well Like P-Well Doping

By changing the drain extension region doping with *N-Well like doping profile*, DePMOS device (DL=0.3µm) has been seen to fail at 1mA/µm (Fig. 11). This further validates that lower drain extension region doping causes the base push out driven early filamentation and failure. Further, the same device shows a ~2X improvement in I_{T2} when the drain diffusion length (DL) is increased, which is attributed to the shift of the onset of base push out towards higher currents [5]. This also gives an indication that failure threshold and ESD window of standard STI DeNMOS can also be improved by changing the N-Well profile in order to mitigate the onset of base push-out.

IX. Conclusion

We demonstrate that the base push out in DeNMOS causes a very low critical temperature for the onset of current filamentation, which eventually results in a lower I_{T2}. However, absence of base push out in DePMOS device leads to ~2.5X higher I_{T2} as compared to DeNMOS. DePMOS devices do not show pulse-to-pulse instability and have identical 2D v/s 3D behavior, which is attributed to the absence of localized charge modulation and regenerative bipolar triggering. One can expect a width scaling due to the uniformity of current. TIM experiments have further validated the point that DePMOS devices have a relaxed self heating. Unlike the DeNMOS device, DePMOS devices have no space charge build-up and current discharge during initial time. In spite of a slightly worse voltage clamping capability per width, DePMOS is a better device option for power clamps, as compared to DeNMOS. It can also be concluded from this work that along with increasing the drain diffusion length, changing the N-Well profile in order to mitigate the onset of base push-out, is also a key for improving the ESD performance of the standard STI DeNMOS.

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