ESD Robust DeMOS Devices in Advanced CMOS Technologies

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Abstract- Improvement of ~5X in the I_{T2} (3.3mA/µm) of a grounded gate N-DeMOS device compared to a standard design is achieved by simple layout variations with a minor impact on its footprint. Robustness of P-DeMOS devices is shown to be further increased by additional p implant in drain region. Electrical and thermal instabilities are studied by Transmission Line Pulsing (TLP), Transient Interferometric Mapping (TIM) method and 3D TCAD simulations.

I. Introduction

Drain extended MOS (DeMOS) devices provide the required performance and reliability robustness for high voltage mixed signal applications in advanced CMOS technologies [1][2]. However, they commonly suffer from early failures under ESD like stress conditions due to filament formation and non-uniform current distribution. This can be a major roadblock for their application in System on Chip (SoC) designs. There have been several attempts to develop an understanding of the detailed failure mechanism using numerical device simulations and analytical formulations [3]-[6]. Recently it was proposed that avoidance of space charge modulation in the lowly doped drain region is the key to improve ESD robustness of these devices [7]-[10]. In this work, we present experimental investigations of N-DeMOS and P-DeMOS devices designed according to the recommendations of [7], which provide ~5X enhancement in the I_{T2}. A comprehensive theory of electrical and thermal instabilities leading to different failure modes is presented based on the detailed electrical (TLP) measurements, Transient Interferometric Mapping (TIM) experiments and 3D TCAD simulations.

II. Devices and Methods

A thin gate oxide, symmetric double finger, drain extended NMOS (DeNMOS) device with STI under gate-drain overlap, as shown in Fig. 1a, is processed in state-of-the-art 65 nm node CMOS technology with two different lengths of the drain diffusion region (DL), i.e. (a) DL=75 nm and (b) DL=750 nm. TIM method monitors the temperature and free-carrier concentration induced changes in the silicon refractive index with a 1.5µm areal resolution and 3ns time resolution while the device is stressed by 100 ns TLP pulses [11]. During TIM scanning along the device width, 20 TLP stress pulses were applied at each scan point.

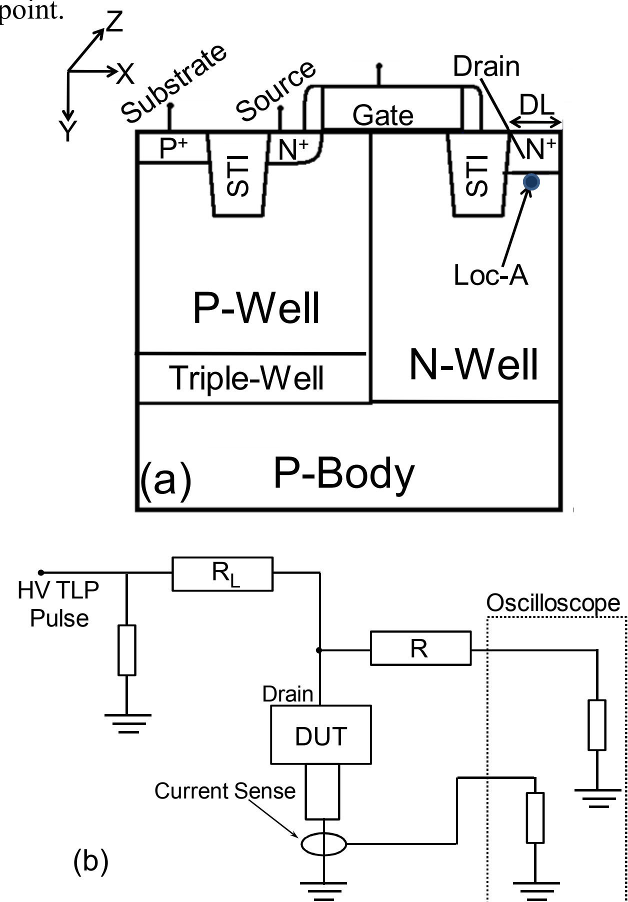

Fig. 1: (a) Cross-section of N-DeMOS device. Figure shows left finger of symmetric double-finger structure realized on-silicon (W (along z-axis) = 2x15µm). DL values are chosen to be 75nm and 750nm. Whole drain diffusion region was salicided. (b) Electrical scheme for device stressing.

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III. N-DeMOS Experimental Results

Impact of DL: With the technology scaling, diffusion length gets scaled at each node, too. For a MOS device, the drain diffusion length is usually defined by the minimum allowed design rule value in a given technology. Based on this fact, an engineering of drain extended MOS device by increasing drain diffusion length is not intuitive. Whereas, we found that the drain diffusion length in a STI type drain extended MOS device has a very strong impact on the device behavior at larger current densities. Figure 2 shows that the device with larger DL (DL=750nm) exhibits ~5X improvement in the failure current compared to a device with smaller DL (DL=75nm), while the layout area is only increased by 30%. The I_{T2} value amounts to 3.3 mA/µm which is the highest reported I_{T2} value for grounded gate DeMOS devices [12]. Also a clear triggering of second finger of the double-finger structure is easily observable close to a current level of 60mA.

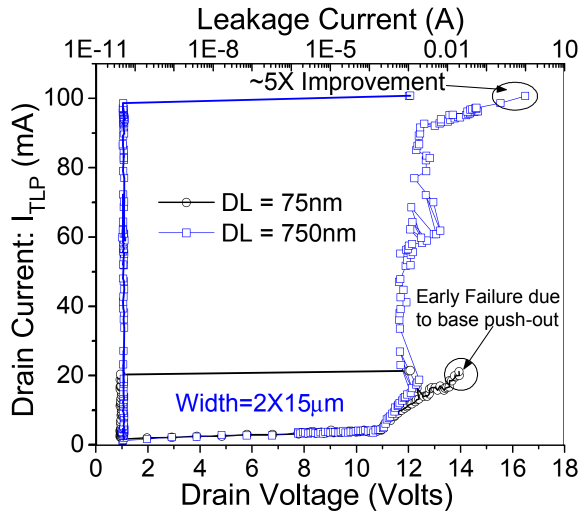

Fig. 2: Measured TLP characteristics of STI type DeNMOS device with (i) DL=75nm and (ii) DL=750nm. Figure shows a ~5X improvement in failure threshold when DL was increased from 75nm to 750nm.

This behavior could not be seen in any of the previous investigations, which is due to the fact that the DeMOS devices did not even survive the snapback at lower currents. The early fail has been explained by base push out phenomena and coinciding current filament formation [7]-[10]. The higher fail level reported in this paper is attributed to the absence of early current filamentation driven by base push-out. The suppression of current filamentation cannot be explained by ballasting resistance - unlike in the case of usual silicide blocked drain diffusion of ggNMOS devices. In the N-DeMOS the drain diffusion (N^+) region is fully silicided and a maximum number of contacts were used. By the increase in DL the on-resistance in the STI type drain extended MOS device is even reduced (fig. 3a) – unlike to the usual degradation in on-resistance of salicide blocked drains of ggNMOS devices. Moreover, increasing DL leads to a minor additional parasitic capacitance, which is due to small contribution (~5%) of the bottom capacitance (C_{small}) to the total capacitance (Fig. 3b).

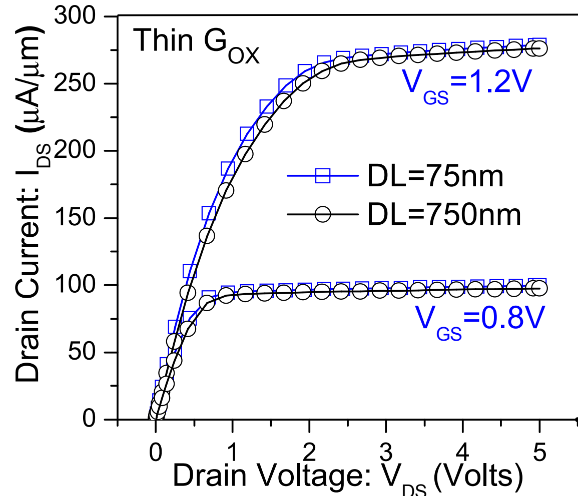

Fig. 3a: I_D-V_D characteristics of device with (i) DL=75nm and (ii) DL=750nm. Figure shows slight improvement in R_{ON} of device with DL=750nm compared to device with DL=75nm.

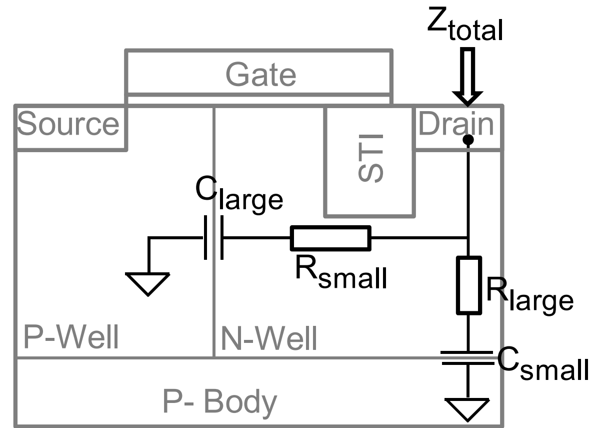

Fig. 3b: Fig. showing the dominant parasitic components and total effective drain-to-body capacitance within the device.

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IV. Electrical and Thermal Instabilities

A. TIM Investigations: To get more insight into the physical phenomena at higher current levels, TIM technique is applied in order to examine free carrier and temperature distribution across the device. Positive phase shift extracted from TIM measurements is a direct measure of temperature increase inside the device [11]. While an increase in free carrier concentration along the probing laser beam leads to a negative phase shift. Usually the signal is dominated by excess temperature within the high current & high field region, which eventually gives rise to an overall positive shift in the phase.

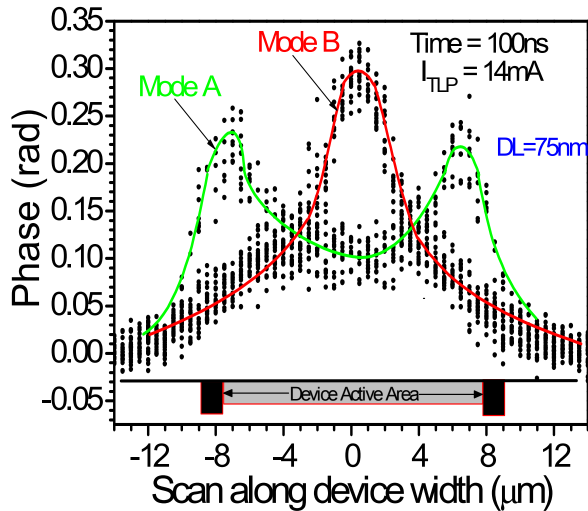

Fig. 4: TIM data for a device with smaller DL (75 nm) at a current right after onset of space charge modulation. Phase shift is plotted versus position along the device width under the drain diffusion region Envelops show phase shift evolution. Mode A and B randomly alternates from pulse-to-pulse.

TIM investigations for both the devices were performed at a current level close to the device failure (i.e. It2). Figure 4 and 5 show the extracted phase shift for devices with DL=75nm and DL=750nm respectively. On one hand, device with DL=75nm shows a localized distribution of current (Note: higher phase shift is a direct measure of higher temperature, i.e. high current density & high electric field) right before the device fails, alternating between two current distribution modes A and B. The, unique and well-determined locations of filamentary envelope shows a predictive nature of filament formation unlike to earlier discussions [6]. On the other hand, a device with DL=750nm shows a uniform temperature (or current) distribution along the device width z. The device with higher DL (750nm) doesn't show filamentation even at higher Itlp level. Note the significant difference in the peak phase shift (i.e. the temperature) extracted right before the fail for both the devices. Device with smaller DL has phase shift close to 0.3 rad and the one with larger DL has a shift of 1.5 rad, which means that right before fail, device with smaller DL has significantly lower lattice temperature compared to that of larger DL device. This leads to the conclusion that a rapid rise in current density and temperature happens during the filament formation in devices with DL=75nm.

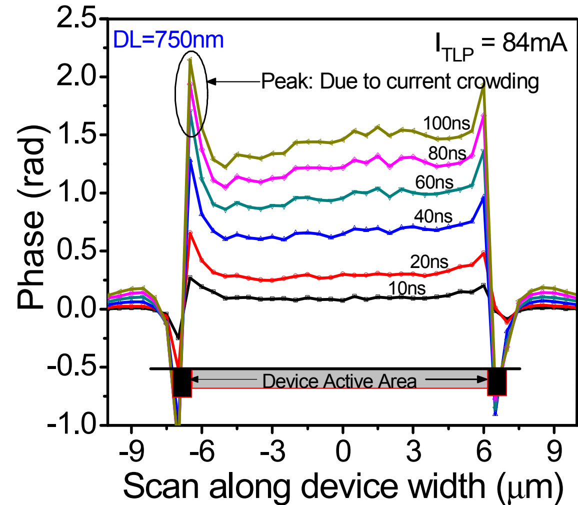

Fig. 5: TIM data for a device with larger DL (750nm). . Phase shift is plotted versus position along the device width under the drain diffusion region . It shows a uniform phase shift evolution across the device active width even at 5X higher current, i.e. no early filamentation..

B. Impact of Pulse Width: To probe the nature of filament, pulses of varying duration are applied. It is well known that devices like ggNMOS, which exhibits thermal fails, have a power law relation between It2 and pulse width [13]. Figure 6 shows a power law dependence for DL=750nm devices, which clearly validates that they fail due to thermal filament formation. On the contrary, It2 of device with small DL (75nm) shows an abrupt dependence on TLP pulse width. It has power law dependence for pulse widths lower than 40ns, which abruptly changes to a saturated value for longer pulses (fig. 6). This is interpreted as a signature of an early fail when an electrical instability occurs at ~40ns. This unique pulse width dependence in DL=75nm device can be seen in conjunction with the findings of filament formation by TIM investigations (fig. 4). In order to understand the physics behind the different behavior, 3D TCAD simulations are performed in section V.

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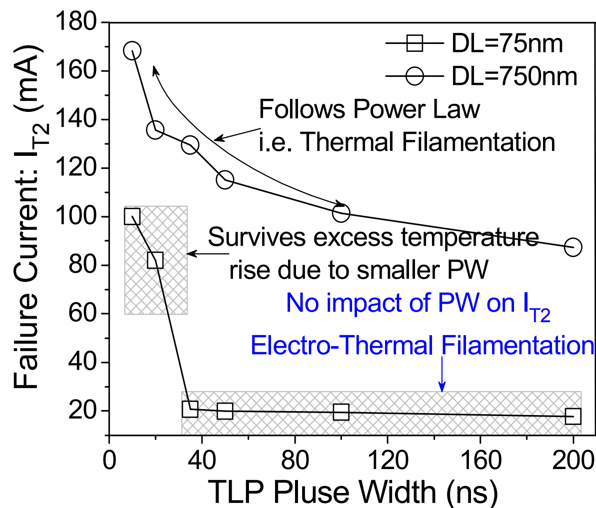

Fig. 6: Impact of pulse width on failure threshold, extracted from TLP measurements, for devices with (a) DL=75nm and (b) DL=750nm. Figure shows, that devices with higher DL follow power law. However, for devices with smaller DL failure current is independent on pulse width for times larger than ~ 40 ns.

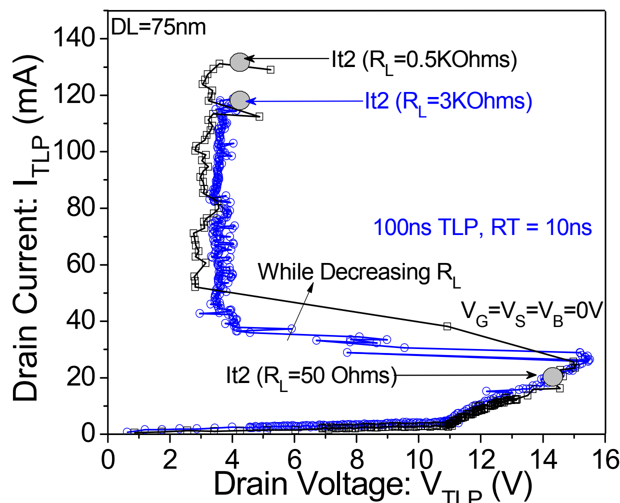

Fig. 7: Measurement of impact of load resistance on the TLP characteristics for devices with smaller DL (75nm). Fig. 1b shows circuit with DUT.

C. Impact of External Load Resistance: Fig. 7 and 8 demonstrate influence of an external serial drain resistance on device types exhibiting (i) electrically driven filamentation (DL=75 nm) and (ii) thermal fails (DL=750 nm), respectively. When an external load resistance was added, a device with DL=75nm undergoes a non-destructive snapback state with a low holding voltage between 3 and 4 V. This behavior further supports the idea that this snapback is not a thermal driven runaway, but an electrical phenomenon. The assumption is, that a filament is formed, which can spread without exceeding a critical temperature due to the slow increase in current [14]. The device with DL= 750nm does not snap back to low holding voltage, but shows two small snap back excursions to about 11V. The turn-on of the second finger of the double finger structure at 60 mA can clearly be seen. This indicates a different field and current distribution in this structure compared to devices with small DL, which goes beyond current spreading due to ballasting resistance. The thermal failure of this device is comparatively less affected by an external load (Fig. 8). The small improvement in It2 is due to current ballasting under thermal filamentation – a case similar to ggNMOS [13].

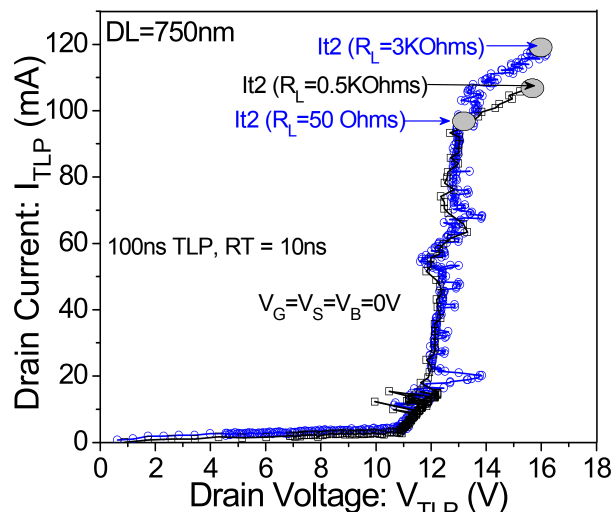

Fig. 8: Measurement of impact of load resistance on the TLP characteristics for devices with larger DL (750nm). Fig. 1b shows circuit with DUT.

V. Current Filamentation and Failure Modelling

***A. Device Behavior**:* A schematic TLP characteristic is shown in fig. 9(i), which is indicating various current levels of interest. Figure 9 (ii) gives a cross section of DeMOS structures highlighting the current paths and high field regions of the device. Two distinct regions in the device are considered. The first one is at the Nwell-to-Pwell junction, where the junction breakdown takes place at point-(a) for both devices. Under such a condition, the peak electric field is located within region-1 and current flows through path-1 - as shown in fig. 9(ii). Moreover, since source/channel region and substrate contacts of both the devices are the same, they both show similar parasitic bipolar turn-on at a lower current level of ~0.3mA/μm, which is shown as point-(b) in fig. 9(i).

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At this condition majority carrier flow starts to be dominating along path-2, whereas, peak electric field is still located within region-1. The difference appears at increased current density levels, where the device with DL=75nm exhibits base push out at point-(c) and fails. Under such a condition, peak electric field shifts from well junction (region-1) towards the highly doped drain diffusion (region-2) as shown in 9(iii) and 9(iv). A device with DL=750nm still has the similar current and field distribution at point-(d) & (e) as it has at point-(b). Finally, devices with DL=750nm shows a thermal fail at point-(f).

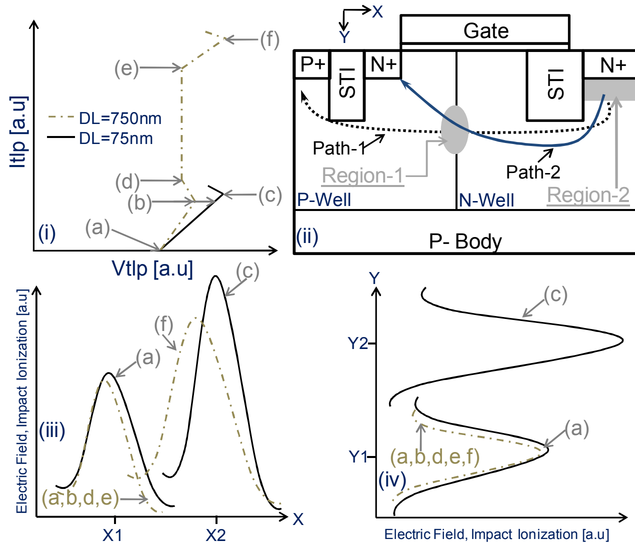

Fig. 9: Figure shows distinct behavior of various investigated devices at different current levels during the overall TLP stress. (i) TLP characteristics showing different current levels of interest, characteristics, (ii) DeNMOS device shows various regions and current paths of interest for further discussion, (iii) & (iv) x & y cut of Electric field/impact ionization profiles inside the device at different levels shown in the TLP. (Note: points X1 and X2 along X-axis represent well junction and drain diffusion respectively. Similarly, Y1 and Y2 along Y-axis represent Nwell-Body junction and point underneath drain diffusion.

B. Filamentation and Failure Modeling: To understand the filament formation and failure mechanism, 3D TCAD simulation is performed using a commercial device simulation tool [15] with well calibrated parameter and model sets [7]-[9]. Figure 10 shows 3D TCAD predictions of current and temperature distribution along the device width for a device with large DL at high current density close to It2 (i.e. point-f in Fig. 9). The predicted uniform distribution along the width is in full agreement with TIM results presented in figure 7. Figure 11 reproduces the current flow and filament formation in device with DL=75nm. As shown in figure 11a, at point-a (of fig. 9(i)) current is uniformly distributed across the whole device width and the peak electric field is located at the Nwell-to-Pwell junction. At the onset of charge modulation (Fig. 11b), current is still uniformly distributed across the whole device's width; however, the peak electric field is shifted to the N^+-Nwell junction unlike to a device with DL=750nm. Adding a drain resistance (of 500 Ohms or higher) to a device with DL=75nm allows the device to survive even higher stress currents while maintaining the deep snap back during filament formation. Fig 11c shows that the peak electric field and drift current is then localized in a narrow filament, which forms a localized hot spot underneath the drain contact region. Finally the fail occurs at this location (fig. 12).

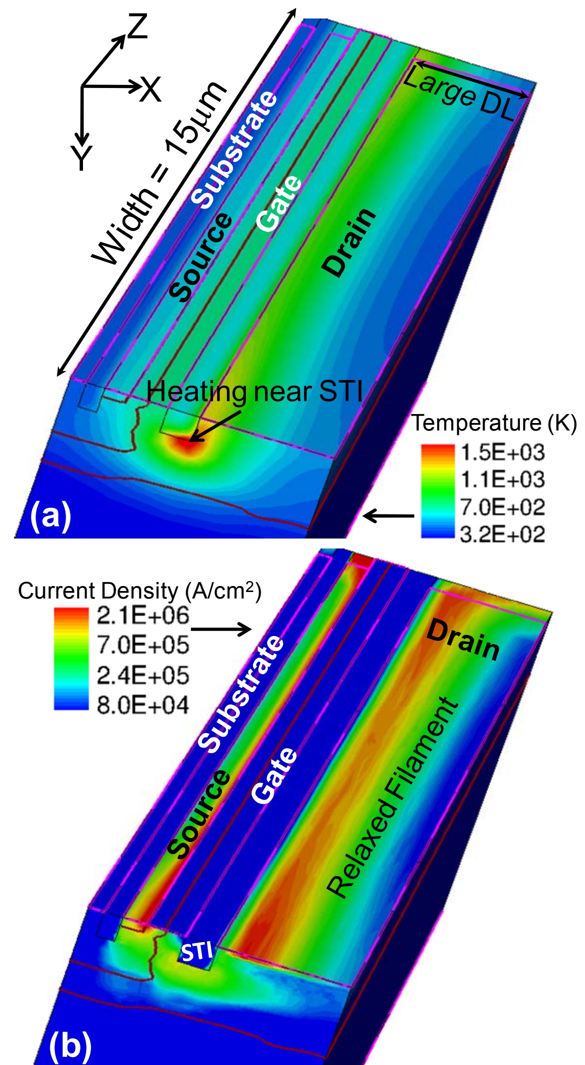

Fig. 10: (a) Lattice temperature and (b) current density distribution across the width for device with DL=750nm @ I_{TLP}=3.3mA/µm and time=100ns. Figure shows significantly widened current filament even at very high temperature and indicates full exploitation of intrinsic thermal failure threshold of device with higher DL (750nm).

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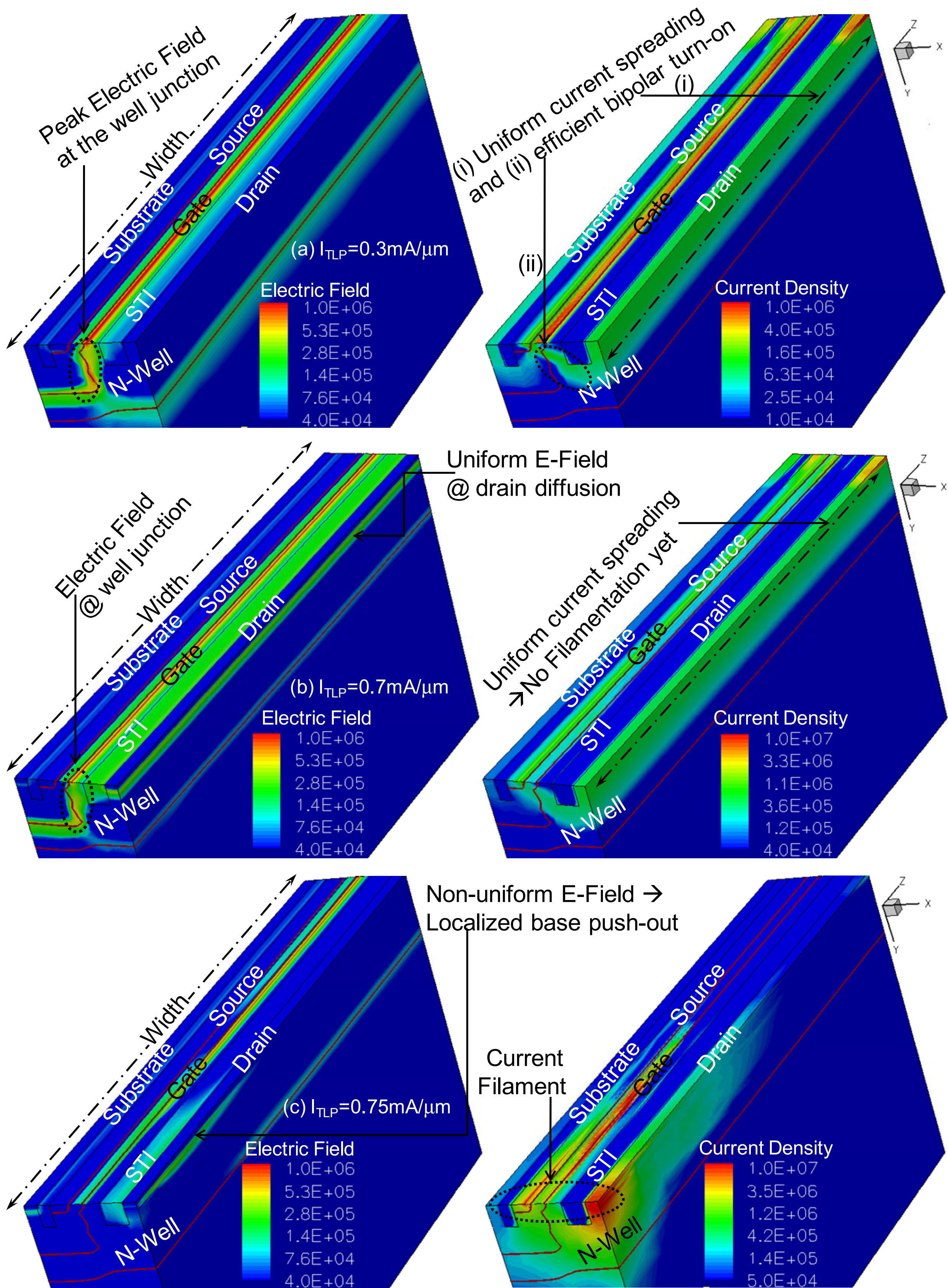

Fig. 11: 3D Electric field [V/cm] and current density profiles [A/cm^2] (a) at the onset of bipolar turn-on, (b) at the onset of base push-out and (c) right after the base push-out.

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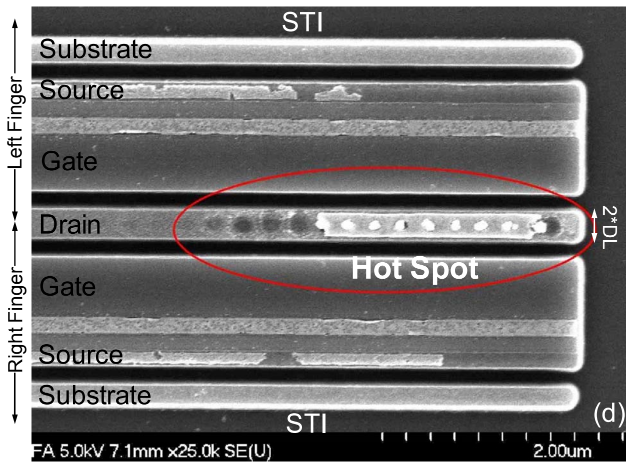

Fig. 12: SEM picture of the failed device with DL=75nm.

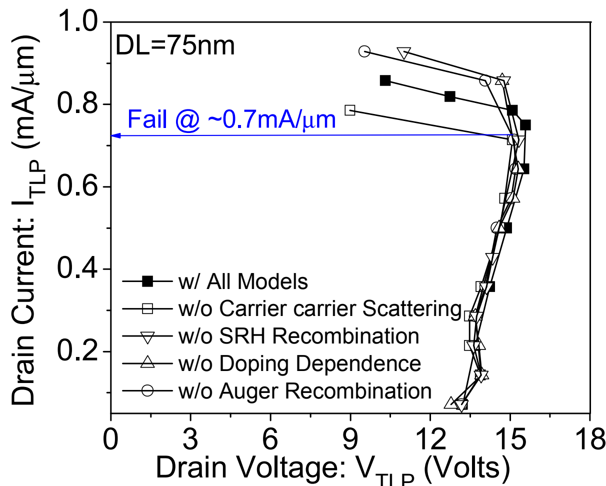

Fig. 13: 3D simulated TLP characteristics of device with DL=75nm by switching off different models affecting the carrier life time. It shows that (i) Carrier-carrier scattering (ii) Auger recombination (iii) Doping dependence mobility degradation and (iv) SRH-recombination have negligible effect on failure threshold.

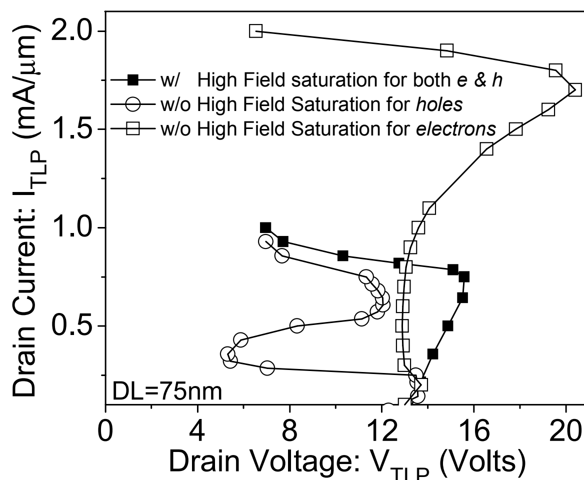

Fig. 14: 3D simulated TLP characteristics of device with DL=75nm when switching on and off different mobility models affecting the carrier mobility under high electric field conditions.

To understand the interaction between space charge modulation, high electrical field and current flow during the formation of filaments a sensitivity study of various mobility degrading mechanisms are performed for a device with small DL. The simulated TLP I-V characteristic doesn't show any effect by modification of low field mobility degradation and carrier recombination (i.e. carrier-carrier scattering, auger recombination, doping dependent mobility degradation and SRH recombination) (fig. 13). The snapback and the fail extracted from peak temperature occur at the same current level. However, the variation of high field mobility degradation, as studied in fig. 14, shows an interesting behavior. Turning off the high field degradation of hole (minority charge carrier) mobility leads to an enhancement of snapback at low current levels. This is attributed to an efficient turn-on of parasitic bipolar due to high mobility of minority carriers entering the base of NPN from the high electric field region (i.e. Nwell-to-Pwell junction). Still It2 is similar to the reference simulation with hole and electron mobility degradation model switched on. While performing same study for electrons (majority charge carriers) a doubling of It2 level can be detected (fig.14). These observations eventually give an indication that (i) current filament formation with immediate thermal fail is linked with degradation of majority carrier mobility under high electric fields and (ii) bipolar triggering is not the driving force for current filamentation and fail. Probing the physical parameters, current density and temperature, shows an abrupt change to a localized current path after 40 ns in the simulation taking into account high field mobility degradation (fig. 15a-b), which is not visible, when high field mobility degradation is switched off (fig. 15c-d). As soon as the localization occurs, an instant rise of temperature to very high values can be detected in figure 15(a-b), which will finally cause the fail.

In order to analyze this further, electric field and electron mobility have been extracted with respect to stress time at the location, where filament starts to appear (fig. 16). Two cases, with and without applying high field mobility degradation model, have been investigated. The observations are as follows: As stress time increases (for a given stress current), the device exhibits higher and higher electric field underneath the N+ drain diffusion (fig.16a), while electron mobility drops to a very low value until ~40ns (fig. 16b). At this point in time the electric field sharply decreases, which coincides with the filament

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formation. The high carrier density inside the filament reduces the peak electrical field due to screening. A small recovery of carrier mobility can be seen (fig. 16b).

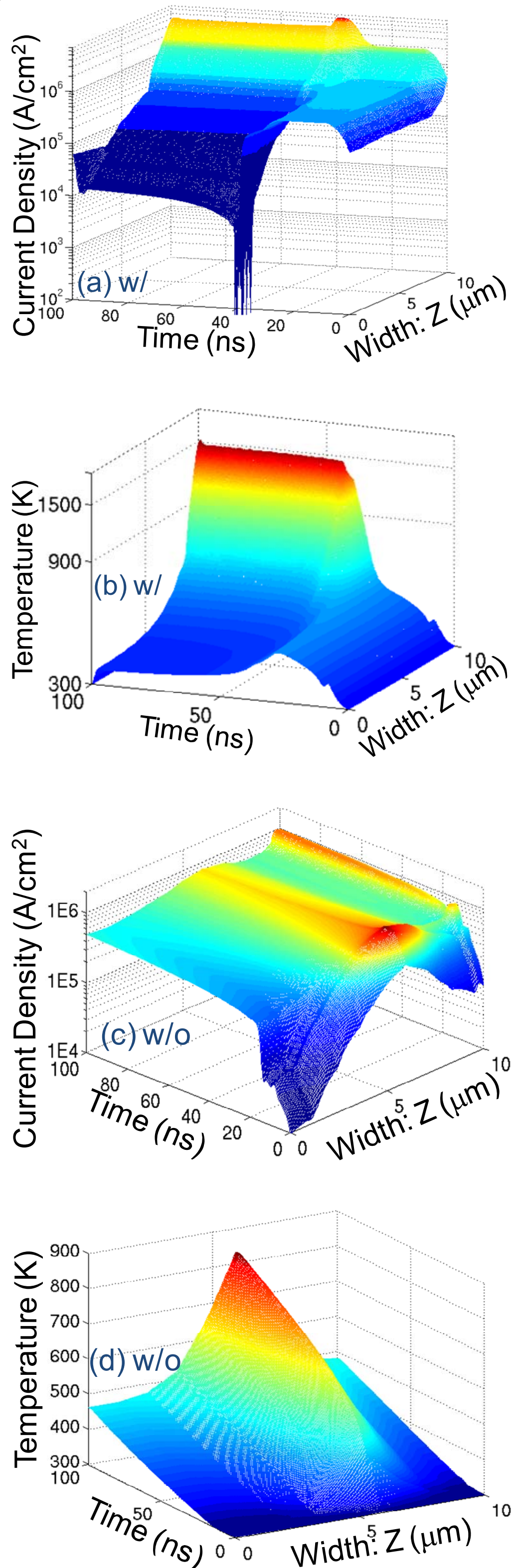

Fig. 15: Simulated (3D TCAD) evolution of current density and lattice temperature with the device's width and stress time (@ I_{TLP}=0.8mA/μm) when high field mobility degradation effect was (a-b) switched-on and (c-d) switched-off. The data was extracted for device with DL=75nm at Loc-A, as shown in fig. 1a, i.e. underneath the N+ drain diffusion region

When high field mobility degradation is switched-off, the region underneath N+ drain diffusion has relatively higher (~5X) carrier mobility compared to the case when this effect was included (fig.16 a). Under such a condition no signature of filament formation could be detected and the device shows a steady (weak) rise in electric field also after 40ns (fig. 16), while keeping electron mobility at a high value.

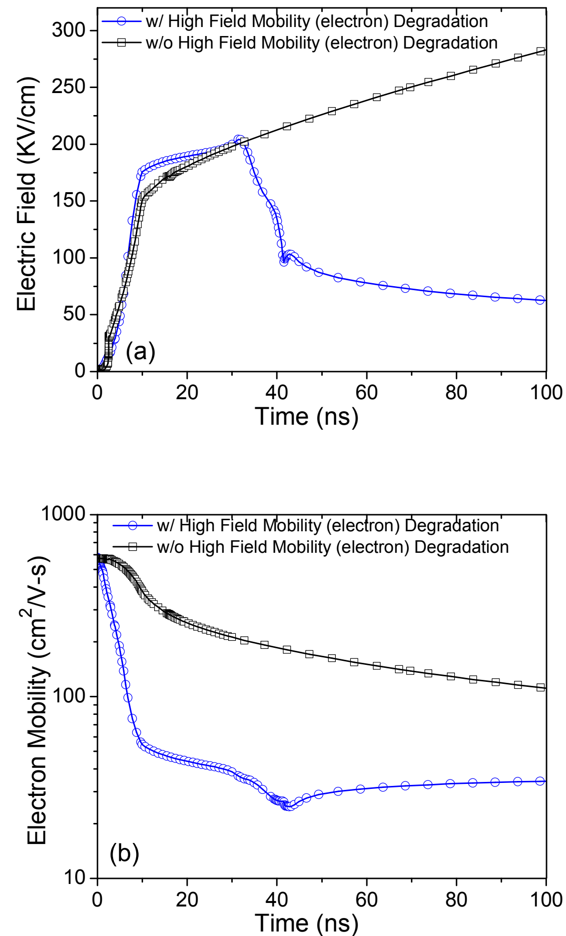

Fig. 16: Simulated (3D TCAD) evolution of (a) electric field and (b) electron mobility with the sress time (@ I_{TLP}=0.8mA/μm) when high field mobility degradation effect was switched-on and switched-off. The data were extracted for a device with DL=75nm at the location-A in 2D plane (as shown in fig. 1a, i.e. underneath the N+ drain diffusion region).

Thus, the physical picture of the formation of a current filament or an electrical instability can be described the following way: the rise in electric field (E) to high values underneath N+ drain diffusion during base push out (= charge carrier modulation of the drain extension area) leads to a strong decrease in carrier mobility (μ) (E↑→μ↓). This is due to high (optical) phonon scattering rate of high energy electrons. To overcome the problem of increasing

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resistance, the system forms a filament of very high charge carrier density, which modifies the electrical field inside the filament. The reduced peak electrical field enhances mobility. A rise in carrier density (n) also screens the optical phonon- carrier scattering, improving mobility even further. This effect is described by the relation $\tau=\tau_0[1+(n/n_c)^2]$, where τ is the effective scattering time, τ_0 is the scattering time at low current density, n is the carrier density and n_c is the critical carrier density required for the screening of optical phonon from carrier scattering [16]. These factors together make the formation of a filament favorable. The process can be summarized as: E↑ ➔ μ↓ ➔ filament formation ➔ n↑ ➔ E↓ ➔ μ recovers.

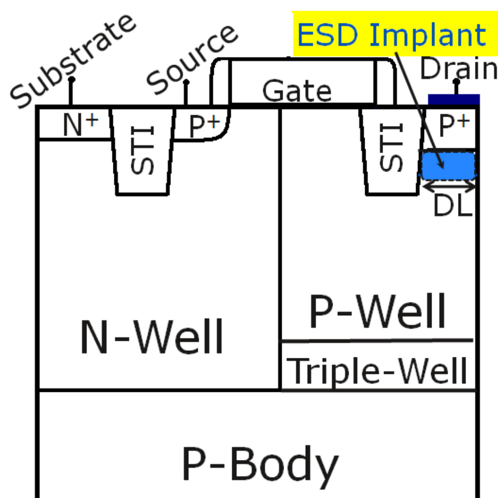

Fig. 17: Modified P-DeMOS device cross-section with p ESD implant. Length of P+ drain diffusion is denoted as DL.

VI. Robust P-DeMOS devices

In this section our understanding of physical phenomena, from section-V, is applied for engineering an ESD optimized p-type drain extended MOS device. Fig. 17 shows cross-sectional view of a P-DeMOS device including an ESD related implant underneath P^+ drain diffusion. The previous investigation has proven that avoiding high electrical field is the key to mitigate the filament formation. As the high field appears after base push out, avoidance of this at lower current levels e.g. by increasing DL, should be beneficial. This is shown in figure 18. The increase of DL of the P-DeMOS improves It2 by 5X similar to N-DeMOS. In addition, the base push out can be shifted to even higher current levels by engineering of the doping profile of the drift region underneath the highly doped drain. In this work a deep p-type implant with higher doping level than the P-well but lower than the P+ drain is added. This changes the doping profile at P-well/P+ drain junction from $P^{(+)}$-$P^{(-)}$ to a more graded $P^{(+)}$-P-$P^{(-)}$ type profile. This eventually increases It2 by a factor of 2.4 for small DL devices (fig. 18). TCAD simulation shows, that these measures, (i) higher DL value and (ii) ESD implant underneath $P^{(+)}$ drain diffusion, can also be combined achieving a 6X improvement of It2. P-type ESD implant can easily be made available in state-of-the-art CMOS processes. These measures allow improvement of P-DeMOS ESD robustness to an It2 level sufficient enough for their use as self-protecting I/O drivers.

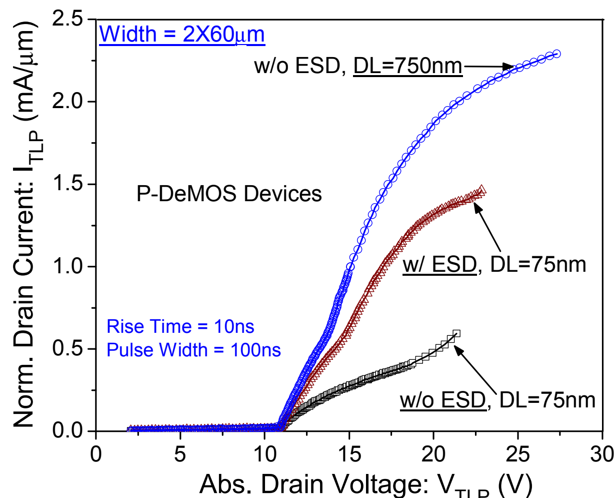

Fig. 18: Measured TLP characteristics of various P-DeMOS devices with DL of 75 nm and 750 nm and a width of 2 x 60 µm. Both process options with and w/o p-ESD implant were investigated.

VII. Conclusion

We have presented experimental evidence of more than 5X improvement in the ESD failure current of state-of-the-art grounded gate DeMOS devices manufactured in 65nm CMOS, reaching a very high It2 value of 3.3mA/µm. This has been achieved by widening the drain diffusion region. The improvement is not related to drain ballasting as commonly applied for low voltage NMOS devices, but by suppressing the onset of filament formation. Full silicidation of the drain region is possible without compromising Ron performance. Early fail of the standard device is explained by electrical instabilities at the onset of space charge modulation. This was verified by TIM investigations, detailed TLP analysis and 3D TCAD device simulation. Design and technology measures controlling these electrical parameters are proposed in order to achieve better intrinsic ESD robustness. The optimization concepts are not limited to drain extended devices in advanced CMOS but can be

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applied to any high voltage device using lowly doped collector or drain regions.

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