Drain Extended MOS Device Design for Integrated RF PA in 28nm CMOS with Optimized FoM and ESD Robustness

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Abstract

This paper explores drain extended MOS (DeMOS) device design guidelines for an area scaled, ESD robust integrated radio frequency power amplifier (RF PA) for advanced system-on-chip applications in 28nm node CMOS. Simultaneous improvement of device-circuit performance and ESD robustness is discussed for the first time. By device design optimization a 45% increase in gain and 25% in power-added efficiency of RF PA at 1GHz, and 5× improvements in ESD robustness are reported experimentally.

Introduction

Advanced system-on-chip (SoC) concepts push to integrate all the functionalities on the same Si Die including high power radio frequency power amplifiers (RF PA) and power management modules [1]-[2]. State-of-the-art high power RF PA is realized by discrete III-V devices [3]. However, integration of these device types on Si substrate is not trivial. Therefore, for CMOS based advanced SoC, a Si based solution has to be explored. Drain extended NMOS (DeNMOS) device is a potential candidate for such applications in advance CMOS nodes [4]-[5]. The challenge for implementation of an integrated RF PA into a sub-65nm node CMOS is low breakdown voltage, sensitivity towards ESD stress and nonlinear device characteristics. This paper discloses DeMOS device design guidelines for designing an integrated high performance RF PA with an excellent ESD robustness.

Experiments and Results

DeNMOS device (Fig. 1) was fabricated in 28nm CMOS technology node, using process and design rules developed for low power devices. Total fabricated electrical width of the device was 1.6mm. In order to study device's suitability for RF PA application, the RF circuit was mounted on a test board. Schematic of the PA circuit is shown in Fig. 2a along with the biasing and matching networks. A capacitor ladder is used at the DC supplies in order to de-couple the RF noise generated by the circuit from DC. Fig. 2b shows the photograph of the fabricated PA circuit prepared on a low loss laminate. Small signal s-parameter measurements were conducted on die, to design the matching and biasing network for the RF PA (Fig. 3). The DeNMOS device's gate was biased slightly above the threshold voltage in order to operate the PA in class-AB mode. Output power of the PA was

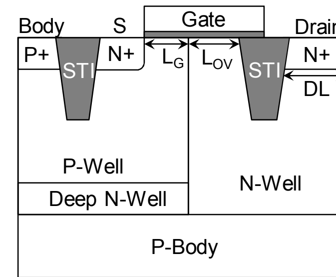
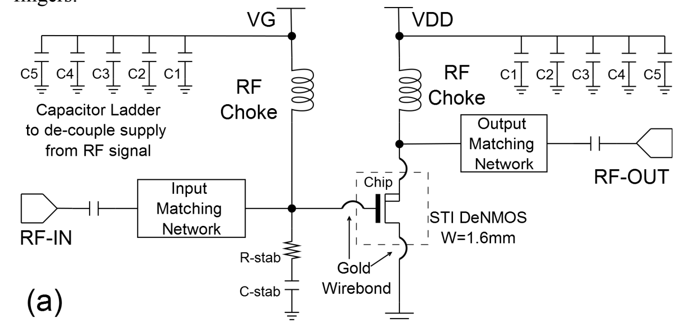


Fig. 1: Cross-sectional view of the DeNMOS device fabricated in 28nm CMOS node. Figure depicts a single finger structure; however, it is realized in a two finger configuration on silicon with sharing of N-well between two fingers.



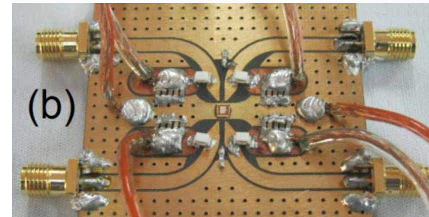


Fig. 2: (a) RF PA circuit, which is used as a vehicle to analyze RF PA performance of the advance CMOS node DeNMOS devices manufactured in this work. (b) Board level implementation of RF PA for device-circuit co-design and RF PA performance analysis. A low loss laminate of thickness = 0.8mm (TanD = 0.0004), dielectric constant = 2.2 and copper cladding of 70µm was used for board level implementation. Electrical connections from die to PCB were made using 25µm gold wire. Die is pasted using thermal conductive epoxy for proper thermal transport as junction temperature rise can be a serious issue to the structure [6].

measured for a 50Ω load, as shown in Fig. 4. RF PA using the standard DeNMOS device offers an output power of 23.9dBm at 1-dB compression point ($P_{1\text{-dB}}$), which corresponds to a power density of 0.16 W/mm, at 1 GHz. Measured RF gain of the PA circuit is 10.8dB, peak drain-efficiency is 46% and power added-efficiency (PAE) is 40.2% at 1-dB compression point. RF distortion produced by

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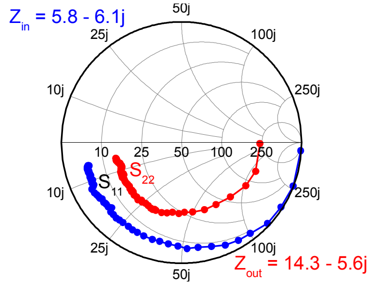

Fig. 3: S-parameter measurement results (S_{11} & S_{22}) for the 1.6mm (electrical width) standard DeNMOS device, which are used for designing matching network for RF PA (Z_{in} and Z_{out} are shown for 1GHz).

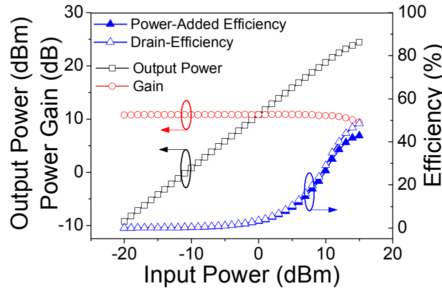

Fig. 4: Performance of the implemented DeNMOS based RF PA, extracted experimentally using class-AB mode of PA operation and tested at 1GHz.

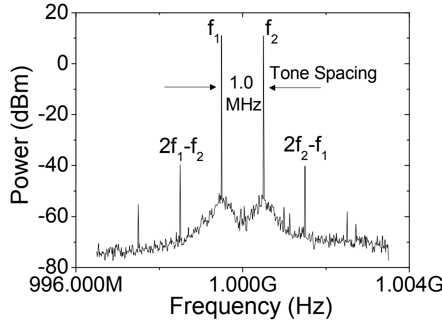

Fig. 5: Circuit response to two-tone signal excitation measured at 0dBm input power. The spectrum shows two fundamental tones (f_1 and f_2) along with two 3rd order harmonics ($2f_1$-f_2 and $2f_2$-f_1) generated due to the non-linearity in the device.

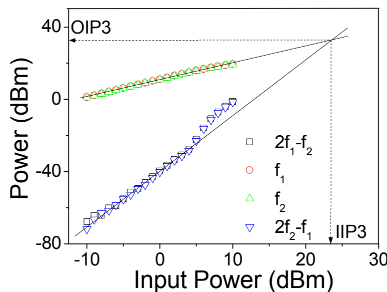

Fig. 6: Two-tone output power measurements of the standard DeNMOS based RF PA design as a function of input power. Both the plots were extrapolated to calculate IIP3 and OIP3.

the device is very critical for deeply scaled technologies [7]. In order to explore linearity of the device for RF applications two-tone measurements were performed. Two sinusoids (f_1 and f_2) centered at 1GHz with a tone spacing of 1MHz were applied at the circuit input port. Fig. 5 shows the output power spectrum and the third harmonic frequency ($2f_1$-f_2 and

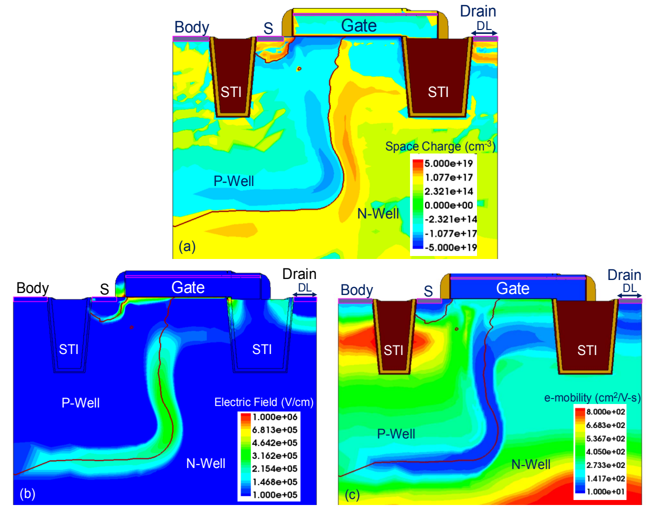

Fig. 7: (a) 2D Space charge contour across the standard DeNMOS device at high drain current (V_G=2V, V_D=5V). Figure depicts significant amount of space charge modulation at high drain current, which may be a possible cause of mitigated device performance and early quasi saturation. (b) 2D electric field contour across the standard DeNMOS device at high drain currents. Figure depicts very high electric field underneath the drain diffusion and in the gate-to-N-well overlap region. High electric field in the drift region is attributed to an early space charge modulation leading to localized field distribution. (c) 2D electron mobility contour across the standard DeNMOS device at high drain current. Figure depicts significant electron (majority carrier) mobility reduction in the drift region, especially under the drain diffusion (or drain N+) and Gate-to-Nwell overlap region. Mobility reduction is attributed to very high electric fields in these regions due to an early space charge modulation.

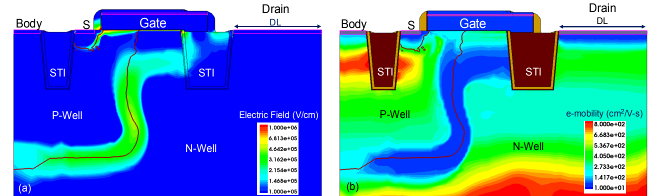

Fig. 8: 2D (a) electric field and (b) electron mobility contour across the modified DeNMOS device (DL= 5× of min. allowed) at high drain currents. Figure depicts lowering of electric field under the drain diffusion region, however increased electric field in the Gate-to-Nwell overlap region. Lowering of electric field is attributed to absence of space charge modulation underneath the drain diffusion, which results in an improved electron mobility in this region.

$2f_2$-f_1) power spectrum generated due to the device's non-linearity. Two-tone measurements (Fig. 5 & 6) show an excellent inter-modulation distortion (IMD3) level of -72dBm at -10dBm of input power. Fundamental and harmonic powers were extrapolated to obtain the input and output third order intercept points (IIP3 and OIP3 respectively). RF PA offers 37dBm of output 3rd order intercept point (OIP3), which is >10dB higher than $P_{1\text{-dB}}$.

Quasi-Saturation, Device Design & RF PA Performance

To optimize DeMOS devices, quasi saturation leading to g_m drop needs to be reduced. Device TCAD simulations were performed under high current condition. Fig.7a shows an early space charge modulation, which leads to localized electric field peaking underneath the drain diffusion (i.e.

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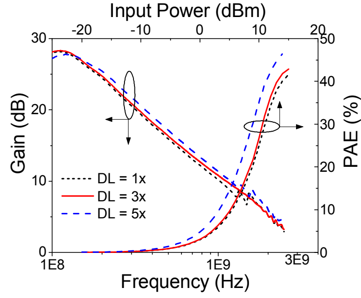

Fig. 9: Measured small signal gain and power added efficiency of the RF PA circuits realized using DeNMOS devices of different drain diffusion lengths (DL). A clear increment in both Gain and PAE can be seen after drain engineering.

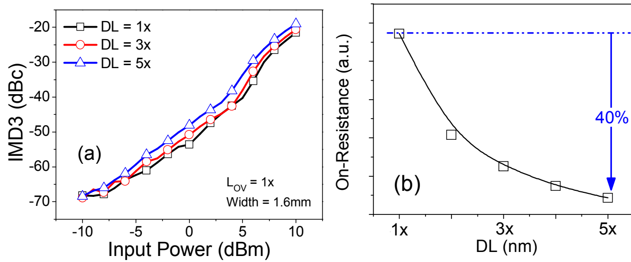

Fig. 10: (a) IMD3 level of the drain engineered devices with respect to two tone input power. IMD3 levels are almost unchanged. (b) On-resistance of drain engineered devices. Figure depicts 40% reduction in the on-resistance of the device, which is a significant factor for power management (or switching) applications.

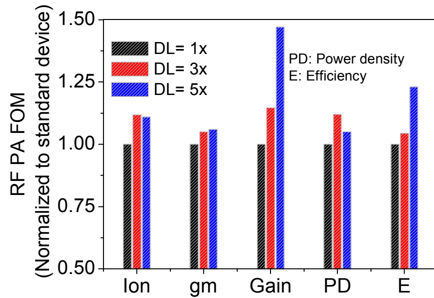

Fig. 11: RF PA FoM improvement after drain engineering. Figure depicts 40%-50% improvement in RF PA FoMs.

drain N+) and within the gate-to-Nwell overlap region (Fig.7b). Increased electric field results in significant mobility reduction across these regions (Fig.7c). As the charge modulation takes place when mobile carriers exceed the background doping, reducing the current density in critical regions should mitigate space charge modulation. Increasing the drain N+, drain diffusion length (DL) successfully reduces current density and mitigates electric field peaking and electron mobility reduction (Fig. 8). This has resulted in an improved device with increased ON-current, lower on-resistance, increased trans-conductance and load line swing when compared to the standard device. The RF PA performance (Fig. 9-11), shows 45% improvement in RF gain and 25% improvement in PAE. Fig. 10b shows 40% reduction in the on-resistance of the DeNMOS device by drain engineering.

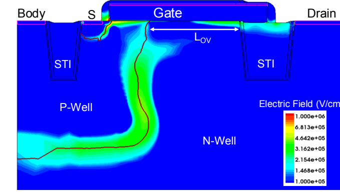

Fig. 12: Lowering of the electric field in the gate-to-Nwell overlap region by engineering the overlap length and thereby doping profile.

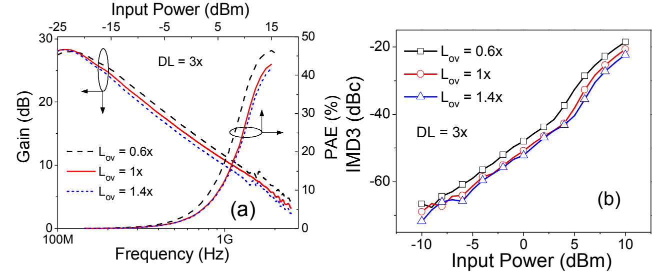

Fig. 13: (a) Measured small signal gain and power added efficiency of the RF PA circuits realized using DeNMOS devices of different gate-to-Nwell overlap length (L_{OV}) and thereby doping profile. (b) IMD3 level of the gate-to-Nwell overlap engineered device based RF PA.

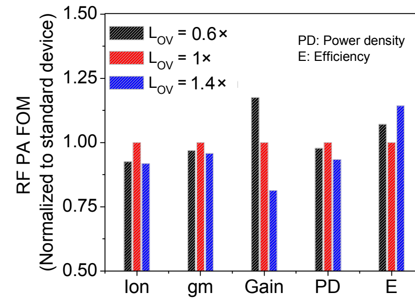

Fig. 14: Gate-to-Nwell overlap engineered device and implemented RF PA FoM.

In order to avoid electric field peaking in the gate-to-Nwell overlap region, the overlap length (L_{OV}) was increased. Although the electric field peaking was mitigated by an increased L_{OV}, (Fig. 12), the RF PA characteristics and FoM show a non-linear trend (Fig. 13 & 14). This can be attributed to the trade-off between Miller/overlap capacitance, non-linearity in the trans-conductance, drain parasitic capacitance and drift region resistance.

ESD Robustness

PA circuits are directly connected to the antenna and exposed to ESD threats. Thus, ESD robustness is an essential feature of PA driver stage. Standard DeNMOS device with smallest DL value is intrinsically ESD weak (Fig. 15a). The root cause is the early current filament formation (Fig. 16a) due to field peaking and mobility degradation. Avoiding the early space charge modulation underneath the drain diffusion, by increasing DL, mitigates an early filament formation (Fig. 16b), which improves the ESD robustness by 5× (Fig. 15a & 15b). This highest reported ESD robustness of DeNMOS device [8] allows the implementation of a self-protecting PA stage without need of an additional ESD protection.

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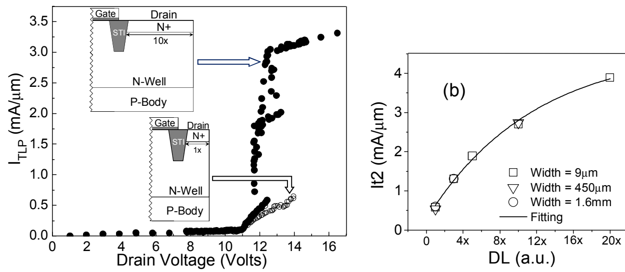

Fig. 15: (a) TLP characteristics of conventional and modified drain engineered device. Figure clearly depicts significant improvement in the device's ESD robustness by drain engineering. (b) Consistent improvement in the failure current (It2) by increasing drain diffusion length.

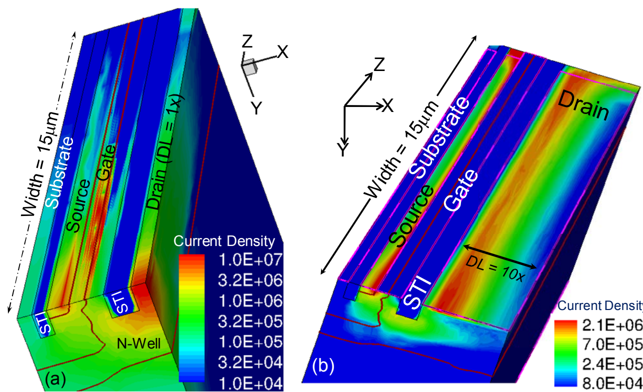

Fig. 16: (a) 3D TCAD pictures depicting current filamentation in the standard DeNMOS device at low currents (I_{TLP} = 0.5mA/µm). (b) Device survives filamentation after drain engineering, even at very high currents (I_{TLP} = 0.5mA/µm).

Self Heating and Technology Scaling

Increase in the die temperature due to high power consumption and limited efficiency of the circuit is a serious issue to the device reliability for power applications. In order to investigate temperature rise across the device, thermal mapping over the Si Die was performed using thermocouple probe tip. The Die temperature, at 24dBm of RF power level, was found to be 25°C above room temperature, which was scaled down to 18°C after device optimization (Fig. 17a). This is in agreement with an increased PAE after device optimization. A scaling of this temperature level to 1 Watt (30dBm) for SoC applications is therefore feasible. An area comparison shows that the DeNMOS based RF PA in 28nm node CMOS occupies 6× less area, for a given power level, compared to the 5 stack silicide blocked NMOS transistor based RF PA (Fig. 17b). As shown, the 5 stack silicide blocked RF PA requires separate RC network at each transistor gate in order to sustain high signal swing at the output node without exceeding gate oxide breakdown voltage. Another way to increase the output power is to stack more transistors. However, in 28nm and beyond, stacking of more than 5 transistors is not possible due to limited drain-to-pwell and nwell-to-pwell reverse bias breakdown voltages. To explore the on-chip integration of PA for advanced CMOS, the scaling trends are compared in Fig. 18. This work shows competitive FoM for RF PA in the most advanced CMOS technology node. Due to the simplicity and process

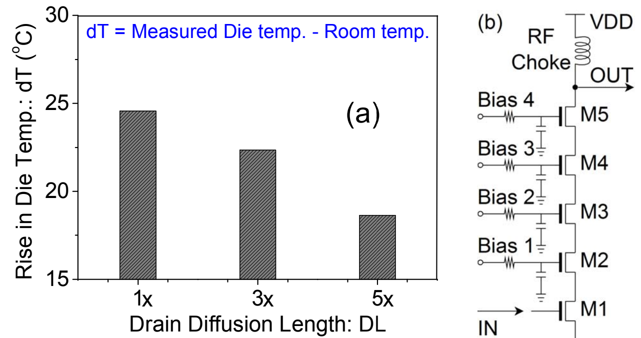

Fig. 17: (a) Rise in Die temperature as a function of drain diffusion length, measured at 24 dBm of RF power level. (b) 5 stack silicide blocked NMOS transistor based RF PA circuit. A stack of 5 transistors are required to achieve a maximum voltage swing in 28nm technology (10V). Note the additional area required by the bias network for individual transistor gates. (De-coupling cap and other details are skipped from this figure for simplicity.)

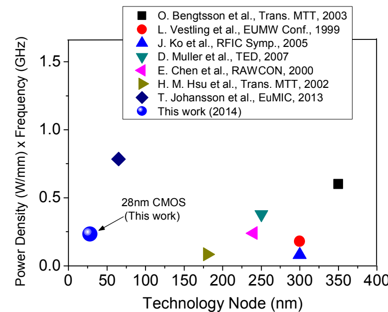

Fig. 18: Figure depicts power density vs. technology nodes of various DeMOS/LDMOS based RF PA implementations. A clear area advantage can be seen for an integrated RF PA in advanced CMOS nodes.

compatibility of DeNMOS device used in this work, it can be integrated into even further scaled technologies with only minor process cost penalty.

Conclusion

A power amplifier based on a STI DeMOS device has been realized in 28 nm CMOS. For a drain to source breakdown voltage of 10V, a high output power of 24dBm, power density of 0.16W/mm at 1GHz with efficiency of 50% has been reported. Thus, STI DeMOS can provide an option for integrating PAs with good intrinsic ESD robustness in advanced CMOS nodes for applications with limited frequency and performance requirements. To optimize the RF performance of the device the field distribution on the drain side has been discussed and an optimization strategy is provided.

References

[1] R. Kumar, et. al., *ISSCC*, 2014. pp. 328-329.
[2] C. H. Wu, et. al., *RFIC Symp.*, 2013. pp. 129-132.
[3] U. K. Mishra, et. al., *Proc. of IEEE,* 2008. pp. 287-305.
[4] T. Johansson, et. al., *Trans. on MTT,* 2014. pp. 111-124.
[5] D. Gruner, et. al., *Trans. on MTT,* 2010. pp. 4022-4030.
[6] A. Ferrara, et. al., *IEDM*, 2013. pp. 168-171.
[7] R. V. Langevelde, et. al., *IEDM,* 2000. pp. 807-810.
[8] M. Shrivastava, et. al., *IEEE TDMR*, 2012. pp. 615-625.

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