Comparison of Breakdown Characteristics of DeNMOS Devices with Various Drain Structures

Ketankumar H. Tailor[1*], Mayank Shrivastava[2], Harald Gossner[3], Maryam Shojaei Baghini[1], and V. Ramgopal Rao[1]
[1]Department of Electrical Engineering, Indian Institute of Technology Bombay, Mumbai 400076, India
[2]Department of Electronic Systems Engineering, Indian Institute of Science, Bangalore 560012, India
[3]Intel Mobile Communications GmbH, Munich, Germany
[*]Email: mailto:ketanht@ee.iitb.ac.in

***Abstract*—In this work, OFF-state breakdown characteristics of shallow trench isolation (STI)-type drain extended NMOS (DeNMOS) devices with different drain structures are studied and compared. The drain structures include deep-drain structure and structures with heavy doping on STI-sidewall regions. These devices show improved ON-state resistance without degrading breakdown voltage. Devices with higher doping underneath the drain diffusion region exhibit stronger bipolar triggering and higher snapback in their breakdown characteristics, thereby sustaining higher drain current levels before device failure. The devices with heavy doping only on the STI-sidewall show intermediate snapback characteristics between conventional and deep-drain devices in the breakdown region. Therefore, this work provides physical insights into the impact of different drain doping profiles on low-voltage *I-V* characteristics and high current drain breakdown characteristics of STI-DeMOS devices for different drain doping profiles.**

Index Terms*—Drain extended NMOS (DeNMOS), electrostatic discharge (ESD), hot carrier, mixed-signal performance, input-output (I/O), breakdown voltage, shallow trench isolation (STI).

I. Introduction

Due to low cost process and high drain breakdown voltage of drain extended MOS (DeMOS) devices, they are used in number of mixed-signal circuits like high voltage I/O drivers and RF power amplifiers in low-power SoC applications [1]. With the added shallow trench isolation (STI) structure under gate-drain overlap, DeMOS devices show improved thin gate oxide reliability. The parasitic bipolar snapback in DeMOS under electrostatic discharge (ESD) strike can be used to sustain large drain currents. Hence, DeMOS devices find use in ESD protection applications in CMOS SoCs [2]. Various techniques involving modifications in layout and doping of the drift region and the gate or body biasing schemes have been proposed to further improve the bipolar triggering behavior and avoid current filamentation during ESD events [2]. Some publications have also reported deep drain profile engineering for RESURF LDMOS device, in order to improve the ESD robustness [3]. In this work, a physical comparison is made of OFF-state drain breakdown characteristics of DeMOS devices, in an advanced CMOS technology, with different drain structures. An understanding of the physics of high current drain breakdown characteristics of the DeMOS devices with different drain structures is helpful to improve the overall ESD characteristics.

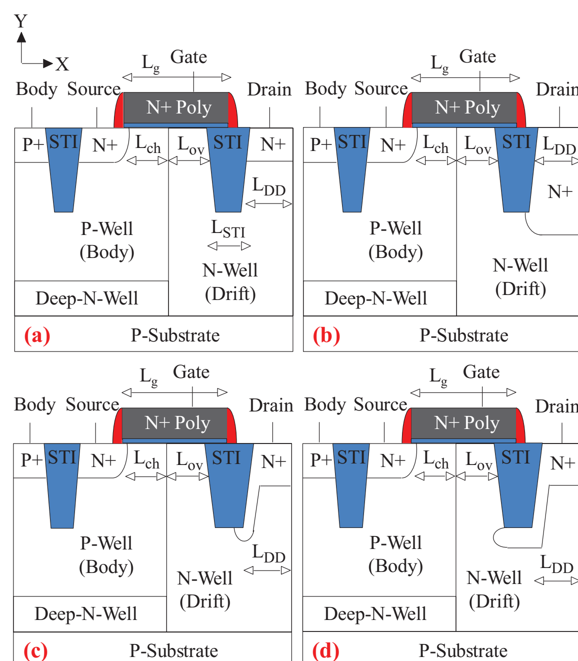

Fig. 1. Schematics of STI-DeNMOS structures under study: (a) conventional device, (b) device with deep drain doping profile (type *A*), (c) device with added heavy doping on right-side of STI sidewall (type *B*), and (d) device with added heavy doping on right and bottom sides of STI sidewall (type *C*).

II. Device Structures and *I-V* Characteristics

A. STI-DeNMOS Device Structures Under Study

Fig. 1 shows the schematics of the STI-DeNMOS device structures under study. The conventional device (Fig. 1(a)) is implemented using a standard low power 65 nm CMOS technology and uses a thin gate oxide of about 2 nm thickness. A shallow trench isolation (STI) structure is added underneath the gate-to-drain overlap region to allow high drain breakdown voltage without affecting thin gate oxide reliability. Since the goal of this paper is to study the impact of drain structure (doping profile under n^+ drain diffusion) on *I-V* characteristics, the devices (Fig. 1(a-d)) are generated using a standard 65 nm process deck. All geometric parameters are kept same in all the devices. The drain structure types of STI-DeNMOS devices studied in this work include the conventional drain diffusion

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(as in the standard CMOS process) (Fig. 1(a)), device with deep n^+ drain diffusion (Fig. 1(b)) (type *A*), and devices with added heavy *n*-type doping (~2e20 cm^{-3}) on STI sidewall regions (Fig. 1(c, d)) (types *B* and *C*).

B. I-V Characteristics

Fig. 2(a) shows simulated OFF-state drain breakdown characteristics at V_{GS} = 0 V of the four STI-DeNMOS devices under study. Since the purpose is to compare the drain breakdown characteristics, hydrodynamic carrier transport model in Sentaurus Device TCAD simulator has been used [4]. Self-heating effects are not included here. The simulated devices show similar OFF-state breakdown voltage V_{BD} (V_{DS} at I_D = 1 nA/μm) and drain leakage current (I_D at V_{GS} = 0 V, V_{DS} = 10 V) (Fig. 2(b)). The experimental breakdown characteristic of the conventional STI-DeNMOS device shows drain breakdown voltage of 10.5 V. In the modified devices under study, heavy doping (~2e20 cm^{-3}) is not added on the left-side of STI sidewall. This is because if heavy doping is added on the all three sides of STI sidewall, then the applied drain voltage drops entirely across the thin gate oxide and, thereby, the OFF-state drain breakdown voltage of the device is severely degraded. As shown in Fig. 2(c), ON-state resistance (at V_{GS} = 1.2 V, V_{DS} = 0.1 V) reduces in devices with deep-drain and sidewall doping due to reduced drift region (*n*-well) (ohmic) resistance in the linear drain current path. Thus, modified STI-DeNMOS devices offer low ON-resistance, while maintaining high OFF-state drain breakdown voltage.

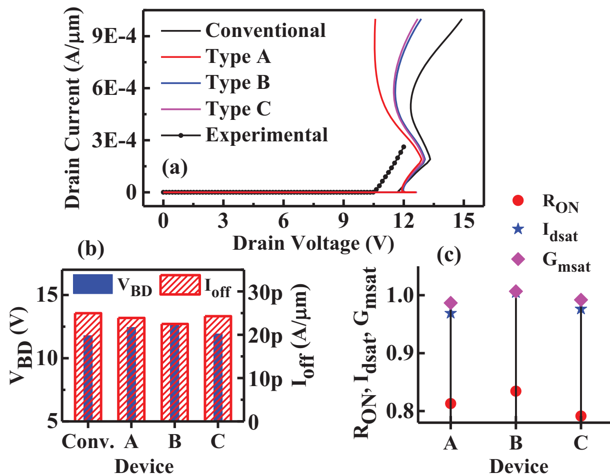

Fig. 2. (a) Simulated OFF-state drain breakdown characteristics (I_D-V_D at V_{GS} = 0 V) of different STI-DeNMOS devices. Measured breakdown characteristic (symbols) of the conventional device is also shown. (b) Comparison of OFF-state drain breakdown voltage (V_{DS} at V_{GS} = 0 V, I_D = 1 nA/μm) and drain leakage current (I_D at V_{GS} = 0 V, V_{DS} = 10 V). (c) Comparison of normalized ON-resistance (at V_{GS} = 1.2 V, V_{DS} = 0.1 V), saturation drain current (at V_{GS} = 1.2 V, V_{DS} = 3.3 V) and peak saturation transconductance (at V_{DS} = 3.3 V). The values in (c) for devices *A*, *B* and *C* are normalized w.r.t. the conventional STI-DeNMOS device.

However, saturation region drain current (I_D at V_{GS} = 1.2 V, V_{DS} = 3.3 V) and peak saturation transconductance (at V_{DS} = 3.3 V) in devices *A*, *B* and *C* show slight degradation compared to the conventional device, due to slight degradation in high field electron mobility in highly doped *n*-type drift region (Fig. 2(c)). The detailed analyses of the impact of the drain doping profiles on the figure of merits of analog and digital circuit performance characteristics of STI-DeNMOS devices will be considered for further study.

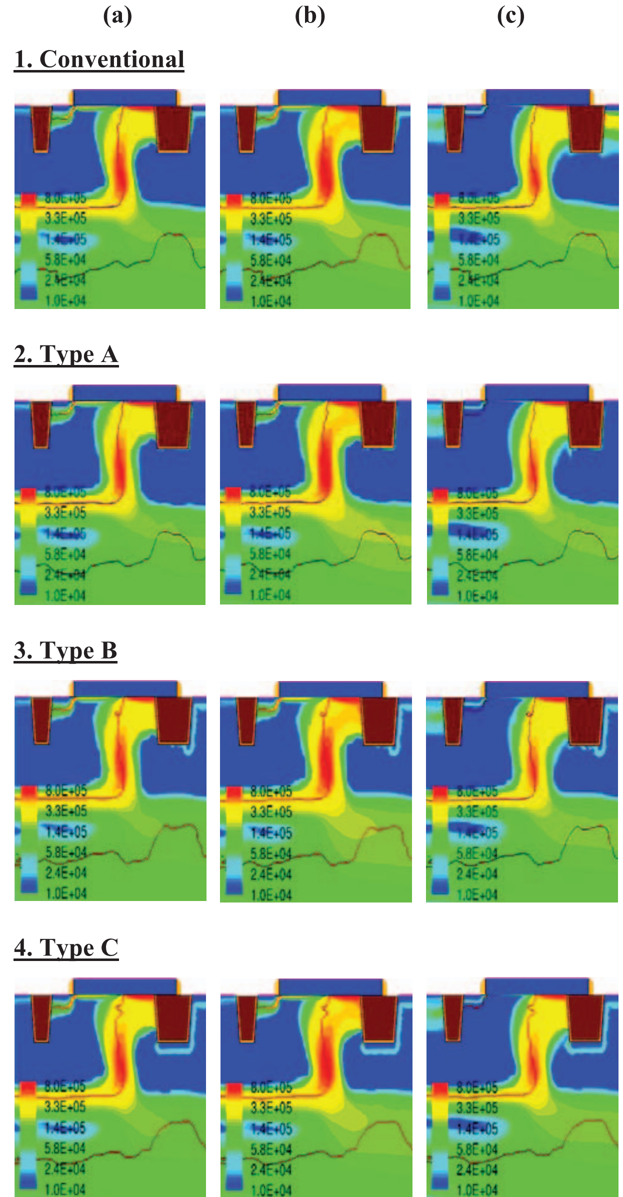

Fig. 3. Electric field (V/cm) contours in silicon region in conventional STI-DeNMOS device and in devices with modified drain structures at V_{GS} = 0 V and (a) V_{DS} = 10 V (pre-breakdown), (b) I_D = 0.1 μA/μm and (c) I_D = 1 mA/μm (post-breakdown).

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III. Detailed Physics of Device Characteristics

As shown in Fig. 2, the STI-DeNMOS devices exhibit similar drain breakdown voltages. However, the differences are observed in the post-breakdown characteristics. The triggering voltage of the parasitic *n-p-n* bipolar is slightly reduced and the snapback in I_D-V_D characteristics is significantly enhanced in devices with deeper drain structures, as compared to the conventional shallow-drain device. This shows that the parasitic bipolar in deep-drain STI-DeNMOS device has same collector-base junction breakdown voltage, slightly lower turn-on voltage and significantly higher collector-to-emitter current gain ratio as compared to the conventional STI-DeNMOS device with shallow drain structure.

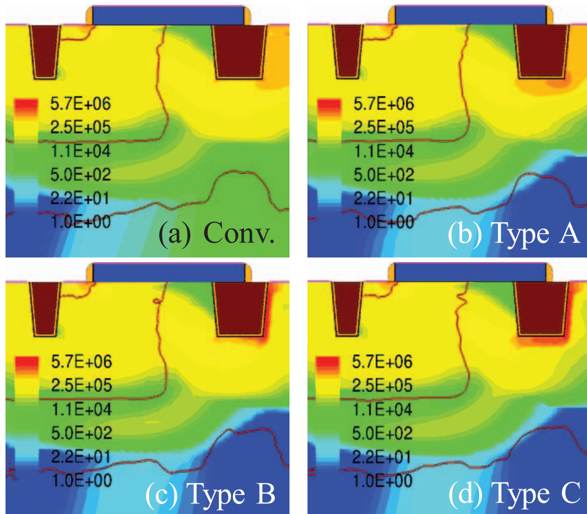

Fig. 4. Conduction current density (A/cm^2) contour at V_{GS} = 0 V, I_D = 1 mA/µm in the different STI-DeNMOS devices.

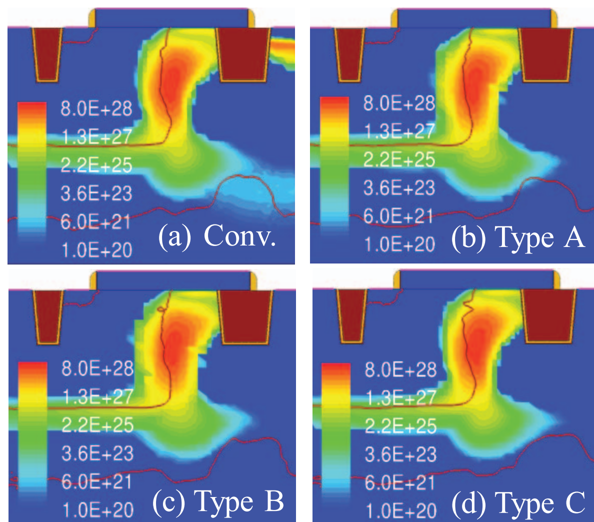

Fig. 5. Impact ionization (1/cm^{3}s) contour at V_{GS} = 0V, I_D = 1mA/µm in different STI-DeNMOS devices.

Also, the snapback I_D-V_D characteristics of devices *B* and *C* with STI-sidewall doping are intermediate between that of conventional DeNMOS (shallow-drain) device and deep-drain DeNMOS device (Fig. 2(a)). Therefore, the parameters of the parasitic bipolar structure of devices with sidewall doping are also likewise intermediate between the other two devices.

A. Physics of Breakdown Characteristics

The detailed physical mechanisms of drain breakdown characteristics are discussed now. Fig. 3 compares electric field distributions in OFF-state pre-breakdown (Fig. 3(a)) and post-breakdown (Fig. 3(b)) conditions. At V_{DS} = 10 V, the maximum field drop occurs across the *n*-well/*p*-well junction in the gate-to-drain overlap region. The depletion region at this junction is not in the vicinity of high doping region of the drain diffusion; hence, the drain breakdown voltage of the different STI-DeNMOS devices is similar and is determined by *n*-well/*p*-well junction breakdown voltage. The fields also drop at n^+ drain/*n*- interface, and the field distributions depend on the doping profile of the n^+ drain structure.

Beyond junction breakdown, as the drain current is increased, the drain voltage remains constant. The field distribution is similar in Fig. 3(a) at V_{DS} = 10 V and Fig. 3(b) at I_D = 0.1 µA/µm (below the triggering point at I_D = 0.2 mA/µm) for different devices; however, the avalanche generation keeps increasing in the junction depletion region due to increase in the injected drain current. At both V_{DS} = 10 V (Fig. 3(a)) and I_D = 0.1 µA/µm (Fig. 3(b)), high fields appear across n^+ source/*p*-well junction, which is effectively reverse biased.

As the drain current is increased to 1 mA/µm (Fig. 3(c)), the field distributions change significantly compared to that at I_D = 0.1 µA/µm. In each device, the fields are lowered across the n^+ source/*p*-well junction, which is now forward biased. Fig. 4 shows the current density contours in OFF-state at a high drain current level of 1 mA/µm. The n^+ source injects high currents into the *p*-well region for all STI-DeNMOS devices (Fig. 4). The major differences in field and current density profiles appear on the drain side. This is due to the increase in injected electrons at the drain contact, which causes the depletion region to expand in the *n*-well region (collector) and shrink in the *p*-well region (base) to maintain space-charge neutrality. This high level injection effect is referred to as base-push (Kirk) effect. In the conventional device, a distinct second peak field appears near n^+ drain diffusion region at high drain current level, apart from the peak field at *n*-well/*p*-well junction (Fig. 3(c)). However, in deep drain device, the right-side of STI structure is a low field region and the field distribution spreads more uniformly from *n*-well/*p*-well junction towards *n*-well/n^+-drain interface region. So, there is only one peak field region in the deep-drain device compared to two distinct peak field regions in the conventional device. The deep drain device can sustain a high current density region between the *n*-well/*p*-well junction and the *n*-well/n^+-drain interface region. This is unlike the conventional device at same drain current level. This explains higher negative differential resistance and the delayed onset of positive differential resistance branch in the deep-drain device, as compared to the

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shallow-drain device. The current flow spreading at high drain current can be further modulated by adjusting the deep-drain doping profile. These current distributions explain the high collector (n^+-drain) to emitter (n^+-source) current ratio of the parasitic bipolar of the deep drain device compared to the conventional shallow drain device.

In the devices with STI-sidewall doping, fields drop along the sidewall regions (Fig. 3(c)); however, the peak fields are still in the gate-to-drain overlap region. The current flow path at I_D = 1 mA/µm is highly localized close to the sidewall regions (Fig. 4). The current density localization in these devices is much stronger compared to deep-drain and shallow-drain devices, which can lead to early current filamentation. Fig. 5 shows a comparison of impact ionization (II) distribution in OFF-state at a high drain current level of 1 mA/µm in the four device structures. Since the peak fields are confined in the gate-drain overlap region in devices *A*, *B* and *C*, the peak impact ionization hot spot does not spread beyond the overlap region in these devices. This is unlike the conventional device, in which a distinct base-push effect causes a second II hot spot to emerge at the n^+ drain diffusion region, compared to the II hot spot at the *n*-well/*p*-well junction. In order for the device to sustain high failure currents, uniform spreading of fields, current densities and impact ionization in the bulk of the drift (*n*-well) region is highly desirable.

B. Impact of Drain Structure on HCI Effects

The OFF-state hot carrier reliability is an important parameter for DeMOS and LDMOS devices [5]. In STI-DeMOS devices, the OFF-state drain leakage current is dominated by impact ionization of electrons and holes in the *n*-well/*p*-well junction depletion region. This II process generates hot carriers, which can get injected in gate-to-drain overlap region and STI-sidewall (left-side) regions. Since the peak surface doping concentration in gate-to-drain overlap region in STI-DeMOS devices is below ~1e18 cm^{-3} and due to the vertical field distribution in presence of the STI structure, band-to-band tunneling generation is negligible compared to avalanche generation in the overlap region (not shown here). The DeMOS devices with different drain structures have similar field, II and current distributions under normal circuit operation at power supply voltages of 5 V and less than 5 V. Hence, the hot carrier injection (HCI) effects must be similar. The details of HCI physical mechanisms in STI-DeMOS devices with different drain structures require further investigations.

IV. Conclusion

The *I-V* characteristics of STI-type DeNMOS devices, in an advanced CMOS technology, with different drain structure types are studied using TCAD simulations. The deep-drain device shows better trade-off between ON-state resistance and OFF-state drain breakdown voltage, but with slight degradation in saturation drain current. However, the device with STI-sidewall doping gives a better trade-off between OFF-state drain breakdown voltage, ON-state resistance and drain saturation region parameters. Hence, the drain doping profile can affect the performance characteristics of DeMOS based I/O circuits. The impact of drain structure on the physical mechanisms of OFF-state drain breakdown characteristics is studied in detail. The snapback mechanisms are found to be highly sensitive to the doping profiles in drift regions. The deep drain STI-DeMOS device has high current gain parasitic bipolar, which allows higher peak current density. Further, the modulation of current spreading in a larger volume of silicon bulk compared to the conventional device requires optimization of deep drain doping profile. Hence, the onset of positive differential resistance branch in the snapback characteristics is delayed in the deep-drain device. However, STI sidewall doping generates localized high current density paths and hence, localized hot spots. Therefore, the detailed optimization of doping profile of the drain structure is required to improve both mixed-signal performance and high drain current behavior of STI-DeMOS devices.

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