On the Breakdown Physics of Trench-Gate Drain Extended NMOS

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***Abstract*—In this work, two drain extended NMOS (DeNMOS) devices, one with only planar gate and another with both planar gate and gate in a trench under the gate-drain overlap region (called trench-gate DeNMOS) are investigated. The latter device shows improved ON-state performance due to greater space-charge control with addition of trench gate. The OFF-state breakdown physics is also compared with conventional DeNMOS device. Due to greater field spreading in the trench-gate device under OFF-state conditions, a distinct base-push effect is not observed, unlike conventional device. The oxide reliability in trench-gate device improves with an additional offset in the drift region. Therefore, the trench-gate DeNMOS can be used as an alternative to improve input/output (I/O) device performance and reliability in advanced system-on-chip (SoC) applications.**

Index Terms*—*Base-push effect, breakdown physics, drain extended NMOS (DeNMOS), input-output (I/O), mixed-signal performance, offset structure, ON-state resistance, radio frequency (RF) performance, space charge modulation, trench gate (TG).

I. Introduction

High voltage devices like laterally diffused MOSFETs (LDMOS) and drain extended MOSFETs (DeMOS) are integrated in standard CMOS technology to support high voltage input-output applications [1]. Several designs of LDMOS devices have been proposed to improve the key device parameters: ON-state resistance and OFF-state breakdown voltage. Compared to conventional LDMOS, RESURF and super-junction LDMOS have low ON-resistance with similar forward blocking voltages [2]. However, trench-gate LDMOS devices are useful to further reduce ON-resistance by allowing ON-state current spreading in the bulk of the drift region, instead of confining the current path to the surface of the drift region [2, 3]. Various publications have investigated the integration of trench-gate LDMOS devices into planar CMOS technology, and also their electrical characteristics [3]. The trench-gated devices have shown an improvement in ON-state resistance and mixed-signal and radio frequency (RF) performance, while maintaining high OFF-state breakdown voltage. In [4], the concept of trench-gate DeMOS structure in advanced CMOS technology was introduced for the first time. The trench-gate DeMOS devices are useful for input-output (I/O) applications operating at 5 V and below 5 V. In this work, ON-state and OFF-state *I-V* characteristics of novel trench-gate DeMOS device structures are investigated using 2-D TCAD simulations.

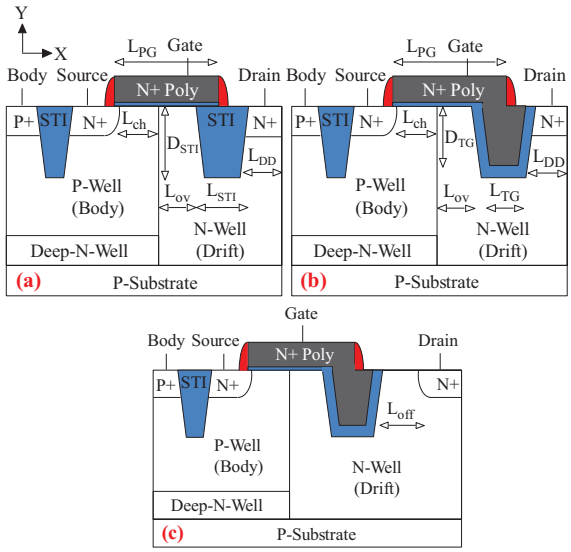

Fig. 1. Schematics of device structures under study: (a) conventional STI-DeNMOS (device *A*), and trench-gate DeNMOS without (b) (device *B*) and with (c) (device *C*) added offset (L_{off}) region. The length of STI (L_{STI}) structure in device *A* is kept same as sum of length of trench gate (L_{TG}) and trench-gate oxide thickness on either side of trench gate in devices *B* and *C*. In this work, a uniform oxide thickness of 20 nm is used on each of the three sides of the trench-gate.

II. Device Structures and *I-V* Characteristics

A. Description of Device Structures

The schematic views of DeMOS device structures under study are shown in Fig. 1. Fig. 1(a) shows the conventional STI-DeNMOS (device *A*) device, which is implemented using a standard 65 nm CMOS process technology. It uses *n*-well and *p*-well in the standard CMOS process as drift and body regions, respectively. The oxide thickness of planar gate is about 2 nm. For the purpose of simulation study in this paper, the DeMOS devices (Fig. 1(a-c)) are generated using a standard 65 nm process deck. Fig. 1(b) shows the modified DeNMOS, called trench-gate DeNMOS (device *B*). It has an additional trench gate in contact with the planar gate. Both trench gate and planar gate are formed with n^+ polysilicon material. In this paper, the depth of the trench structure etched in silicon for

trench gate formation is same as that of the STI structures. A uniform oxide thickness of 20 nm is used to isolate n^+ polysilicon material, forming the trench gate, from bulk silicon. Device *C* (shown in Fig. 1(c)) is identical to device *B*, except for an additional offset (L_{off}) of 200 nm between trench gate edge and drain diffusion region edge. The channel length, overlap length, and drain diffusion length are kept same in all the devices. The length (L_{TG}) and depth (D_{TG}) of the trench gate in devices *B* and *C* are kept as 330 nm.

All 2-D device simulations in this work are performed using Sentaurus Device TCAD simulator [5]. The hydrodynamic carrier transport model has been used in this work. The van Overstraeten impact ionization model, SRH generation-recombination and Auger recombination models have been used. Also, doping dependent mobility, high field mobility saturation and interface field induced mobility degradation models are switched on for the simulations.

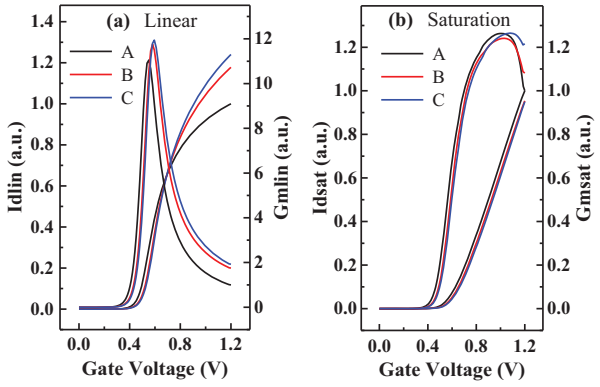

Fig. 2. Simulated (a) linear (at V_{DS} = 0.1 V) and (b) saturation (at V_{DS} = 3.3 V) I_D-V_G characteristics (on left-Y axes) of the devices. Right side Y-axes show (a) linear and (b) saturation transconductance characteristics. In (a), trench-gate DeNMOS devices show high linear drain current and transconductance. In (b), trench-gate DeNMOS devices show higher linearity in saturation transconductance w.r.t. gate voltage as compared to the conventional device.

B. I_D-V_G Characteristics

Fig. 2 compares linear and saturation region I_D-V_G characteristics of the DeNMOS devices under study. The conductive portion of the trench structure, when positively charged, attracts negative charges in bulk silicon region, which is the n-well (drift) region, for devices *B* and *C*. Trench-gate device (device *B*) shows higher linear drain current and transconductance and lower ON-resistance (R_{ON}) compared to the conventional device, mainly due to reduced drift region resistance in the conduction current path. The trench-gate device with 200 nm offset region (device *C*) shows slightly greater R_{ON} reduction compared to device *B*. This is because the added offset region allows current flow spreading over a wider region of *n*-well before the current sinks to the drain contact.

However, there is slight reduction in saturation drain current in both trench gate devices compared to conventional device. This is due to appearance of a depletion (non-conducting) region on trench gate sidewalls, which reduces the width of the conducting current flow. Also, the dependence of saturation region transconductance on the gate voltage is more linear in the trench-gate devices, compared to the conventional device. This is due to enhanced space-charge control in the drift region by the trench-gate. The linearity of saturation I_D-V_G characteristics is beneficial for RF power amplifier and other analog circuit applications. The detailed analysis and design of the performance characteristics of trench-gate devices for mixed-signal and RF applications requires further study.

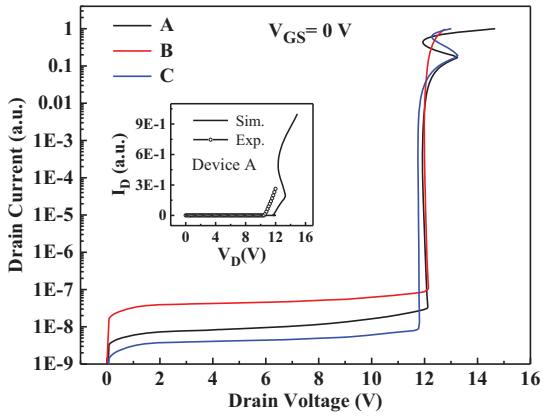

Fig. 3. Simulated OFF-state drain breakdown characteristics (I_D-V_D at V_{GS} = 0 V) of the DeNMOS devices under study. Inset shows comparison of measured and simulated drain breakdown characteristics of the conventional STI-DeNMOS device (device *A*).

C. I_D-V_D Characteristics

The simulated OFF-state drain breakdown characteristics of the DeNMOS devices under study are shown in Fig. 3. The measured breakdown characteristic of the conventional device exhibits a breakdown voltage of 10.5 V. Each simulated device shows OFF-state drain breakdown voltage of about 12 V. The breakdown voltage of the trench-gate device *B* is similar to conventional device *A*, whereas the breakdown voltage of device *C* is slightly reduced. The pre-breakdown drain leakage current is also slightly reduced in the trench-gate devices. The details of breakdown mechanisms are investigated in next section.

III. Detailed Physics of Breakdown Characteristics

The physics of OFF-state drain breakdown in conventional and trench-gate DeNMOS devices is discussed here. Understanding drain breakdown physics of trench-gate DeMOS devices is useful to study its safe operating area and aid in the design of trench-gate DeMOS structures for further improvement. The following discussion refers to Figs. 4, 5, and 6. The electric field distribution in pre-breakdown region at V_{GS} = 0 V and V_{DS} = 10 V is compared for the three devices *A*, *B* and *C* in Fig. 4. The field contour plots are marked with field directions in different regions of interest. The OFF-state conduction current density and impact ionization profiles for devices *A* and *C* are compared in Figs. 5 and 6 respectively.

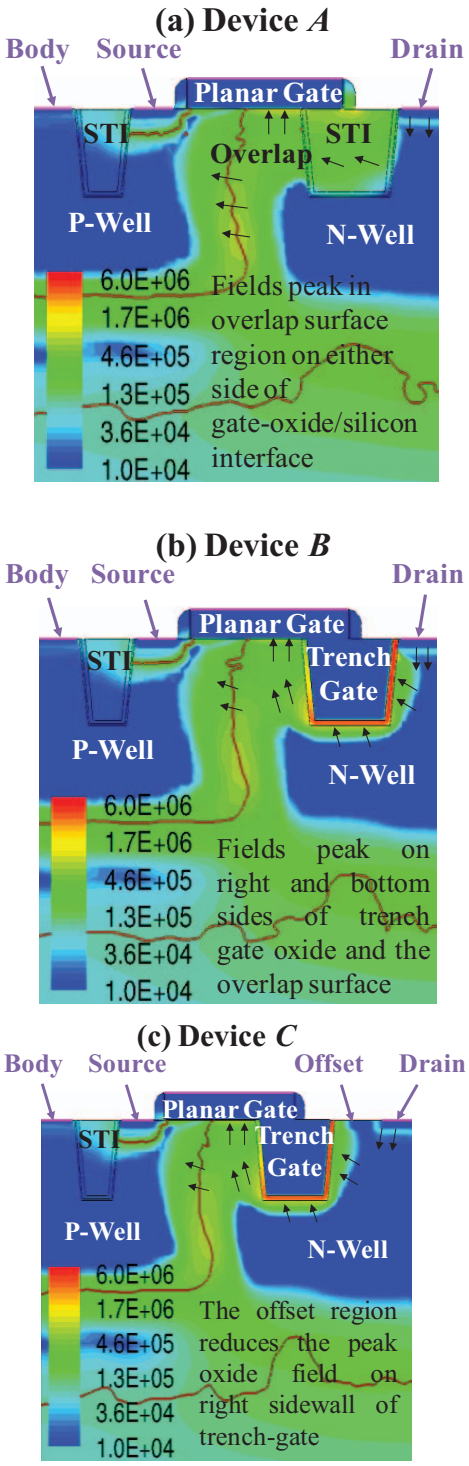

Fig. 4. Electric field (V/cm) contour in devices (a) *A*, (b) *B*, and (c) *C* at V_{GS} = 0 V and V_{DS} = 10 V (pre-breakdown region). Trench-gate devices show relaxed field distribution under gate-drain overlap region. Device *C* with offset region shows lesser peak field at V_{DS} = 10 V in trench-gate oxide region compared to device *B*.

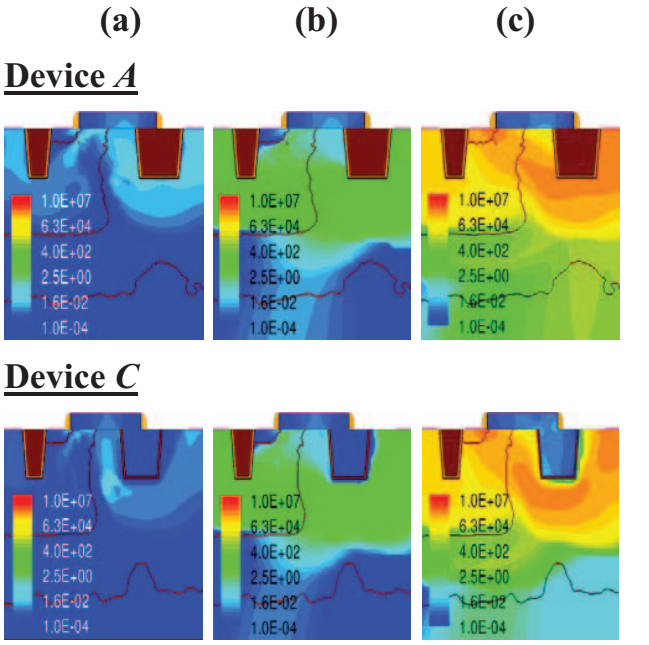

Fig. 5. Conduction current density (A/cm^2) contour in devices *A* and *C* at V_{GS} = 0 V and (a) V_{DS} = 10 V, (b) I_D = 0.1 μA/μm and (c) I_D = 1 mA/μm. Breakdown current flow is diverted away from sidewalls of trench gate device with depletion region.

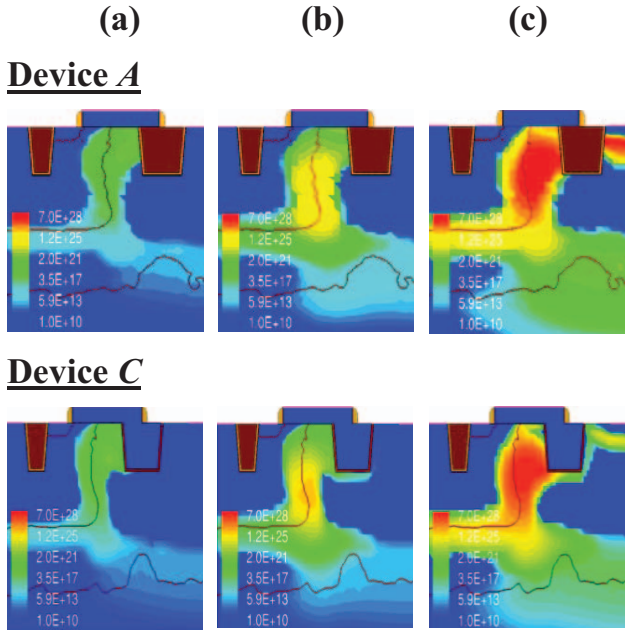

Fig. 6. Impact ionization (1/cm^{3}s) contour in devices *A* and *C* at V_{GS} = 0 V and (a) V_{DS} = 10 V, (b) I_D = 0.1 μA/μm and (c) I_D = 1 mA/μm. In device *A*, peak impact ionization hot spot shifts from *n*-well/*p*-well junction towards *n*+ drain. In device *C*, impact ionization region emerges in *n*-well/*p*-well junction and spreads in sidewall depletion regions of the trench-gate.

In the conventional STI-DeNMOS device (device *A*), in the pre-breakdown region (the OFF-state drain breakdown voltage is ~12 V), peak field distribution occurs across the *n*-well/*p*-well junction region, mainly under the gate-to-drain overlap region (Fig. 4(a)). The STI block helps to effectively reduce the peak gate oxide fields. The OFF-state leakage current flows from drain through the surface of the overlap region to source (Fig. 5(a)), according to the field profile in Fig. 4(a). For the doping profiles of the devices under study, band-to-band tunneling cannot contribute to pre-breakdown leakage. The avalanche generation at the reverse-biased *n*-well/*p*-well junction contributes to the leakage current. Since the depletion region is confined to the gate-to-drain overlap region, the impact ionization (II) distribution is also confined there (Fig. 6(a)). As *n*-well/*p*-well junction breakdown occurs, the current flow through the junction increases and the *p*-well (body) current due to holes from II (Fig. 5(b) at I_D = 0.1 μA/μm). Also, the peak II hot spot increases in the *n*-well/*p*-well junction (Fig. 6(b)). At high drain current level of I_D = 1 mA/μm, the voltage drop in *p*-well (body) forward biases the n^+ source/*p*-well (body) junction to trigger the parasitic bipolar (Fig. 5(c)). As the space charge region spreads more in the *n*-well side, another field peak and hence, II peak appears at the n^+ drain/*n*-well interface, called base-push effect (Fig. 6(c)).

The field distribution plot of trench-gate DeNMOS device (Fig. 4(b)), in pre-breakdown region, shows a relatively large spread of high field region around the *n*-well/*p*-well junction and around the trench gate sidewalls. This is because of applied high positive drain voltage, grounded trench-gate and the grounded planar gate. Hence, the maximum field drop occurs across the right and bottom sides of the trench gate oxide. This peak field is higher than that at the overlap surface region. Hence, oxide reliability of trench-gate DeMOS devices under drain breakdown is more severe concern than in conventional DeMOS devices. To alleviate this effect, a novel modification is proposed in this work, as compared to the structures disclosed in [4], without affecting low voltage device characteristics (Fig. 2). Device *C* with the offset region shows reduced peak field in the trench-gate oxide (Fig. 4(c)). This is because the n^+ drain contact is moved away from trench gate oxide.

For trench-gate DeMOS devices, the pre-breakdown drain leakage is slightly reduced. This can be explained by the reduction in the width of current flow path under OFF-state, due to the depletion region induced by the grounded trench-gate on the sidewalls of the trench-gate (Fig. 5(a)). In addition, the slight reduction in drain breakdown voltage in device *C* as compared to device *B* (Fig. 3) is because the field distribution is slightly more relaxed in the extended depletion region around the trench-gate sidewalls. In Fig. 6(a), slightly more relaxed II plot is observed for device *C*. In post-breakdown region, the depletion region formation and hence, space-charge control of *n*-well by the trench-gate plays an important role in breakdown characteristics. The breakdown current flow due to *n*-well/*p*-well junction breakdown is diverted away trench-gate sidewalls (Fig. 5(b, c)). Also, the II distribution gradually expands around the trench-gate sidewalls from *n*-well/*p*-well junction towards the n^+ drain contact (Fig. 6(b, c)). Hence, the double peak of the II region as observed in the conventional device is not observed in the trench-gate device.

IV. Conclusion

This paper investigated the distinct *I-V* characteristics of trench-gate drain extended NMOS device, for the first time, using TCAD simulations. A comparison has been made with conventional STI-type DeNMOS device. Due to the space-charge control of *n*-well (drift) region by the trench gate, the trench-gate DeMOS devices showed improved linear and saturation region characteristics, compared to conventional device. The trench-gate devices could deliver better ON-state performance, while maintaining similar breakdown voltage. The details of OFF-state drain breakdown mechanisms were investigated and compared. The oxide reliability in trench-gate DeNMOS is highly sensitive to its geometrical parameters. A novel offset structure modification is proposed to enhance its oxide reliability. The high field spreading and space charge modulation due to the trench gate structure dominates the breakdown mechanisms in trench-gate DeMOS devices.

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