A Fully-Integrated Radio-Frequency Power Amplifier in 28nm CMOS Technology mounted in BGA Package

Ankur Gupta, *Student Member, IEEE,* Mayank Shrivastava, *Member, IEEE,* Maryam Shojaei Baghini, *Senior Member, IEEE*, Harald Gossner, *Senior Member, IEEE*, and V. Ramgopal Rao, *Senior Member, IEEE*

***Abstract*—In this paper, we present a fully integrated radio-frequency (RF) power amplifier (PA) using high voltage STI type DeNMOS device in standard 28nm CMOS technology. The device is fully compatible with scaled CMOS process technologies with minor cost penalties. The device prototype was fabricated in 28nm CMOS process and packaged in commercially available ball-grid-array (BGA) package to mimic real application conditions. Complete power amplifier circuit, made on low-loss laminate using this BGA package, is also presented. Packaged RF PA achieves 19dBm of output power at frequency of 1GHz with high linearity.**

***Index Terms*— Drain Extended MOS (DeMOS), Shallow-Trench-Isolation (STI), System-on-Chip (SoC), RF, Power Amplifier (PA) and linearity.**

I. Introduction

Semiconductor market has seen tremendous growth in the wireless devices operating at radio-frequencies (RF) [1]–[3]. Over the past few decades, significant improvements have been made in these wireless devices (i.e. mobile phones, Bluetooth and WiFi devices) for more computing power, higher communication speed and longer battery life.

Fig. 1 shows a general block diagram of RF system used for transmitting and receiving wireless data in these devices. This system can be partitioned into three sections: First is the digital backend and baseband unit which also consist of digital signal processor and memory, and make the computation unit of the device. Second is Analog/RF transceiver unit consisting of RF and baseband mixers which provides data conversion and frequency translation. Third unit is RF Power amplifier which boosts up the high frequency RF signal to transmit it for long distance communications.

From system design and fabrication point of view, digital and baseband blocks are implemented using standard cost effective CMOS devices which have very high level of integration capability [4], [5]. RF mixer and low noise amplifier (LNA) are generally been implemented using CMOS

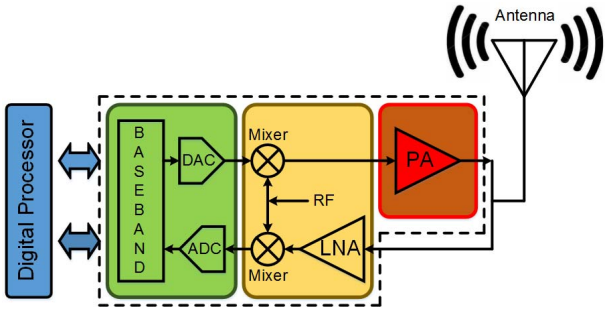

Fig. 1. Simplified block diagram of a transceiver network used in modern wireless communication systems.

devices itself but with the high performance variant of the devices to meet stringent requirements of speed and performance [6]–[8]. This comes at the extra cost of few lithographic mask during the fabrication and hence generally been fabricated on a separate chip. On the other extreme of this spectrum, lies the RF power amplification block which is generally implemented using III-V compound semiconductor devices. These devices offer higher breakdown voltage compared to standard CMOS devices without sacrificing the carrier mobility and hence enhance the performance. Since, the integration of these compound semiconductors with standard CMOS is not trivial these blocks are always implemented as a separate chip on the printed circuit board (PCB).

Low fabrication cost is the main driving factor to obtain a system-on-chip (SoC) solution where all digital, baseband and RF blocks can be fabricated on single wafer using CMOS devices. As the CMOS technology improves, the device performance strengthens. This device improvement has made it possible to use the standard devices at radio frequencies in multiple applications [9], [10]. However, due to the scaling, breakdown voltage of the devices has also come down [11], [12], which adversely impacts the power handling capability of the device. Many research groups are actively involved to fabricate a CMOS compatible high voltage device which can meet power and performance goals at the system level [13], [14]. In this paper, we fabricate a complete RF PA using CMOS compatible DeMOS device and show the RF

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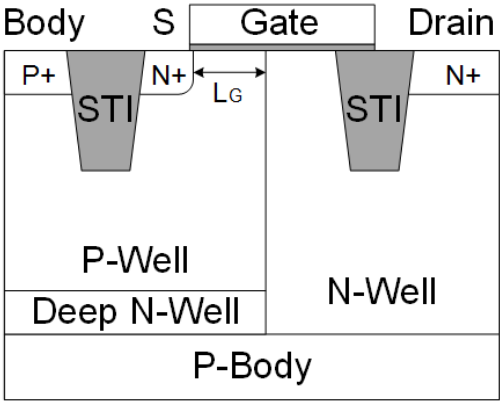

Fig. 2. Schematic cross-section of STI type DeNMOS device fabricated in 28nm CMOS process. Figure depicts a single sided structure. However, the device is fabricated in double finger structure with sharing of N-well.

performance. We take effects of packaging also into account to mimic practical conditions for SoC applications.

II. RF PA Circuit Realization

Recently, STI type DeMOS device is shown as a potential candidate for RF PA applications in scaled technologies [15]. In this paper, we started with a foundry standard STI DeNMOS device and fabricated it in 28nm CMOS technology with a total gate width of 1.6mm. The schematic of the device is shown in Fig. 2. This device has thin gate oxide which can sustain only low applied gate voltages. However, the drain contact is not adjacent to gate edge and separated by shallow trench isolation block. Because of this isolation block, high voltages can be applied at the drain terminal of the device. N-

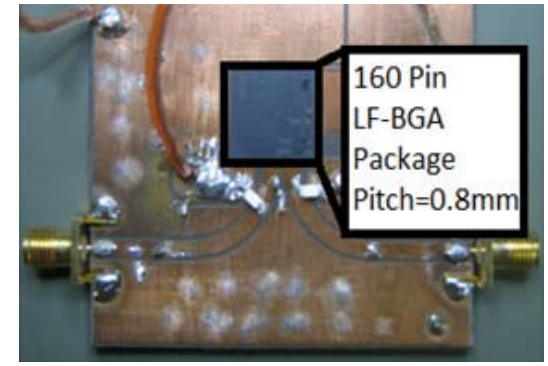

Fig. 4. Photograph of the complete fabricated RF PA on low loss laminate.

Well region of the device provide reduced surface field (RESURF) action which enhance the breakdown voltage (V_{BD}) to ~10V even in scaled technologies. The charge carriers drift in this U-shaped N-well to reach to drain contact. This device provides high voltage (hence, high power) capability at the expense of extra series resistance of N-well drift region.

The fabricated device was packaged in commercial 160-pin ball grid array (BGA) package. High pad count BGA package was chosen to keep enough number of I/O pads for additional digital circuitry when used in integrated form. Most of the earlier work was demonstrated on probe-station based on-die measurements where package losses were not taken into account. In this paper, for the first time, packaged device was chosen to accommodate RF losses occurring inside a realistic BGA package for integrated SoC solutions. BGA package was chosen due to its widespread use and good prospects for future packaging technology. The package has dimension of

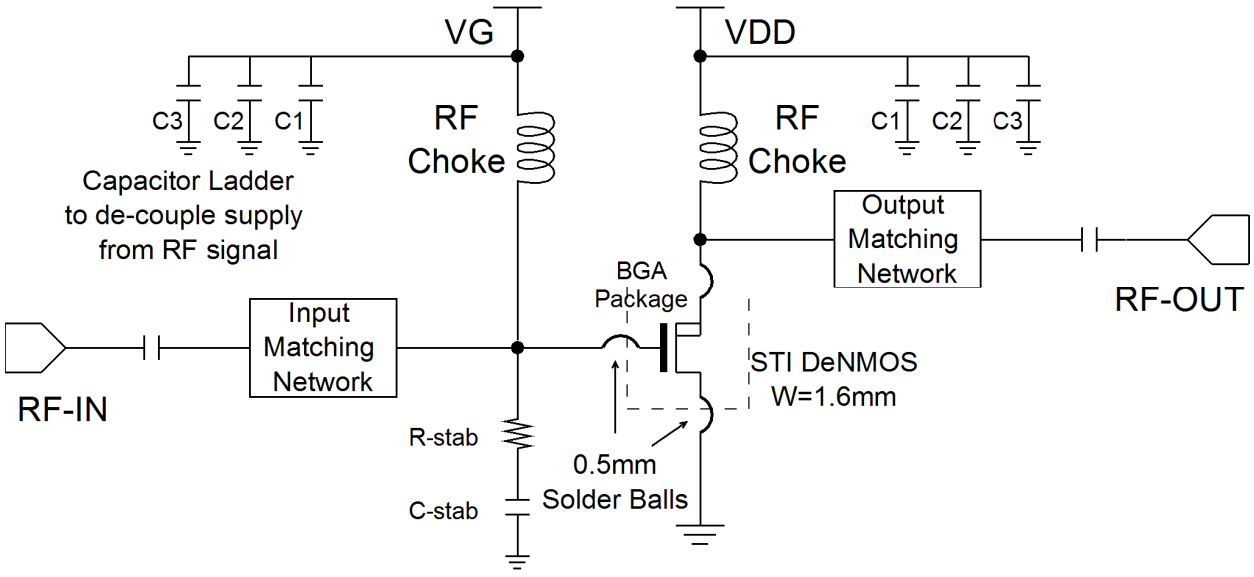

Fig. 3. Circuit schematic of the RF PA with off-chip matching and biasing network.

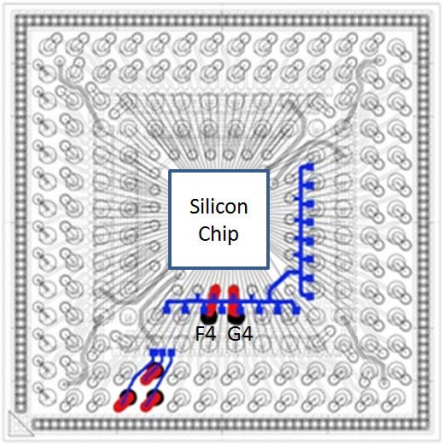

Fig. 5. Internal view of the BGA package used for measurement of RF losses in the traces inside package.

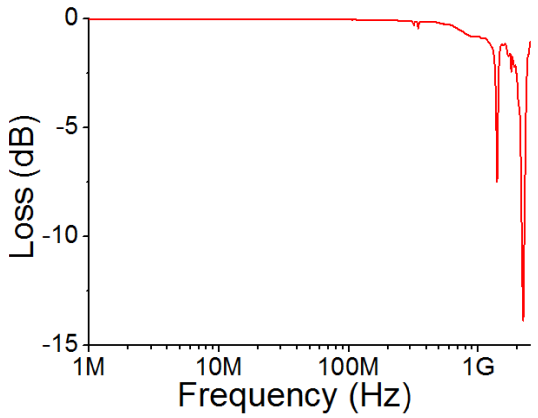

Fig. 6. Measured RF loss in the BGA package as a function of frequency at small applied output power.

13mm×13mm with a ball pitch of 0.8mm and ball diameter of 0.5mm. Bond-wire connections were chosen instead of flip-chip configuration due to its significant cost advantages.

Complete RF PA circuit schematic is shown in Fig. 3 with off-chip matching and biasing networks. The circuit uses stability network designed to provide stability to the circuit for a wide frequency range. RF choke coils are used to provide DC biasing to the device. To fabricate this complete RF PA circuit, a low loss laminate was chosen to prepare printed circuit board (PCB). Low loss laminate was used to minimize the losses occurring in the PCB traces at high frequencies. Laminate had a loss tangent (tan ∂) of 0.0004 which corresponds to very low loss in the PCB micro-strip at high frequencies. The copper cladding used was 70µm which is generally used for high frequency applications. DC voltage was applied to the circuit through multi-strand wire to reduce the wiring resistance of the power supplies. SMA connectors were used at the input and output of the circuit for RF signals. Input and output impedance of the circuit was matched to standard 50Ω RF terminations. Input and output micro-strip traces were designed to operate in different direction to

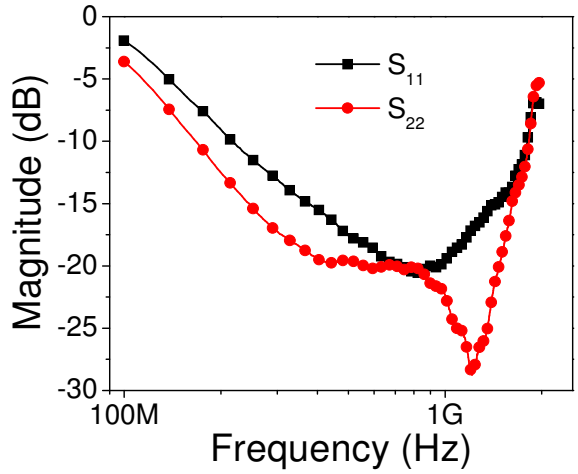

Fig. 7. Measured input and output matching of the RF PA circuit on board. Low magnitudes of S_{11} and S_{22} shows very good matching with standard 50Ω RF terminations.

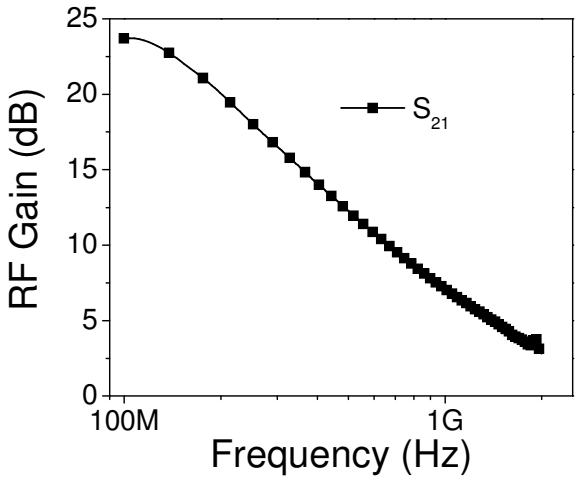

Fig. 8. Measured small-signal RF gain of the RF PA. Measurements show a 24dB gain at lower frequencies which reduces to 7.2dB at 1GHz.

minimize the coupling in RF signals.

Fig. 4 shows the photograph of fabricated RF PA on low loss PCB with BGA package. Back side of the PCB is complete copper which acts as a ground plate for RF signals.

III. BGA Package RF Loss Measurements

BGA package can provide more number of pins compared to dual-in-line (DIP) package while keeping the package area same. This high density of pins makes it an attractive choice in modern packaging industry. Unlike DIP packages, BGA does not have the problem of accidently bridging two adjacent pins with solder which improve the reliability and usage of the package manifold. Good Thermal transport is also an important feature of BGA. BGA package provides low thermal resistance between the package and PCB which dissipates the heat more evenly compared to DIP packages. Another very important feature of BGA packages is the short

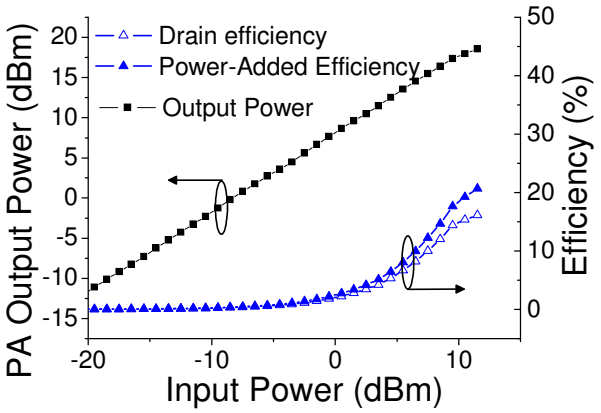

Fig. 9. Large-signal power measurements performed on fabricated RF PA.

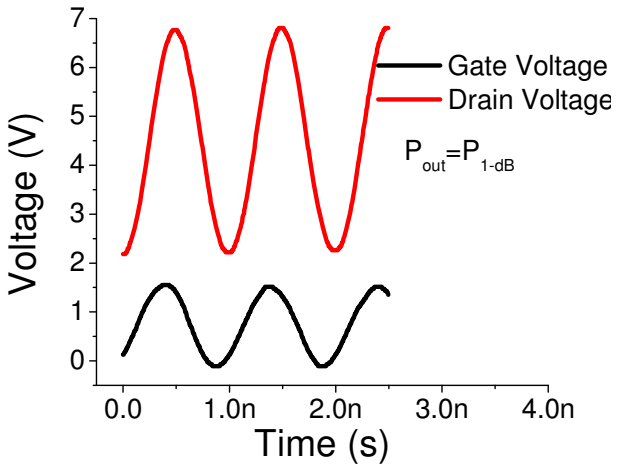

Fig. 10. Measured gate and drain voltage waveforms using oscilloscope at 1GHz frequency of operation when circuit was operated at its peak output power.

length of contact leads compared to DIP packages. Due to short contact leads, the parasitic inductance and capacitance of the BGA package is low which makes them further attractive for high frequency applications.

We performed RF measurements to check the suitability of these BGA packages for SoC applications with wireless communication capability. We measured the RF loss between two adjacent solder balls (F4 and G4) which were connected internally through package tracks (shown blue) as shown in Fig. 5. This BGA Package was mounted on the low-loss laminate to measure the return path loss of this package. The measurements were conducted at small-signal level of -20dBm power at Agilent's E5071C vector network analyzer (VNA). Measurement results are shown in Fig. 6. Measurements show that there is negligible RF signal loss at low frequencies (~300MHz). However, as the frequency increases, the loss due to package increases. In the proximity of 1GHz, package pins can causes as much as 5dB to 7dB loss. This loss further increases as the frequency of operation increases. At 2GHz frequency, the loss can be as high as 12dB which can limit the use of BGA packages for high frequency/RF applications.

IV. RF PA Measurement Results

Small-signal RF measurements were performed on the fabricated board using Agilent's E5071C vector network analyzer (VNA). Small signal power of -20dBm was applied and the frequency was swept from 0.1GHz to 2GHz in linear steps through VNA. PA was designed to operate at the fundamental frequency of 1GHz. This frequency is chosen due to its proximity to the GSM band used for wireless communication for handheld devices. Fig. 7 shows the measurement results. Input and output matching of the circuit is given by S_{11} and S_{22} respectively. S_{11} and S_{22} are forward and reverse reflection coefficients when the ports are connected to standard 50 Ω termination. There represent the ratio of reflected power to the incident power. Magnitude of the reflected power should be as low as possible in case of matched condition. Practically, magnitude of S_{11} and S_{22} should be below -10dB in order to achieve matching conditions with standard 50Ω RF port terminations. The designed RF PA achieves -20dB of S_{11} and S_{22} which represent a very good matching.

Fig. 8 shows the small-signal RF gain (S_{21}) of the circuit in matched conditions. As shown, the RF PA has a high gain of 25dB in the vicinity of 100MHz. However, the gain drops at high frequencies due to the limited cut-off frequency of the device and various packaging effects which were discussed in previous section. The measured small-signal RF gain of RF PA circuit is 7.2dB at a fundamental frequency of 1GHz.

Large-signal measurements were performed on the fabricated board at a fundamental frequency of 1GHz. Signal generator was used for applying the input power to RF PA at 1GHz. The circuit was biased at maximum drain voltage (VDS_{MAX}) and a gate bias voltage of VGS1. Gate bias voltage is chosen to operate the PA in class-AB mode of operation. Class-AB mode is known to have better trade-off between linearity and efficiency. Input was swept from a low power of -20dBm to a high power value of 12dBm. Fig 9 shows the measurement results. As shown, the output power generated by the circuit increases linearly with a gain of 7.2dB which is the small-signal gain of the circuit measured earlier through VNA. Efficiency of the circuit also increases due to increase in the RF power. However, at large-signal levels, the RF gain of the circuit degrades and the device enters into saturation region. The point at which the RF gain of the circuit degrades by 1 dB is called the 1-dB compression point and denoted by $P_{1\text{-}dB}$. This point is considered as the peak output power generated by an RF PA. Fig. 9 shows a measured peak output power of 19dBm delivered to 50Ω termination by the PA at 1GHz frequency. Beyond 1-dB compression point, the output RF power saturates but the DC power consumption increases monotonically which degrades the efficiency of the system. This extra DC power goes into the harmonics and hence significantly degrades the system linearity.

Another very important aspect of PA operation is to maintain all large signal swings within the device breakdown

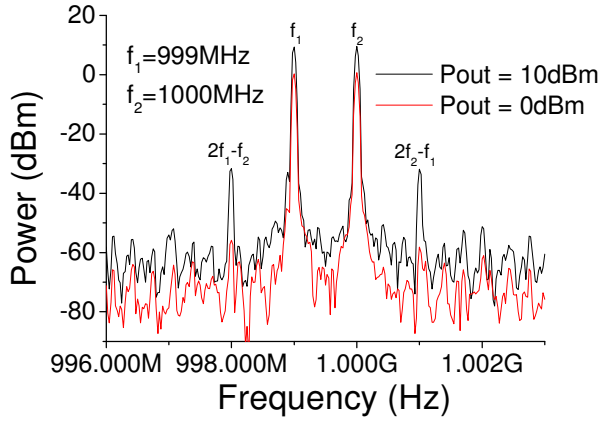

Fig. 11. Measured output power spectrum when the circuit was excited using two tones.

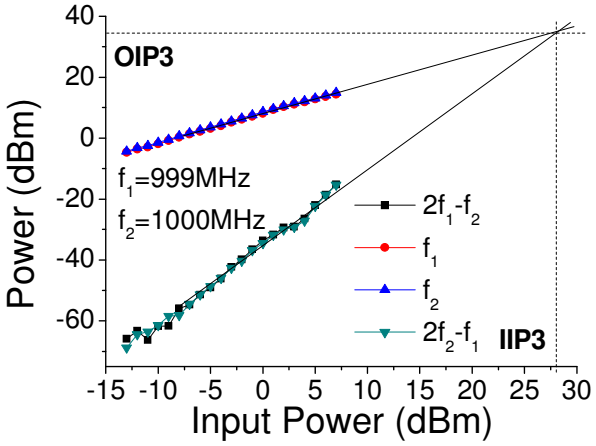

Fig. 12. Calculation of input and output 3rd order intercept point (IIP3 and OIP3 respectively).

limits. The device used in this work has a thin gate oxide which cannot sustain high voltage across gate terminal. Hence, the gate input voltage was kept below oxide breakdown to ensure reliable operation of the device. However, the drain terminal can sustain high voltage due to RESURF action. Hence, the drain was biased at comparatively higher voltages to provide higher power at the output. Fig. 10 shows the gate and drain voltage waveforms at peak output power measured using real time oscilloscope.

Linearity of an RF PA is very important for its usability in wireless communication. Linearity of circuit is generally measured using two-tone test where two fundamental frequencies are applied at the input and output is observed using spectrum analyzer. Fig. 11 shows the output of fabricated RF PA at output power of 0dBm and 10dBm. As shown, the 3rd harmonic power content ($2f_1$-f_2 and $2f_2$-f_1) of the spectrum increases with increase in output power. Output and input third order intercept points (OIP3 and IIP3) represent the linearity figure-of-merit for an RF PA which is calculated from two-tone test. As shown in Fig. 12, the output power of both the tone increases with input power. 3rd harmonic power also increases with 3 times the slope of fundamental power. These two graphs are extrapolated in order to calculate OIP3 and IIP3 as shown in the figure. Designed RF PA achieves a high value of 34dBm for OIP3 which represents a very good linearity of the circuit.

Small and large signal measurements show that PA shows a good linearity and RF gain. RF gain using BGA package is ~3.5dB less compared to the RF gain reported earlier by our group for a non-packaged device [15]. Detailed comparison and degradation due to packaging is shown in table I. This is because of the package parasitic effects and in close agreement with the measured RF loss due to packaging.

V. Conclusion

This paper presents an STI type DeMOS device based RF power amplifier fabricated in 28nm process and packaged in 160-pin BGA package. All packaging and wire-bonding effects were taken into account to mimic the realistic conditions. The PA achieved 7.2dB of RF gain with a high degree of linearity at 1 Ghz. As presented in table-I, the gain and efficiency of the circuit can be further improved significantly by optimizing the BGA package for RF applications.

TABLE I
Comparison of RF PA Performance with and without Package

Performance	Without Package	With Package	Degradation
RF Gain	10.8 dB	7.2 dB	50 %
Output Power	24 dBm	19 dBm	66 %
Drain Efficiency	46 %	21 %	54 %
PAE	40 %	16 %	60 %

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