Device-Circuit Co-design for High Performance Level Shifter by Limiting Quasi-saturation Effects in Advanced DeMOS Transistors

Peeyusha Saurabha Swain,
Maryam Shojaei Baghini,
and V. Ramgopal Rao
EE Department, IIT- Bombay,
Mumbai, India {peeyushs, mshojaei,
rrao}@ee.iitb.ac.in

Mayank Shrivastava
Advance Nanoelectronic Device
and Circuit Research Laboratory
Department of ESE
IISc-Bangalore, India
mayank@dese.iisc.ernet.in

Harald Gossner
Intel Corp. Mobile and
Communications Group
Munich 80336, Germany
harald.gossner@intel.com

***Abstract*—This paper presents a device-circuit co-design methodology for a DeMOS 5V GHz-speed high voltage level shifter. The limiting quasi-saturation effect is addressed by a co-design methodology. The co-design methodology is applied to the STI-DeMOS in a calibrated setup using experimental data. As a result, a 15% improvement in the speed is achieved for a high-performance level shifter circuit.**

I. Introduction

STI type of DeMOS (drain extended MOS) device has recently found many applications in system-on-chips (SoC). Level shifter (LS) is frequently needed in I/O interfacing of SoC's. The STI-DeMOS device is reliable and easily integrable in CMOS technology [1]. The reliability is due to STI [Fig. 1 (a)] which prevents the electric field crowding in the gate oxide edges near the drain terminal. However, the STI diverts the current path into the bulk, thereby impacting the performance.

A device-circuit co-design approach recently has shown that a high speed high voltage LS beyond 1GHz operating clock frequency is feasible [2]. However, a few aspects of the device engineering such as STI-depth and drain contact length (DL) [Fig. 1 (a)] are not explored in [2]. Both the design parameters are considered in this paper without adding to the process complexity and cost. The effect of the quasi-saturation (QS) on the current is shown in Fig. [1 (b)].

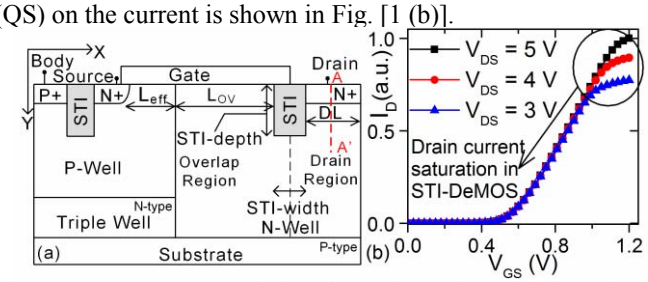

Fig. 1. (a) An STI-DeMOS device. The overlap region and drain region are collectively called as drift region. (b) I_D-V_{GS} characteristics of typical STI-DeMOS device indicating drain current saturation at higher V_{GS}.

II. Test Circuit and Simulation Methodology

The LS architecture reported in [2] is used as a test vehicle [Fig. 2]. Four high voltage transistors P5, P6, N5 and N6 [Fig. 2] are STI-DeMOS devices and core of the co-design process. Calibrated process and device simulation decks, for 65nm technology are used in this work [3] [Fig. 3]. The circuit simulations are performed using mixed-mode TCAD simulations [4].

A. STI-DeMOS ON Current Limitation and The QS Effect

Quasi-saturation is a current limiting phenomenon in HV devices even without any channel pinch-off. As absolute value of the gate bias increases, a large amount of drain potential is dropped in the drift region (below drain terminal). This pushes the intrinsic MOS device into the ohmic region of operation and hence the overall transconductance of the device, g_m, reduces. A large potential drop in the drift region occurs when the drain current exceeds certain critical current given by [5]

$$I_C = qAnV_{sat} \quad (1)$$

where q is the electron charge, A is the area of the current path, n is the carrier concentration in the drift region and V_{sat} is the carrier velocity saturation. When the drain current is higher than I_C, the carrier velocity gets saturated resulting in carrier accumulation, carrier depletion, high electric field and potential drop [4]. We have observed that, the electric field is high and velocity of carriers is saturated in the region where the carriers are depleted or accumulated. This is the region where a large amount of drain potential drops. Hence, in the optimization of the drift well, we attempt to increase the critical current.

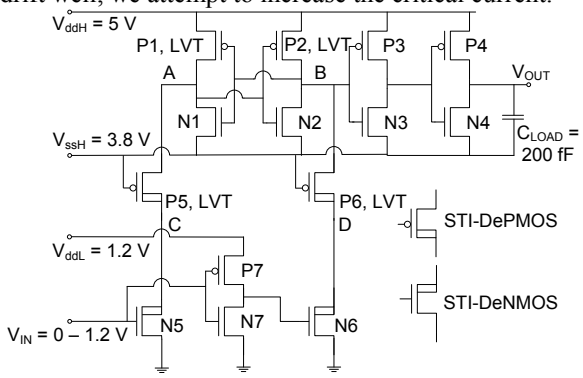

Fig. 2. Level shifter test circuit

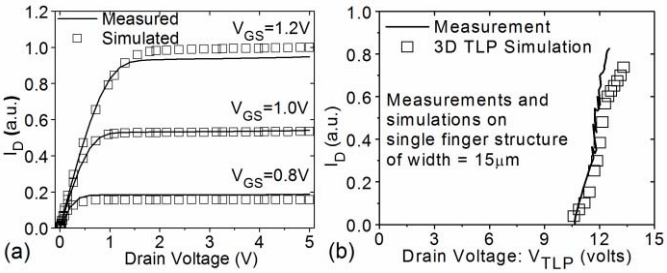

Fig. 3. Calibration of models used in TCAD simulations for STI type DeMOS devices (a) I-V characteristics (b) Breakdown behavior.

B. Co-design Parameters

For a circuit designer, the effective channel length (L_{eff}) and transistor width (W) are the most important parameters. However, here, in the device-circuit co-design domain, we explore other geometrical design parameters of STI DeMOS device to enhance the performance of the LS. These parameters are: STI-width, gate-to-N-well overlap length (L_{OV}), DL. We also explore STI-depth and doping of drain N-well [Fig. 1]. Design of all the parameters doesn't add any extra process cost.

Even for doping optimization, the needed additional mask is already available in the HV CMOS process.

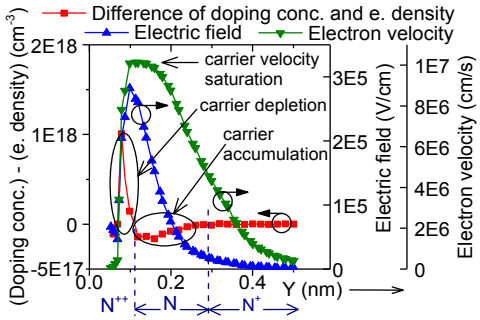

Fig. 4. Carrier depletion, accumulation, electric field and carrier velocity of a typical STI-DeMOS device biased at 5 V of drain bias and 1.2 V of gate bias. The plots are shown across the AA' cross section in Fig. 1 (a).

Increase in DL and L_{OV} enhances 'A' and increase in the doping increases the 'n', in (1). However, they affect the capacitances C_A, to C_D at nodes A to D, respectively (Fig. 2).

III. Device-Circuit Co-Design for LS Application

A. L_{OV}, DL and STI-depth Optimization

A matrix of DL and L_{OV} values is considered at different STI-depth values for optimization [Fig. 5]. For the STI-depth of 250 nm and greater, the DL value greater than 200 nm and the L_{OV} values in the range of 250 nm to 300 nm lead to the least LS delay range with negligible effect on the breakdown voltage. For STI-depth of 150 nm, a further low LS delay is observed at DL more than 300 nm and L_{OV} less than 300 nm. Keeping both area and performance in mind, we select L_{OV} = 200 nm and DL = 300 nm. The Lower STI-depths show better delay performances than the higher STI-depths at the cost of affecting the isolation of the STI-DeMOS devices and the core devices as well as breakdown voltage.

B. Doping Dose and Implant energy Optimization

The STI-DeMOS device has an N^{++}-N-N^{+} structure (due to its retrograde doping profile) in the drain region. When the drain current is higher than the I_C, the N^{++} region [Fig. 4] is depleted and N region is accumulated with carriers. In order to avoid this effect, both the implant dose and implant energy are optimized. A high implant dose is undesirable as it reduces the breakdown voltage. Lowering implant energy increases the doping of the lowly doped N region in the overlap and drain region. Thus, the critical current is enhanced. This reduces the LS delay as the ON current is improved [Fig. 6].

The co-designed LS performance parameters are tabulated in Table I. The LS with 1.5 GHz operation speed is obtained. 15% improvement as compared to the previously published work is achieved with reasonable breakdown voltages of 7 V and 8 V for STI-DeNMOS and DePMOS, respectively.

IV. Conclusion

A co-design methodology for optimizing an STI-DeMOS device while considering quasi-saturation for HV level shifting application is elucidated in this paper. By including STI-depth and DL as design parameters in the co-design process, a 15% improvement is achieved with no additional process cost or complexity as compared to the previously reported work.

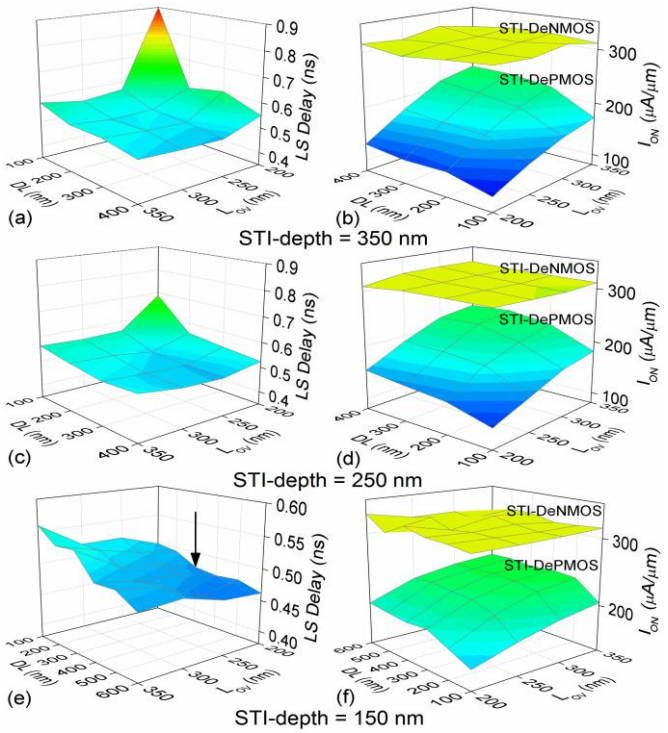

Fig. 5. LS delay and ON current for STI-depth (a), (b) = 350 nm (c), (d) = 250 nm (e), (f) = 150 nm. The arrow indicates the optimized device.

TABLE I. Device –Circuit Co-Designed LS Performance

Performance Parameters	LS co-designed in [2]	LS co-design in this work
Average delay (ns)	0.45	0.38
Duty cycle (%)	48	48
Average power (mW)	6.8	6.8
Standby Power (μW)	1.1	1.1
Max. clk. freq. (GHz)	1.3	1.5

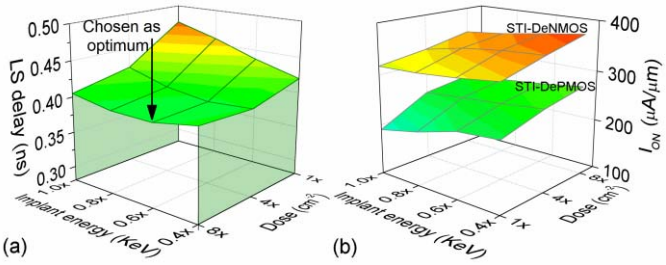

Fig. 6. (a) LS delay with dose and implant energy matrix (b) STI-NMOS and STI-DePMOS ON current with dose and implant energy matrix.

References

[1] M. Shrivastava, et al., "Part I: Mixed-Signal Performance of Various High-Voltage Drain-Extended MOS Devices," *IEEE Trans. Electron Devices*, vol. 57, no. 2, pp. 448–457, Feb. 2010.

[2] P. S. Swain, et al., "Device-circuit co-design for beyond 1 GHz 5 v level shifter using demos transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3827–3834, 2013.

[3] M. Shrivastava, et al., "A drain-extended MOS device with spreading filament under ESD stress," *IEEE Electron Device Lett.*, vol. 33, no. 9, pp. 1294–1296, 2012.

[4] Sentaurus Device User Guide, Synopsys Inc., Version C-2009.06.

[5] M. N. Darwish, "Study of the quasi-saturation effect in VDMOS transistors," *IEEE Trans. Electron Devices*, vol. 33, no. 11, pp. 1710–1716, Nov. 1986.