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A Systematic Study on the Hysteresis Behaviour and Reliability of MoS_2 FET

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***Abstract*—For reliable use of Molybdenum Disulfide (MoS_2) FETs in ULSI applications device reliability issues like hysteresis behaviour and non idealities must be well understood and mitigated. In this work, we present unique hysteresis behaviour in the I-V characteristics of few layer MoS_2 FETs. Root cause and physics behind the hysteresis behaviour has been explored by repeated experiments under various electrical, temperature, pressure, and environmental conditions. A trap based theory is proposed considering the device behaviour in different conditions and these observations give insight towards device passivation and choosing the right dielectric for reliable utilization of MoS_2 FETs.**

I. Introduction

There is a great interest in understanding the physics and advancing the VLSI processing methods of 2D materials like TMDCs for beyond CMOS applications, which is triggered by the advances in graphene and its vast applications. This is attributed to natural scalability and other distinctly unique properties of such materials. After graphene, various groups have given a lot of attention to molybdenum disulfide (MoS_2) among various TMDCs, which is a layered material similar to graphene however with a direct bandgap of 1.8 eV (single layer MoS_2). On one hand a number of studies have demonstrated great potential of MoS_2 FETs for applications in VLSI, sensors and photonics. However, device reliability has been greatly untouched. Recently hysteresis behaviour in the I-V characteristics of MoS_2 FETs was reported, which was attributed to electron capture by water molecules [1]–[4]. However, a systematic study of repeatability, device degradation, comparison of hysteresis behavior under various temperature, pressure, and environmental conditions along with gate current studies during these conditions are missing in literature. Moreover, root cause for fast device degradation and the hysteresis behaviour is also not well explained in the available literature. These are addressed in this work.

II. Device Fabrication and Experimental Setup

Single-layer and few-layer MoS_2 flakes were obtained by means of mechanical exfoliation on 300nm thick thermally grown SiO_2 wafer. These flakes were first identified using optical microscopy and number of layers was determined using Raman spectroscopy and AFM (Fig. 1). Contact pads were deposited using E-beam lithography followed by E-beam evaporation of Ti/Au (5/70nm). Highly doped Si was used as back gate for process simplicity (Fig. 2). The device characteristics were extracted, while using a cryogenic probe station. The best I_{ON}/I_{OFF} among 10 devices was $5x10^4$ and measured low field mobility, as extracted using $\mu = \frac{(\frac{dI_{DS}}{dV_{GS}})L}{C_i W V_{DS}}$ was $11 cm^2 V^{-1} s$. The hysteresis behaviour was investigated at 3 different temperatures (77K, 300K and 400K), three different environmental conditions (low pressure / vacuum, atmospheric pressure and ambient condition) and two different electrical modes (single sweep and dual sweep with varying gate stress range). After each stress cycle, device was electrically annealed to recover it to its initial state.

III. Results and Observations

Electrical characterization of MoS_2 FETs under different ambient and temperature conditions reveals strong dependence of its I-V characteristics on the ambient as well as temperature conditions (Fig. 2). For example, it was observed that drain current increases with increase in temperature for a given gate bias whereas gate loses its control on the channel at higher temperatures. Moreover, non-linearity in the output characteristics can be seen at low temperatures and low pressure conditions. This is attributed to Schottky S/D contacts. However, the same gets linear under atmospheric conditions (Fig. 2). This can be attributed to presence of trapping states induced by absorbed water molecules over the MoS_2 surface [1] [2]. These trends have unique device reliability consequences, unlike Si FETs, as discussed below [1] [2]. These trends have unique device reliability consequences, unlike Si FETs, as discussed below.

Repeated I_D vs. V_D measurements at low temperature and room temperature under low pressure / vacuum conditions reveal no observable drift and hysteresis in the drain current (Fig. 3 (a)-(b)). However, the same at high temperature in vacuum (low pressure) and at room temperature under atmospheric condition give rise to a noticeable drift in the drain current and hysteresis after repeated stress cycles (Fig. 3(c)-(d) . Similar observations can be drawn from repeated I_D vs. V_G measurements in dual sweep mode, however with much stronger drain current upward shift with hysteresis in drain current (Fig. 4). Note that we have observed an anticlockwise hysteresis behaviour unlike reported in the other work [1]. Moreover, a pronounced hysteresis was seen in case of slower gate ramp. Fig. 3 and Fig. 4 reveal that gate stress has much stronger impact on device reliability compared to drain stress. This is further validated in Fig. 5. Reduction in drain current can be noticed when device was stressed under atmospheric conditions. However, an increase in drain current can be clearly seen when gate was stressed under vacuum at high temperature. Fig. 6 compares hysteresis behaviour under 4 different measurements conditions and depicts that largest hysteresis was present under atmospheric conditions followed by high temperature conditions. A noticeable hysteresis behaviour was observed even at low temperatures (and low pressure) when

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gate was overdriven (Fig. 7). This further validates strong influence of gate stress on device reliability.

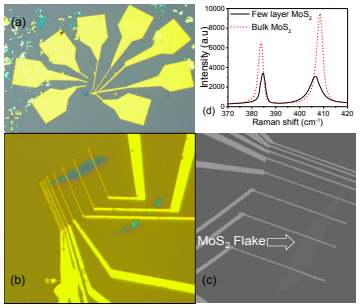

Fig. 1. (a−c) Optical and SEM Micrograph of fabricated back-gated MoS_2 FET. (d) Raman spectra of exfoliated few layer and bulk MoS_2 used in this work.

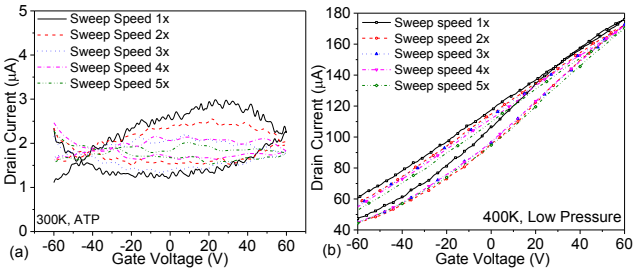

Fig. 4. Repeated I_D-V_G measurement (at V_D=1V) of MoS_2 FET depicting hysteresis behaviour under following conditions: (a) 300K, ATP and (b) 400K, Low pressure.

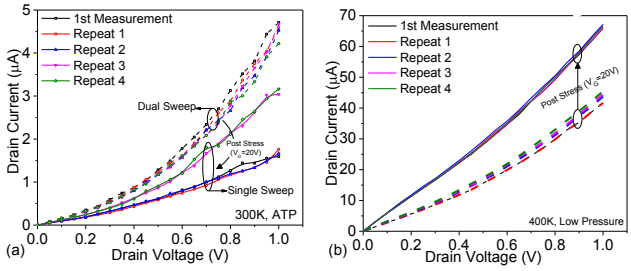

Fig. 5. : Repeated I_D-V_G measurement (at V_D=1V) of MoS_2 FET depicting hysteresis behaviour under following conditions: (a) 300K, ATP and (b) 400K, Low pressure.

Unlike the previous studies [1] [2], we explored the gate leakage trends as well. No noticeable gate current and drift was observed at 77K and 300K under low pressure conditions. However, a gradual positive shift in the gate current when stressed at 400K (vacuum) (Fig. 8) was noticed. Moreover, an asymmetric hysteresis in gate current can be observed with higher hysteresis area for $V_G > 0$V and negligible hysteresis area when $V_G < 0$. Interestingly, no noticeable drift in gate current and a symmetric hysteresis behaviour was observed when stressed under atm. conditions (Fig. 9). These observations (Fig. 2-9) indicate competing events changing the device degradation and hysteresis trends under different conditions. It was noticed that devices re-gain its original

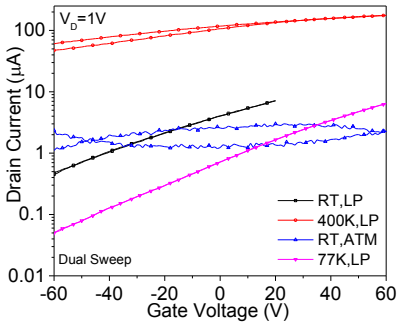

Fig. 6. I_D-V_G measurement of MoS_2 FET comparing hysteresis behaviour at (i) 300K, low pressure; (ii) 400K, low pressure; (iii) room temperature, atmospheric pressure; and (iv) 77K and low pressure.

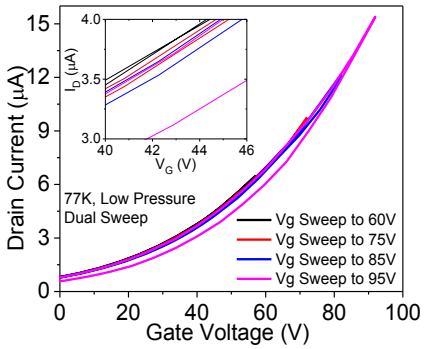

Fig. 7. I_D-V_G measurement (at V_D=1V) of MoS_2 FET depicting an increase in the strength of hysteresis behaviour with increased range of gate voltage sweep.

characteristics from its degraded state after stressing gate with -60V for a longer period (Fig. 10). This indicates that hysteresis behaviour and device degradation in MoS_2 FETs are related to filling of traps at the MoS_2-SiO_2 interface and electron trapping by water molecules (moisture) present over MoS_2 surface (discussed below).

Based on the observations above we propose a double sided-dual trap mechanism, unlike reported elsewhere [5]. The hysteresis behaviour and current drift seen is attributed to presence of deep and shallow traps present at the MoS_2-SiO_2 and shallow traps at MoS_2-H_2O interface with different charge trapping or de-trapping time constants. Deep traps at MoS_2-SiO_2 interface (Fig. 11-12) leads to drift in drain and gate current whereas shallow traps at MoS_2-SiO_2 interface and electron trapping at MoS_2-H_2O interface give rise to competing hysteresis behaviour. The competing hysteresis behaviour as reported above is attributed to trapped electrons in the water molecule (under atmospheric conditions), which acts as a virtual gate with negative charge sheet. Furthermore, at higher temperatures, increased electron concentration in the MoS_2 layer increases trapping probability; hence hysteresis and current drift. The contribution of hysteresis from water molecules is larger due to higher trap density and electron trapping (Fig. 12), which is evident from the submerged gate current drift and hysteresis caused by SiO_2-MoS_2 interface traps (Fig. 8-9).

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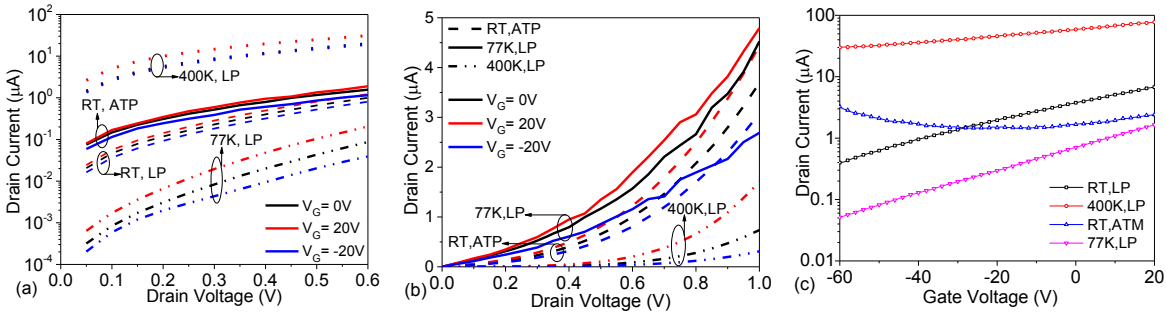

Fig. 2. (a b) I_D-V_D and (c) I_D-V_G characteristics (at V_D=1V) of MoS_2 FET under different atmospheric conditions. Here LP stands for low pressure, RT is room temperature and ATP stands for Atmospheric pressure condition.

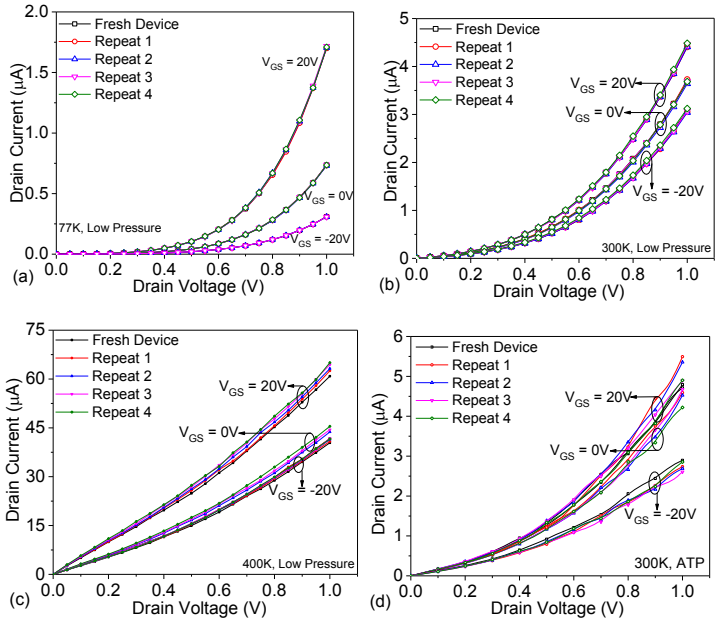

Fig. 3. Repeated I_D-V_D measurement of MoS_2 FET at V_G= 0V, 20V and -20V under different conditions (a) 77K, Low pressure, (b) 300K, Low pressure, (c) 400K, Low pressure and (d) 300K, atmospheric pressure

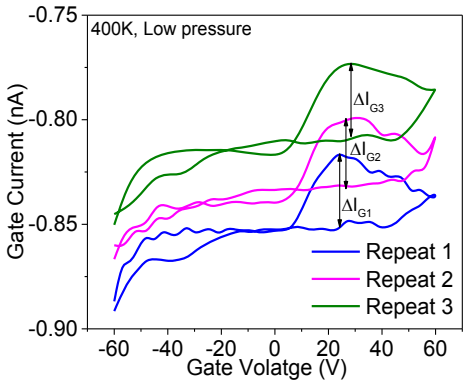

Fig. 8. Gate current vs. gate voltage characteristics (at V_D=1V), depicting hysteresis behaviour in gate current, extracted after repeated stress measurements under dual sweep configuration at 400K and low pressure condition.

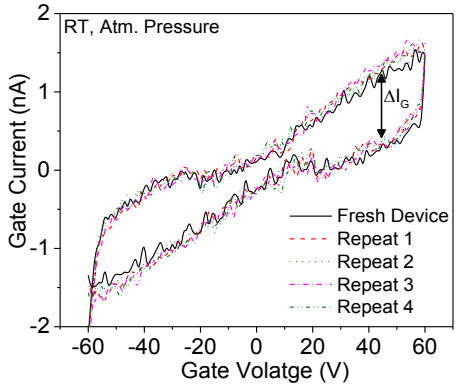

Fig. 9. Gate current vs. gate voltage characteristics, depicting hysteresis behaviour in gate current, extracted after repeated stress measurements under dual sweep configuration at room temperature and atmospheric pressure condition

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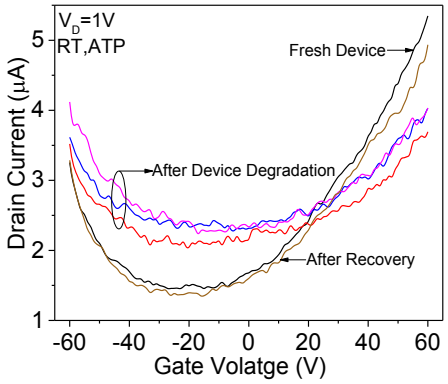

Fig. 10. I_D-V_G measurements depicting device degradation while stressing under atmospheric conditions and complete recovery after negative gate stress.

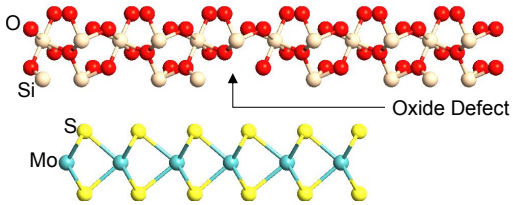

Fig. 11. Atomistic model of SiO_2-MoS_2 interface with oxide defect used to compute electron density using density functional theory and transport using NEGF formalism

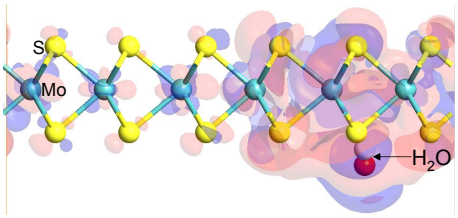

Fig. 12. Charge Density Difference contour superimposed with atomistic model of H_2O-MoS_2 interface used to compute electron density using density functional theory. Cyan (Blue) indicates accumulation (depletion) of charge.

IV. Conclusion

For reliable use of MoS_2 as a channel material for beyond CMOS nodes, device reliability and hysteresis behaviour must be clearly understood. We observe unique hysteresis and degradation trends in MoS_2 FET under different atmospheric, temperature and bias conditions. We have proposed a double sided - dual trap mechanism to explain the hysteresis behaviour and drift in gate and drain current. Importance of traps at the $MoS_2 - SiO_2$ and $MoS_2 - H_2O$ interface with different charge trapping or de-trapping time constants is briefly discussed. Finally, based on the observations, we suggest a vacuum dehydration followed by surface passivation to minimize the influence of moisture.

V. Acknowledgment

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